

# Exhibit 6

No. 21-1772

# United States Court of Appeals for the Federal Circuit

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ACQIS, LLC,  
*Plaintiff-Appellant,*

– v. –

EMC CORPORATION,  
*Defendant-Appellee.*

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On appeal from the United States District Court  
for the District of Massachusetts, No. 1:14-cv-13560-ADB,  
Hon. Allison Dale Burroughs

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## **CORRECTED BRIEF FOR PLAINTIFF-APPELLANT**

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**U.S. Patent No. RE43,171 (Claim 24)**

24. A method comprising: providing a computer module, the module comprising  
a central processing unit,  
a connection program,  
an integrated interface controller and bridge unit to output an  
encoded serial bit stream of **address and data bits of [a  
Peripheral Component Interconnect (PCI) bus  
transaction]**, the integrated interface controller and bridge unit  
coupled to the central processing unit without any intervening  
PCI bus, and  
a low voltage differential signal channel coupled to the integrated  
interface controller and bridge unit to convey the encoded serial  
bit stream of PCI bus transaction,  
inserting the computer module into a computer console, the computer  
console having access to a network,  
receiving connection information from the computer console,  
configuring the connection program to adapt to the connection  
information, and  
establishing a connection between the computer module and a server  
coupled to the network,  
wherein the low voltage differential signal channel further comprises  
two sets of unidirectional serial bit channels which transmit  
data in opposite directions.

*(Disputed text emphasized)*

## **CERTIFICATE OF INTEREST**

Pursuant to Federal Circuit Rule 47.4, counsel for Plaintiff-Appellant, certifies the following:

1. The full name of the party represented by me is ACQIS LLC.
2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me: N/A.
3. Parent corporations and publicly held companies that own 10% or more of stock in the party: ACQIS Technologies, Inc.
4. The names of all firms and the partners or associates that appeared for the party now represented by me in the trial court or are expected to appear in this Court (and who have not or will not enter an appearance in this case) are:

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5. The title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal:
  - *ACQIS LLC v. Samsung Elecs. Co., et al.*, No. 2:20-cv-00295 (E.D. Tex.);
  - *ACQIS LLC v. Acer Inc.*, No. 2:21-cv-00275 (E.D. Tex.);
  - *ACQIS LLC v. MITAC Holdings Corp., et al.*, No. 6:20-cv-00962 (W.D. Tex.);
  - *ACQIS LLC v. Inventec Corp.*, No. 6:20-cv-00965 (W.D. Tex.);
  - *ACQIS LLC v. Asustek Comput., Inc.*, No. 6:20-cv-00966 (W.D. Tex.);
  - *ACQIS LLC v. Lenovo Grp. Ltd., et al.*, No. 6:20-cv-00967 (W.D. Tex.);
  - *ACQIS LLC v. Wistron Corp., et al.*, No. 6:20-cv-00968 (W.D. Tex.).
6. The organizational victims and bankruptcy cases applicable to this appeal: N/A.

Dated: August 16, 2021

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## STATEMENT OF RELATED CASES

Pursuant to Federal Circuit Rule 47.5, Appellant ACQIS, LLC states that the following is a list of related cases:

- *ACQIS LLC v. Samsung Elecs. Co., et al.*, No. 2:20-cv-00295 (E.D. Tex.);
- *ACQIS LLC v. Acer Inc.*, No. 2:21-cv-00275 (E.D. Tex.);
- *ACQIS LLC v. MITAC Holdings Corp., et al.*, No. 6:20-cv-00962 (W.D. Tex.);
- *ACQIS LLC v. Inventec Corp.*, No. 6:20-cv-00965 (W.D. Tex.);
- *ACQIS LLC v. Asustek Comput., Inc.*, No. 6:20-cv-00966 (W.D. Tex.);
- *ACQIS LLC v. Lenovo Grp. Ltd., et al.*, No. 6:20-cv-00967 (W.D. Tex.);
- *ACQIS LLC v. Wistron Corp., et al.*, No. 6:20-cv-00968 (W.D. Tex.).

## INTRODUCTION

ACQIS is a pioneer in modular computing. A “modular” computer consists of computer “modules” attached to a shared “console.” Each module contains the core elements of a computer, and the console provides modules access to shared resources.

ACQIS invented a technique for connecting modules to the consoles using a new “interface channel” that was faster, more efficient, and less costly than existing channels, but still compatible with existing software because it could still communicate the “transactions” defined by the dominant communication standard of the time—the “Peripheral Component Interconnect” Standard (“PCI Standard”).

To protect this invention, ACQIS obtained the eight asserted patents, which belong to three patent families. *See* Appx2495–2498 (¶¶ 95–97) (illustrating family relationships). Each claims a computer module employing the new interface channel to transmit at least some portion of a “PCI bus transaction” between a processor and peripheral device.

The PCI Standard was succeeded by the “PCI Express” standard (“PCIe”), which adopted the same new interface channel ACQIS invented.

EMC makes and sells computer modules that use PCIe to connect processors to peripheral devices. ACQIS filed suit because those EMC computer modules use the claimed interface channel to communicate “PCI bus transactions.”

After over a decade of litigation—in which the first district court to consider the issues construed the claims in ACQIS’s favor and the PTAB upheld all of ACQIS’s claims—the district court granted EMC summary judgment of non-infringement against all asserted claims on the basis that PCIe does not communicate “PCI bus transactions,” as construed by the district court.

That was error for three reasons. First, the district court erroneously refused to consider ACQIS’s arguments about the meaning of “PCI bus transaction” as supposedly untimely. Second, the district court’s construction of that phrase was wrong. Third, its construction of “PCI bus transaction” does not support summary judgment of non-infringement against *all* asserted claims. Because the district court granted summary judgment against all claims based on these errors, the Court should reverse and remand.

### **STATEMENT OF JURISDICTION**

The United States District Court for the District of Massachusetts had jurisdiction over this case pursuant to 28 U.S.C. §§ 1331 and 1338(a). It entered final judgment through an Order of Dismissal on February 19, 2021. Appx14, Appx3558. Appellant timely filed a notice of appeal on March 19, 2021. Appx3559. This Court has jurisdiction pursuant to 28 U.S.C. § 1295(a)(1).



## STATEMENT OF THE ISSUES

1. Whether the district court erred by (a) declining to consider ACQIS's claims based on an erroneous finding of waiver, (b) granting summary judgment of non-infringement based on a fundamentally flawed construction of "PCI bus transaction," and (c) doing so even as to claims that recited communicating only the "address and data bits" of a transaction that the court construed such a transaction to require.
2. Whether the district court misconstrued "communicating ... a PCI bus transaction" based on an apparent agreement between the parties that did not exist.
3. Whether the district court misconstrued "encoded ... (PCI) bus transaction" based on a prosecution disclaimer that had not occurred.

## STATEMENT OF THE CASE

### A. Technology Background

The primary question on appeal is what information constitutes a "PCI bus transaction." According to ACQIS, a PCI bus transaction is the information exchanged between PCI components. According to EMC and the district court, a transaction is that information *plus* signals for controlling the physical medium over which that information used to be exchanged. Deciding this issue requires understanding (1) the PCI Standard, (2) improvements claimed in the asserted patents, and (3) the PCIe standard.

### 1. *PCI Standard*

Computer processors communicate with peripheral devices such as mice, keyboards, and graphics cards. In the 1990s, the “most widely accepted and implemented [peripheral device communication] standard in the world” was the PCI Standard. Appx2466–2473 (¶¶ 42–57). That standard was published in the 1992 “PCI Local Bus Specification” (“PCI Specification”). Versions 2.1 and 2.2 followed in 1995 and 1998. Appx2236; Appx2467–2468 (¶¶ 45–47); *see* Appx2235–2359.

The PCI Standard defines (1) a “transaction” layer and (2) a “physical layer.” Appx2469 (¶ 48). The “transaction layer” defines the messages (“transactions”) that PCI components communicate. The “physical layer” defines the physical infrastructure that communicates those transactions and signals used to control that physical infrastructure. *Id.* Analogizing to a telephone call, the transaction layer defines the content of a telephone conversation (*i.e.*, the message), whereas the physical layer defines both the telephone network’s physical infrastructure and the signals for controlling that infrastructure (*i.e.*, signals for establishing and maintaining a connection).

#### a) *PCI Transaction Layer*

PCI components communicate by exchanging PCI “transactions.” *See* Appx1205–1207 (¶¶ 61–66). Those transactions are “the information

conveyed” between two PCI components. Appx2505 (¶ 110); *see also* Appx1205 (¶ 61).

A “transaction” is conveyed in at least two phases: “an address phase followed by one or more data phases.” Appx2246 (footnote omitted); *see also* Appx2470 (¶ 50). A “phase” is a time period “in which a single unit of information is transferred.” Appx3396–3397 (¶ 18). Data transferred in paired address and data phases typically include (1) “command bits,” (2) “address bits,” (3) “data bits,” and (4) “byte enables.” *See* Appx1205 (¶ 61); Appx3397 (¶¶ 19–20).

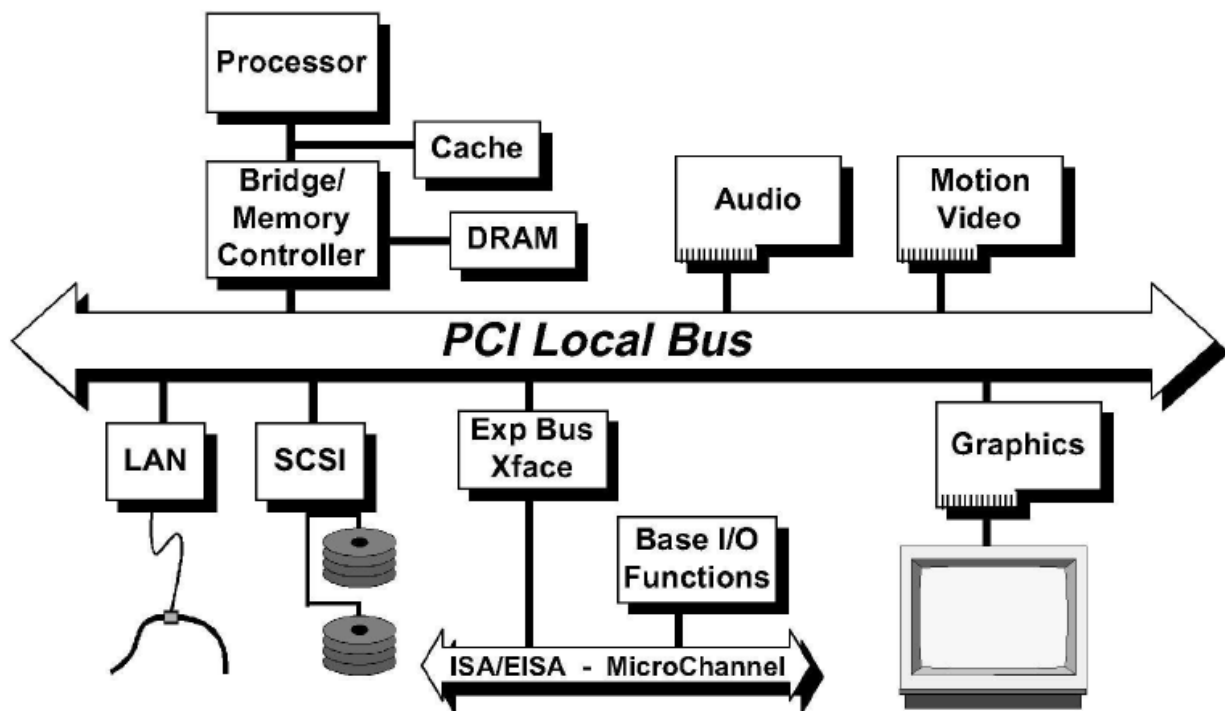
During the “address phase,” the devices exchange: (1) “command bits” and (2) “address bits.” Appx2470, Appx2472 (¶¶ 51, 54). “Command bits” indicate what PCI command is being performed. Appx2470, Appx2505 (¶¶ 50, 110); Appx1205 (¶ 61). Example commands include reading data from (or writing data to) a given location in memory. Appx2470, Appx2505 (¶¶ 50, 110); Appx1205 (¶ 61). The “address bits” indicate the memory locations (*i.e.*, memory “addresses”) that the command targets. Appx2470, Appx2505 (¶¶ 50, 110). For example, if the command is to write data, the “address bits” indicate the memory address to write to. Appx2470 (¶ 50). For different types of commands, the PCI Standard defines different formats for the address bits, as well as different “address spaces” (*i.e.*, reserved areas of memory) where the commands operate. Appx2470–2471, Appx2585 (¶¶ 51, 220).

“[D]ata phases” follow “address phase[s].” Appx2472–2473 (¶ 56). During data phases, the PCI components exchange two types of information: (1) “data bits” and (2) “byte enable[s].” *Id.* The data bits indicate the data for the transaction. *Id.* For example, if the command was to write data in the address phase, then the data bits are the data to write to the memory address also identified during that address phase. *Id.* The “Byte Enables” indicate which of the data bits are used. Appx2246. Thus, the transaction layer specifies the information to be communicated, the address, and the operation.

#### b) PCI Physical Layer

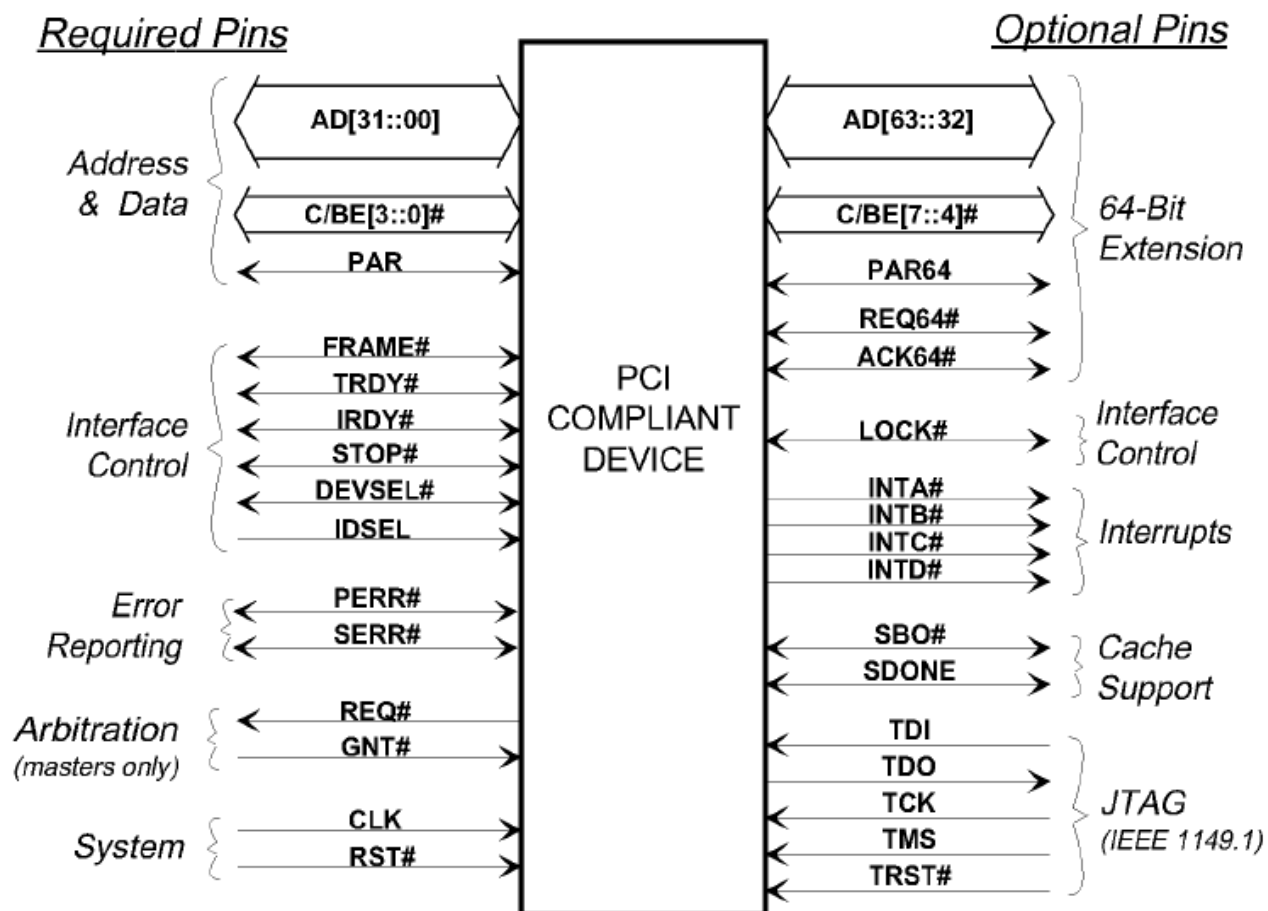
Whereas the “transaction layer” defines the information communicated, the PCI Specification’s “physical layer” defines (1) the physical infrastructure that communicates transactions and (2) signals that coordinate this communication across that physical infrastructure. Appx2469 (¶¶ 48–49).

The figure below shows an example system’s physical infrastructure using the PCI Standard.



Appx2240. This figure shows a processor and peripheral devices (e.g., audio, video, and graphics cards) connected to the bus. Appx1204–1205 (¶ 58–60). The salient physical feature of the PCI Standard is the “PCI Local Bus”—a physical broadcast medium to which the PCI components connect and through which they exchange transactions. Appx2466–2473 (¶¶ 42–57).

The diagram below details the physical “interface” (i.e., the wiring) by which components connects to the PCI Local Bus. Appx2469 (¶ 49).



Appx2469 (¶ 49). The left hand shows the “Required Pins” (*i.e.*, wires) for connecting to the bus, and the right side shows optional pins. As shown, at least 47 “pins” are required of all components and another two for components that initiate transactions (“masters”). Appx2469 (¶ 49).

Thirty-two “AD” (“address and data”) pins and four “C/BE” (“command and byte enable”) pins transmit the address, data, command, and byte enable bits described above. Appx2246. During the address phase, the 32 AD pins (“AD[31::00]”) transmit 32 address bits, and the four C/BE pins (“C/BE [3:00]#”) transmit four command bits, one bit across each pin in parallel, *i.e.*, simultaneously. Appx1854–1855 (¶ 140). During subsequent

data phases, the 32 AD pins transmit the 32 data bits, and the four C/BE pins transmit the four byte enables. Appx1854–1855 (¶ 140). The bits transmitted on the four C/BE pins (*i.e.*, “command” in the address phase and “byte enables” in the data phases) are referred to as the “control bits” because they control what the target PCI component does with the data it receives. Appx2473, Appx2599 (¶¶ 57, 239); Appx3419–3420 (¶ 83).

The remaining 13 required pins control transmission of the transaction. Appx3399 (¶ 26). For example, two “arbitration” pins obtain control of the physical parallel PCI bus. Appx3399–3400 (¶¶ 26–27); *see also* Appx1854–1855 (¶ 140). Six “Interface Control” pins coordinate communication of the transaction over the physical parallel PCI bus—*e.g.*, by indicating which device is the recipient (DEVSEL#), when it is ready to receive the transaction (IRDY# and TRDY# signals), and when a transaction starts and ends (FRAME# signals). Appx1854–1855 (¶ 140). Additional signals control timing (CLK), detect and report transmission errors on the physical parallel PCI bus (“PAR”, SERR#, and PERR#), and reset (RST#). Appx1854–1855 (¶ 140).

## 2. *Patented Technology*

The asserted patents concern modular computers that communicate at least some portion of a “PCI bus transaction” between a processor and a peripheral device. Appx2498–2501 (¶¶ 98–102).

Each module contains the core elements of a computer (*e.g.*, processor, memory), and shared consoles provide those modules with access to shared peripheral devices (*e.g.*, I/O devices, mass storage devices, *etc.*). *Id.* Modular computers are popular in data centers, which arrange thousands of computer servers on “racks” that provide shared peripherals. Appx2463–2464 (¶¶ 35–38).

a) The Problem: Backwards Compatibility

In the 1990s, ACQIS recognized that the demand for data centers would grow exponentially and that modular computers could lower data center costs, reduce space requirements, improve energy efficiency, and ease maintenance. Appx2490–2491, Appx2498, Appx2500–2501 (¶¶ 84, 98, 102). But making modular computing feasible in these environments required confronting the PCI Standard’s shortcomings. Appx2501 (¶ 103).

At the time, “the ability to execute a PCI bus transaction was required for a computer system to be commercially acceptable.” Appx2501 (¶ 103). But the PCI Standard’s *physical layer* was ill-suited for modular computing. Appx2501 (¶ 103). The 47-pin connections were too cumbersome for densely packed data centers (Appx37 (3:35-49); Appx2462, Appx2463–2464 (¶¶ 32, 36–38)), expensive, and energy inefficient (Appx37 (3:35); Appx2501 (¶ 122)). Moreover, such connections were slow: the “shared bus topology,” which required that “only one device can ‘talk’ at any one time,” is ill-suited for connecting a large number of components. Appx2512 (¶¶ 121–22). And



so many wires in “parallel” created reliability issues (due to electromagnetic interference and signal “skew”), exacerbated by the long cable lengths required. Appx2464–2465 (¶ 39); Appx37 (3:64–65). These issues made it impractical for ACQIS to connect modules to consoles using PCI buses. Appx2502 (¶ 105).

Nevertheless, ACQIS could not abandon the PCI Standard because “the ability to execute a PCI bus transaction was required for a computer system to be commercially acceptable.” Appx2501 (¶ 103). Accordingly, ACQIS had to overcome these problems while still supporting the Standard.

b) ACQIS’s Solution.

ACQIS solved the problem by replacing parallel buses with *serial* interface channels—specifically, “low voltage differential signal” (“LVDS”) channels—that maintained backwards compatibility with the PCI Standard. Appx37 (3:64-65) Appx38 (5:31-62); Appx2503 (¶ 107). “Serial” channels send data one bit at a time, as opposed to “parallel” channels, which send multiple bits, “in parallel” (*i.e.*, simultaneously). Appx2464–2466 (¶¶ 39–41). ACQIS replaced the parallel PCI bus with a new serial interface channel that used far fewer pins/wires and thus mitigated the bulk, cost, energy, and performance shortcomings of the PCI Standard’s physical layer. Appx38 (5:31–62).

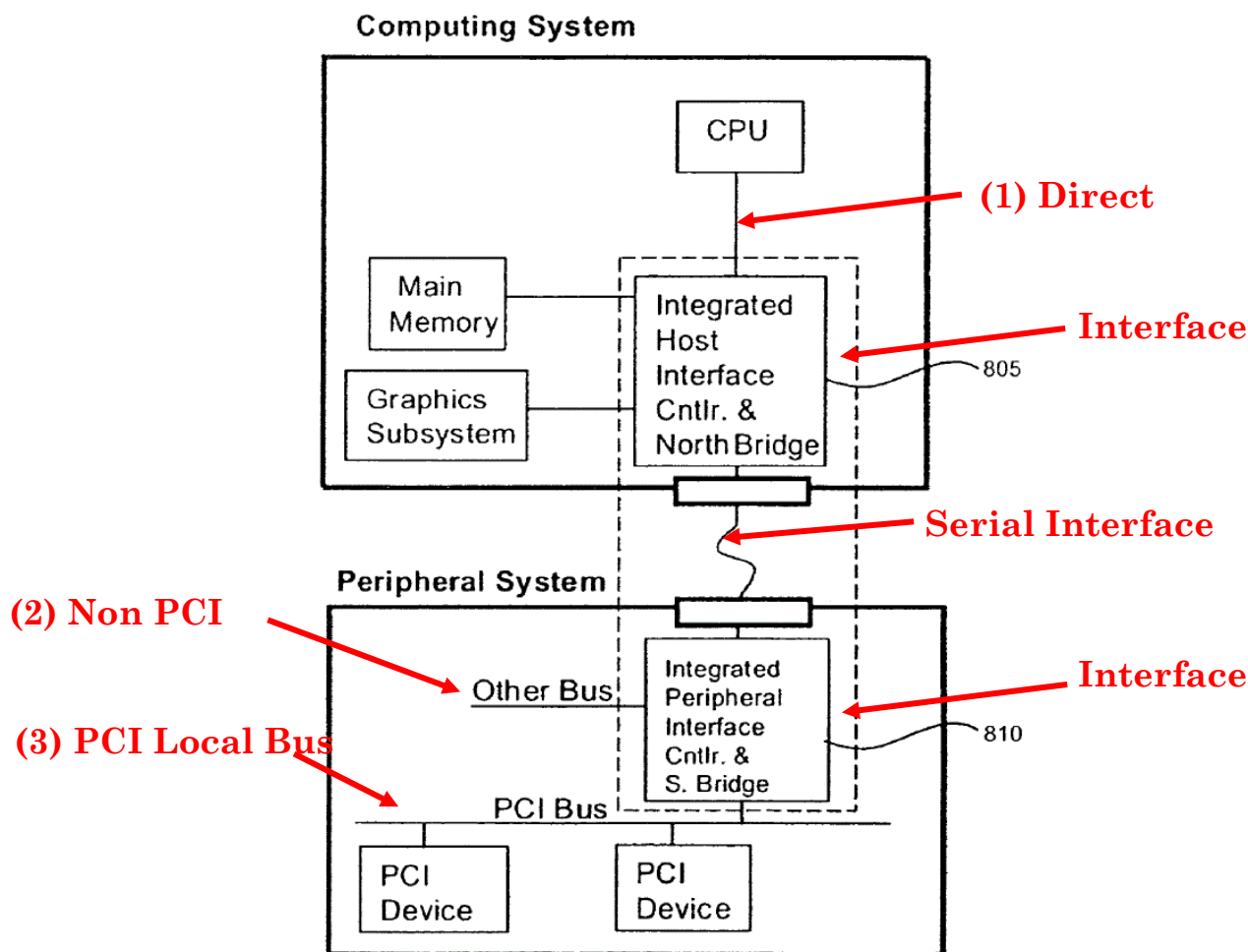
ACQIS added “interface controllers” that enabled the serial interface channel to communicate the same PCI transactions defined by the PCI

Standard and therefore remain compatible with existing PCI software. Appx2491 (¶ 85). The interface controllers included “translators” for encoding and decoding PCI data received from PCI components, a “transmitter” for transmitting encoded data on the new serial channel, and a “receiver” for PCI data from the serial interface channel. Appx38 (6:37-49). In addition, for some applications, ACQIS integrated the serial interface channel directly into a processor.

Thus, ACQIS replaced the PCI Standard’s physical layer (including the parallel PCI Local Bus) with this combination of serial interface channels and interface controllers, yet it maintained backwards compatibility by enabling the new physical layer to communicate PCI Standard bus transactions.

#### c) Asserted Patents

The eight asserted patents each disclose a modular computer that communicates at least some part of a “PCI bus transaction” over serial interface channels. For example, Figure 8 of the ’415 Patent is a block diagram showing a “Computing System” (computer module) and a “Peripheral System” (console), connected by a serial interface channel. As shown, access to that channel is controlled on either end by an “interface controller.”



'415 Patent (Fig. 8) (annotations in red).

PCI components connect to interface controllers any way, such as by using a (1) Host CPU Bus, (2) non-PCI bus, or (3) PCI Local Bus. In Figure 8, the CPU connects *directly* to the “host interface controller” (805) whereas “Peripheral System” components connect to the “peripheral interface controller” (810) through a legacy PCI Local Bus or “other bus.” Appx44 (17:65-67) (serial interconnect “may be used to interface ... PCI-like buses”).

Where the PCI components connect to the interface controller using a PCI Local Bus (e.g., Figure 7 of the '415 patent), the interface controllers

capture and communicate *both* PCI transaction *and* PCI physical layer signals so those signals may be recreated on the receiving end. '415 Pat. (16:48-54, 20:43-48). Physical layer signals are captured and processed using different hardware than the transaction data. '415 patent (17:16-54). For example, a “control encoder” reads the parallel control signals from the PCI Local Bus, records them in memory as additional “control bits,” and passes them to a “transmitter” for transmission across the serial interface channel. '415 patent (17:35-41). At the transmitter, the control bits in memory are “serialized by parallel to serial converters” (*e.g.*, grouped into 10-bit packets) and transmitted across the serial interface channel. '415 patent (18:1-7).

d) Asserted claims

Each asserted claim recites a modular computer system that uses interface controllers to communicate at least some part of a “PCI bus transaction” across a serial interface channel. Seven claims recite that the controllers communicate the entire “(PCI) bus transaction”<sup>1</sup> or the “data of ... [a] (PCI) bus transaction.”<sup>2</sup> Four recite that the controller communicates

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<sup>1</sup> '873 patent (cls. 29 and 61) (Appx163, Appx165); '294 patent (cl. 44) (Appx195).

<sup>2</sup> '416 patent (cl. 60) (Appx52); *see also* '487 patent (cls. 38 and 49) (Appx104, Appx105) (“bus transaction data”).

only the “*address and data bits* of a ... (PCI) bus transaction” (the “Address and Data Claims”).<sup>3</sup>

Each of those Address and Data Claims recites that the CPU connects to the controller “*without any intervening PCI bus.*” Claim 24 of the ’171 patent is one such example:

24. A method comprising: providing a computer module, the module comprising  
 a central processing unit,  
 a connection program,  
 an integrated interface controller and bridge unit to output an  
 encoded serial bit stream of **address and data bits of [a]  
 Peripheral Component Interconnect (PCI) bus  
 transaction**, the integrated interface controller and bridge unit  
 coupled to the central processing unit **without any  
 intervening PCI bus**, and  
 a low voltage differential signal channel coupled to the integrated  
 interface controller and bridge unit to convey the encoded serial  
 bit stream of PCI bus transaction,  
 inserting the computer module into a computer console, the computer  
 console having access to a network,  
 receiving connection information from the computer console,

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<sup>3</sup> ’171 patent (cl. 24) (Appx332); ’468 patent (cl. 29) (Appx372); ’814 patent (cl. 31) (Appx246); ’119 patent (cl. 38) (Appx293) (“(‘PCI’) bus transaction address and data”).

configuring the connection program to adapt to the connection information, and  
 establishing a connection between the computer module and a server coupled to the network,  
 wherein the low voltage differential signal channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

Appx332 (emphasis added).

### 3. *PCIe Standard*

In 2002, PCI Express succeeded the PCI Standard. Appx2473–2474 (¶ 59). “One of the most important design goals for PCIe was backward compatibility with PCI software.” Appx2476–2478 (¶ 63). To achieve compatibility, “PCI Express maintain[ed] the same standard transactions defined in the PCI Local Bus Specification.” Appx2479 (¶ 65). That is, PCIe defined “transactions” “using PCI standard addresses, data, encoded commands, and byte enables.” Appx2479–2484 (¶¶ 65–73). By maintaining the same transaction layer as PCI, PCIe was “100-percent compatible with conventional PCI compliant operating systems and their ... software.” Appx2476–2478 (¶ 63).

While retaining the PCI Standard’s transaction layer, PCIe replaced the *physical* layer. Appx2481 (¶ 68). Specifically, just as ACQIS had before,

it replaced the physical PCI Local Bus with a serial LVDS channel. Appx2473–2475 (¶¶ 59–61).

Thus, as ACQIS had, the PCIe standard ensured that “[k]ey PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its bus implementation is replaced by a highly scalable, fully serial interface.” Appx1781 (¶ 51).

## **B. Procedural Background**

EMC makes and sells modular computers using PCIe. Appx1774 (¶ 4). Those systems infringe because they use the claimed serial interface channel to communicate “PCI bus transactions.”

### *1. Eastern District of Texas*

On September 9, 2013, ACQIS filed an infringement suit against EMC in the Eastern District of Texas, which was assigned to Judge Davis. Appx2. After EMC moved to transfer to Massachusetts, Judge Davis agreed, but only after claim construction. Appx2.

After briefing and a *Markman* hearing on February 21, 2015, as relevant here, Judge Davis construed the phrases (1) “PCI bus transactions” and (2) “encoded ... PCI bus transactions.”

a) “PCI bus transaction”

The parties agreed that a “PCI bus transaction” refers to a transaction as defined in the PCI Standard, but disagreed over whether such a transaction must be “communicated over a PCI bus.” Appx505. This was a potentially dispositive non-infringement issue because the accused devices do not have PCI Local Buses.

ACQIS contended that no PCI Local Bus was required because a “PCI bus transaction” was the transaction layer “*information* content according to the PCI standard” (*i.e.*, the “command, address, and data” bits) and this information could be created *without* a PCI Local Bus. Appx390–395.

Judge Davis agreed with ACQIS and construed “PCI bus transaction” as “information, in accordance with the PCI standard, for communication with an interconnected peripheral component.” Appx506–507 (quotation marks omitted). He did not detail that information other than by referring to the Standard.

b) “encoded ... PCI bus transaction”

EMC argued that the claims require the “PCI bus transaction” to be “encoded,” and “encoding” means converting the transaction from parallel signals into bits for transmission on the serial interface channel. Appx454. EMC planned to argue that, because its products lack a PCI bus, the



“transactions” communicated do not start as parallel signals and therefore are never converted into bits for serial transmission.

Judge Davis rejected that argument too. He held that “an encoded PCI bus transaction does not require any parallel-to-serial conversion at all,” and that an “encoded” transaction is merely “code representing a PCI bus transaction.” Appx508; *see also* Appx390–398 (ACQIS arguing for this construction).

## 2. *Patent Trial and Appeal Board*

The District of Massachusetts stayed the litigation pending resolution of IPRs EMC had filed against claims 54 and 56-61 of the '873 patent (Appx1091) and claims 24 and 31-33 of the '814 patent (Appx1066). Appx3.

The parties again disputed the meaning of “PCI bus transaction” and “encoded ... PCI bus transaction.”<sup>4</sup> This time, EMC changed positions.

### a) “PCI bus transaction”

EMC now argued that a “PCI bus transaction” meant any “communication with an interconnected peripheral component,” without regard to the PCI Standard. Appx550. ACQIS again argued that a “PCI bus transaction” is the “command, address, and data information, in accordance with the [transaction layer of the] PCI standard.” Appx679, Appx673–685.

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<sup>4</sup> “Communicating ... a PCI bus transaction” was not at issue.

The Board rejected EMC’s argument, holding that a “PCI bus transaction” “refers to a particular industry standard, not to just any communication with an interconnected peripheral component.” Appx1094–1096. It therefore construed “PCI bus transaction” as a “(PCI) industry standard bus transaction.” Appx1094–1096. Like Judge Davis, the Board did not specify what the Standard requires. Appx1094–1095.

b) “encoded ... PCI bus transaction”

EMC also changed its tune on the “encoded” limitation, arguing that an “encoded” transaction simply means “converted or formatted from one form into another.” Appx972–973.

ACQIS argued that “encoded” meant certain reversible operations, including those that “(1) turn[] a signal into bits, (2) group[] bits into a specified size block, or (3) order[] bits onto one or more serial transmission lines.” Appx797–799. ACQIS emphasized that the definition does *not* require that the transaction begin as parallel signals. Appx1047 (50:12-22) (ACQIS arguing that it does not “matter where [the data] originates from”).

The Board did not construe this term because ACQIS *conceded* that the cited art “encoded” transactions under ACQIS’s construction—specifically, by using “8b/9b line encoding,” which groups bits into specified size blocks. Appx817. EMC agreed to the concession and therefore argued

that the Board “need not construe ‘encoded.’” Appx972–973. Consequently, *neither* party advocated a construction of “encoded” requiring a transaction to start as parallel signals. *See also* Appx1752 (¶ 57) (EMC arguing that such encoding “is not parallel-to-serial conversion.”)

### c) Final Written Decision

The Board upheld all challenged claims. After accepting ACQIS’s concession that the prior art’s “8b/10b line encoding” satisfies the “encoded” limitation (Appx1099–1100, Appx1104 n.4), it still found no invalidity because the prior art (*e.g.*, “Horst”) failed to communicate “PCI bus transactions.” Appx1099–1103. Rather, the prior art transmitted “TNet” transactions, which the Board held do not include “*any* address bits” or “*any* data bits” “of a PCI industry standard bus transaction,” Appx1100–1101 (emphasis added), exactly ACQIS’s argument. Appx1099–1103; Appx815, Appx820; *see also* Appx782, Appx793, Appx795, Appx801, Appx806, Appx808.

### 3. Subsequent District Court Claim Construction

After the stay was lifted, EMC argued that “critical developments during the IPRs” required the district court to revisit the constructions of (1) “PCI bus transaction,” (2) “encoded ... PCI bus transaction,” and (3) “communicating ... [a] PCI bus transaction.” Appx1121. According to

EMC, ACQIS had purportedly disclaimed its litigation positions with respect to these three terms at the IPR hearing. It had not.

a) “PCI bus transaction”

EMC urged the district court to reconsider the construction that “PCI bus transaction” does not require a PCI bus. Appx506–507. According to EMC, ACQIS purportedly disclaimed that construction by telling the Board that the absence of a PCI Local Bus in Horst is “one indicator” that Horst does not communicate PCI transactions. Appx1130–1131; Appx1043–1044.

The district court rejected that argument because ACQIS in fact had told the Board that “the claims don’t require a bus,” that the absence of a PCI bus in Horst was simply “one indicator,” and this indicator was “not determinative.” Appx1700–1704, Appx1707 (citing Appx3580–3581); *see also* Appx1043–1044 (“You don’t have to have the PCI bus” because “[y]ou could generate a PCI transaction without a bus”).

The district court then construed “PCI bus transaction” consistently with Judge Davis’s construction: a “transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” Appx1703–1704. Again, the district court did not say what information a “PCI bus transaction” must include to be “in accordance with the ... Specification.” Appx1704.

b) “encoded ... PCI bus transaction”

EMC urged the district court to revisit Judge Davis’s construction that “encoded” “does not require any parallel-to-serial conversion at all.” Appx508. According to EMC, ACQIS’s IPR arguments limited an “encoded ... PCI bus transaction” to one that had undergone parallel to serial encoding. Appx1136–1137.

ACQIS protested that it “never took the position that encoding required parallel-to-serial conversion.” Appx1175; *see* Appx1167–1170, Appx1173–1177. To the contrary, ACQIS had explicitly asked the Board to construe that term more broadly (Appx1168–1170, Appx1173–1175; *see also* Appx797–799), and it *conceded* that the prior art “encoded” based on that broader construction (Appx817; *see* Appx1099–1100, Appx1104 n.4).

Nevertheless, based on ACQIS’s statements at the hearing describing the importance of transmitting a transaction in serial form, the court held that ACQIS had “clearly and unmistakably” argued that “an encoded PCI bus transaction requires that a PCI bus transaction be encoded for serial transmission *from a parallel form*,”. Appx1704–1711 (emphasis added). The district court reached that incorrect conclusion because it misunderstood ACQIS’s emphasis on communicating data in *serial* form to imply that the data must have started in *parallel* form.

Based on this purported disclaimer, the district court construed “encoded ... PCI bus transaction” as “a PCI bus transaction that has been serialized *from a parallel form.*” Appx1711.

c) “communicating ... [a] PCI bus transaction”

EMC raised a new dispute concerning “communicating ... [a] PCI bus transaction.” Appx1137. EMC argued that, due to purported IPR disclaimer, that phrase meant “communicating a PCI bus transaction, including *all address, data and control bits, without discarding any of those bits.*” Appx1137 (emphasis added).

But ACQIS had never argued that the accused products communicate any less than an entire PCI bus transaction. Indeed, ACQIS’s position was that “communicating” simply carried its ordinary meaning, and any dispute over what “communicating ... [a] PCI bus transaction” means would be resolved by construing “PCI bus transaction.” Appx1147; *see also* Appx1177–1178; Appx1413; Appx1635 (220:1–5), Appx1642 (227:19-25).

Consequently, ACQIS agreed at the *Markman* hearing that “communicating ... [a] PCI bus transaction” means communicating “all address, data and control bits,” *provided that “control bits” refers to the command information.* Appx1643 (228:2–15) (“I think that’s right. Because I think you would communicate ... the address, *you do communicate a*

*command that tells you what you have to do* and then you send the data. So I think that’s right. That’s all right”) (emphasis added); *see also* Appx1643 (226:12–15) (“control bits ... refer[s] to the command” information). The court then adopted that construction pursuant to the agreement. Appx1711.

The parties did not agree on a construction for the related phrase “communicate *address and data bits of* [a] PCI bus transaction,” and similar variations, as recited in the Address and Data Claims. ACQIS argued that these claims could not require transmitting the address and data bits *and also the control bits*, because that would contradict those claims’ language. Appx1177–1180; Appx1635–1636 (220:15–221:6), Appx1637 (222:14–23).

ACQIS disputed having made any IPR disclaimer regarding the Address and Data Claims. Appx1176–1180. Rather, as ACQIS pointed out, the quotations EMC had cited to support its disclaimer argument dealt with ACQIS defining a “PCI bus transaction” generally or the requirements of claims other than the Address and Data Claims. Appx1177–1180.

#### 4. *Summary Judgment*

EMC moved for summary judgment of non-infringement based on each of those three constructions.

- a) “PCI bus transaction” / “communicating ... PCI bus transaction”

EMC primarily argued that the accused products do not communicate a “PCI bus transaction” because they do not communicate certain *physical layer signals*. Appx6–11, Appx12–13. According to EMC, both (1) a “transaction, in accordance with the ... PCI Local Bus Specification” and (2) “communicating ... control bits” require communicating certain physical layer signals, including the “interface control signals” and the “parity bit.” Appx1735–1736, Appx1738, Appx1764–1767. EMC argued that the accused products have no PCI Local Bus and therefore do not use these physical layer signals. Appx1735–1736.

ACQIS protested that the PCI Local Bus Specification requires only information for the *transaction layer*, and not the information described by the physical layer. Appx3347–3359, Appx3373–3376. Moreover, it argued that “control bits” refers only to the “command bits,” as ACQIS had made explicit at the *Markman* hearing. Appx3345–3347, Appx3347–3359.

ACQIS also argued that, even if a “transaction” requires these physical layer signals, summary judgment would still be inappropriate against the Address and Data Claims, which explicitly recite transmitting only the “address and data bits of a PCI bus transaction.” Appx3337–3338.



Finally, ACQIS argued that genuine fact disputes remained about whether PCIe communicates signals analogous to the disputed physical layer signals. Appx3373, Appx3376–3378; Appx3386–3388 (¶¶ 15–19, ¶ 21).

b) “encoded ... PCI bus transaction”

EMC also sought summary judgment of non-infringement because PCIe does not serialize PCI bus transactions *from parallel form*, as required by the district court’s construction. Appx1756.

ACQIS responded that as ACQIS’s expert had opined, “PCI Express data *is* ... sent to the parallel-to-serial converter for serialization before transmission over the serial PCI Express channels.” Appx3370–3372 (emphasis added). Thus, a genuine dispute of material fact barred summary judgment.

### **Summary Judgment Order**

Two and a half years later (and without oral argument), the district court granted EMC summary judgment of non-infringement. Appx1–13.

Although the 13-page order discussed each of EMC’s three arguments, its reasoning turned only on the court’s *reinterpretation* of “PCI bus transaction”: the district court (1) agreed with EMC that a “transaction, in accordance with the ... PCI Local Bus Specification” means information that includes the physical layer’s “control” and “parity” signals (Appx6–11), and

it held that, because the accused products lack a “PCI bus transaction,” they cannot (1) “communicat[e] ... [a] PCI bus transaction” or (2) “encode[] ... [a] (PCI) bus transaction” (Appx11–13).

The district court dismissed ACQIS’s counterarguments as “untimely” “attempt[s] to reopen claim construction.” Appx9. It refused to consider those arguments because “district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs.” Appx9–10.

The court never reached ACQIS’s separate arguments regarding the Address and Data Claims, which recite transmitting only the address and data bits of the transaction rather than an entire transaction. Nor did it reach ACQIS’s argument that genuine fact disputes remained about whether PCIe communicates signals analogous to the disputed physical layer signals.

## **SUMMARY OF THE ARGUMENT**

The district court erred by granting summary judgment of non-infringement based on a new and incorrect construction of “PCI bus transaction.”

I. Respecting the “PCI bus transaction” phrase, the district court made three errors.

*First*, the district court erred procedurally by refusing to consider ACQIS's claim construction arguments as untimely. ACQIS's arguments were timely raised at the first opportunity in response to a new issue *EMC* first raised at summary judgment.

*Second*, the district court erred on the merits by misconstruing "PCI bus transaction" to require physical layer signals, including "control" signals and "parity" bits. The ordinary meaning of that phrase (in light of the full intrinsic and extrinsic record) is the information required by the PCI Specification's transaction layer (*e.g.*, address, data, command, and byte enables), not physical layer signals. EMC's systems infringe because they send the transaction layer information required by the claims.

*Third*, the district court erred by granting summary judgment against the Address and Data Claims based on its construction of "PCI bus transaction." Because those claims recite transmitting only the "address and data bits" of the transaction rather than an entire transaction, they cannot reasonably be read to require transmitting physical layer "control" and "parity" signals. Yet, the district court granted summary judgment of non-infringement against these claims on the basis that the accused products do not send "control" and "parity" signals. This was error.

The Court should correct the district court's construction and reverse its grant of summary judgment at a minimum, it should remand for the district court to evaluate those arguments in the first instance.

**II.** This Court should also clarify the district court’s constructions of “communicating ... a PCI bus transaction” and “encoded ... (PCI) bus transaction” by giving each of these phrases its ordinary meaning in light of the construction of “PCI bus transaction.”

The district court construed “communicating ... a PCI bus transaction” based on a purported agreement about the meaning of that term, even though it has become clear that the parties had not actually agreed. In particular, the parties assigned materially different meanings to “control bits” in the construction. The Court should correct the error.

Finally, the district court misconstrued “encoded ... (PCI) bus transaction” based on its incorrect holding that ACQIS had disavowed any meaning that did not require converting parallel signals.

Although neither of these constructions formed the basis of summary judgment, clarifying them now would be in the interest of judicial economy because the issues created by those erroneous constructions are likely to become important on remand.

## **ARGUMENT**

### **I. Standard of Review**

“This court reviews summary judgment decisions under the law of the regional circuit.” *Momenta Pharm., Inc. v. Teva Pharm. USA Inc.*, 809 F.3d 610, 614–15 (Fed. Cir. 2015). The First Circuit reviews summary judgment grants *de novo*, reversing “if, after reviewing the facts and making all

inferences in favor of the non-moving party ..., the evidence on record is sufficiently open-ended to permit a rational factfinder to resolve the issue in favor of either side.” *Adamson v. Walgreens Co.*, 750 F.3d 73, 78 (1st Cir. 2014).

“[T]he ultimate issue of the proper construction of a claim should be treated as a question of law.” *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 326 (2015). The Court reviews “subsidiary factual findings on extrinsic evidence” for clear error. *Wi-LAN USA, Inc. v. Apple Inc.*, 830 F.3d 1374, 1381 (Fed. Cir. 2016) (brackets omitted).

“[T]his court applies Federal Circuit precedent when determining whether a claim construction argument has been waived.” *Lazare Kaplan Int’l, Inc. v. Photoscribe Techs., Inc.*, 628 F.3d 1359, 1376 (Fed. Cir. 2010). Issues of “waiver for failure to timely present evidence or raise an issue[] are reviewed for abuse of discretion.” *F.lli De Cecco di Filippo Fara S. Martino S.p.A. v. United States*, 216 F.3d 1027, 1031 (Fed. Cir. 2000). “A district court abuses its discretion when its decision is based on clearly erroneous findings of fact, is based on erroneous interpretations of the law, or is clearly unreasonable, arbitrary or fanciful.” *Whitserve, LLC v. Comput. Packages, Inc.*, 694 F.3d 10, 26 (Fed. Cir. 2012).

## II. Granting summary judgment based on an incorrect construction of “PCI bus transaction” was error.

The district court misinterpreted its earlier claim construction of “PCI bus transaction.” Appx6–11. ACQIS does not dispute the district court’s original construction of that term—*i.e.*, “a transaction, in accordance with the ... PCI Local Bus Specification.” Appx3. ACQIS does, however, dispute the district court’s reinterpretation of that construction at summary judgment—*i.e.*, its holding that “in accordance with the ... PCI Local Bus Specification” means communicating physical layer “control” and “parity” signals. Appx7–8. That is not what the specification requires.

That reinterpretation resulted from procedural and substantive errors. Appx6–11. The district court erred *procedurally* by refusing to consider ACQIS’s claim interpretation arguments as purportedly untimely and therefore waived. Appx9–10. It erred *substantively* by construing a “PCI bus transaction” to require physical layer “control” and “parity” signals.

The Court should hold that “a transaction, in accordance with the ... PCI Local Bus Specification” need not include physical layer signals, or in the alternative, remand with instructions for the district court to consider ACQIS’s arguments in the first instance.

### A. ACQIS’s arguments were timely.

The district court refused to consider ACQIS’s arguments regarding the reinterpretation of “PCI bus transaction” urged by EMC on the

erroneous basis that ACQIS's arguments were "untimely" and therefore waived. Appx9–10. Far from untimely, the arguments arose in a routine pre-trial dispute over interpretation of a previously issued claim construction—a dispute that *EMC*, not ACQIS, had raised unexpectedly at summary judgment. ACQIS responded immediately in its opposition with arguments consistent with positions it had taken for years. ACQIS's arguments were therefore timely and not waived. This Court should vacate the grant of summary judgment and remand for the district court to consider ACQIS's claim construction arguments in the first instance.

1. *EMC, not ACQIS, raised a new claim construction position at summary judgment.*

To start, the district court wrongly characterized the claim construction dispute as manufactured by ACQIS at summary judgment. To the contrary, *EMC* first raised the dispute at summary judgment, not ACQIS. Appx1734–1736.

Before summary judgment briefing, the parties did not debate whether "transaction" refers to physical layer signals. But that was because ACQIS had argued for years that "transaction" did not include such signals, and EMC had not clearly objected.

- a) ACQIS argued for years that a “PCI bus transaction” is defined by transaction layer data.

Throughout this litigation, ACQIS maintained that a “PCI bus transaction” is defined by the PCI Specification’s *transaction layer*, and not by its physical layer.

1. Before Judge Davis, ACQIS maintained that a “PCI bus transaction” is best described as ‘digital *command, address, and data information*, in accordance with the PCI standard’—*i.e.*, the transaction layer information—“because according to the PCI specification, that is what makes up a PCI bus transaction.” Appx484 (emphasis added); *see also* Appx484 n.4 (“the thing that determines whether the devices ... convey a PCI bus transaction, is the information—the command, address, and data information in accordance with the PCI standard”); Appx394 (the “intrinsic evidence all consistently require a ‘bus transaction’ of the PCI standard to require ‘command, address, and data information’”); Appx390–395.

2. Before the Board, ACQIS again maintained that a “PCI bus transaction” is the “command, address, and data information, in accordance with the PCI standard.” Appx679, Appx673–685.

3. Before the district court, ACQIS again argued that a “transaction, in accordance with the industry standard PCI Local Bus Specification” was the “address, command, and data information [required] in accordance with the PCI Standard.” Appx1160, Appx1170. At the *Markman* hearing, ACQIS



confirmed that “the characteristics of a PCI bus transaction” are a “PCI address,” “command code,” and the “data”—*i.e.*, the transaction layer data. Appx1540–1541 (125:7–126:2).

ACQIS argued explicitly that a “transaction” does *not* refer to physical layer signals. In its claim construction briefing, ACQIS stated that the inventor “chose to keep the information contained in the transaction layer of the PCI protocol, *but eliminate the physical layer of that protocol.*” Appx1159 (emphasis added). At the *Markman* hearing, ACQIS explained that a “PCI bus transaction” “has to involve the transaction layer,” “not the physical bus.” Appx1560 (145:22–25).

ACQIS had also consistently argued that the accused devices infringe because they communicate “PCI addresses,” “command instructions,” and “data.” Appx1544 (129:17–130:2); *see also* Appx1546 (131:23–132:1) (“the PCI drivers read, not surprisingly, PCI addresses. They read PCI command information, and then they work and exchange the data as is required by the protocol”); Appx1554 (139:9–12) (arguing that a PCI driver must understand “a PCI address ... PCI command information ... and ... data.”); Appx1555 (140:3–141:14) (detailing the address, command, and data exchanged during a “transaction”).

Accordingly, ACQIS argued consistently for years that a “PCI bus transaction” is a transaction as defined by the transaction layer of the PCI Specification, and that physical layer signals are irrelevant.

- b) EMC did not clearly object to ACQIS's manifest understanding.

At no point during the claim construction proceeding did EMC clearly object to ACQIS's repeated statements that a "PCI bus transaction" is defined only by transaction layer information. To the contrary, EMC appeared to *agree*. Compare Appx1126 (EMC arguing that a "transaction" "is an active exchange of something (e.g., an exchange of information) between two or more entities") with Appx1205 (¶ 61) (ACQIS's expert opining that "a 'transaction,' within the context of the PCI standard and the patents, is an exchange of information between interconnected computer components"). Rather than speak out about any dispute on this issue at claim construction, EMC emphasized instead that "the only issue that we believe is remaining on this point is whether or not the PCI bus transaction has to involve a PCI bus." Appx1480 (65:16–19); *see also* Appx1443 (28:19–20); Appx1382–1383. Judge Davis's decision that the claims do not require a PCI bus then was not disturbed.

Hints of EMC's eventual summary judgment position can only be divined in hindsight. For example, when discussing a different term ("control bits"), EMC noted (in a parenthetical) that those bits "control the timing of events on the PCI bus"—perhaps implying that physical layer signals may be relevant to "control bits." Appx1138. EMC made a similar drive-by at the *Markman* hearing. Appx1527 (112:18–19) (mentioning in an

aside that “[c]ontrol bits actually control the sequencing of the transaction”). But EMC never squarely confronted ACQIS’s repeated and manifest understanding that a “PCI bus transaction” is the transaction-layer information exchanged by PCI components.

It was not until summary judgment that EMC unexpectedly challenged that position. ACQIS timely responded that EMC’s reinterpretation of the district court’s construction constituted an “improper narrowing [that] is inconsistent with the Court[’s claim construction] ruling that no physical PCI Local Bus is required.” Appx3348. ACQIS’s position was consistent with what it had argued for years. It was therefore wrong to criticize ACQIS for failing to recognize, let alone preemptively respond to, EMC’s new argument before EMC ever raised it.

Importantly, the district court did not hold that ACQIS’s claim construction arguments prejudiced EMC or that ACQIS was otherwise estopped from making them. Indeed, it could not have done so because ACQIS had taken the same position for years—*i.e.*, that a “transaction” requires only transaction layer information. It was therefore timely for ACQIS to reassert its position in response to EMC’s unanticipated reinterpretation of the district court’s construction, and wrong of the district court to conclude otherwise.

2. *A claim construction dispute arising at summary judgment is timely.*

Even if ACQIS *could have* theoretically anticipated and raised EMC's claim construction dispute earlier, that possibility would still not justify a finding of waiver because ACQIS nevertheless raised the dispute *pre-trial*, and ACQIS's arguments were consistent with its positions throughout the litigation. The district court's contrary holding was an abuse of discretion because it was "based on erroneous interpretations of the law." *Whitserve*, 694 F.3d at 26.

"[A] district court may engage in claim construction during various phases of litigation, not just in a *Markman* order." *Conoco, Inc. v. Energy & Envtl. Int'l, L.C.*, 460 F.3d 1349, 1359 (Fed. Cir. 2006). That includes making claim construction rulings "on summary judgment ... rather than in the phase of the case specifically dedicated to claim construction." *Wi-LAN USA*, 830 F.3d at 1381. Moreover, a "district court may (and sometimes *must*) revisit, alter, or supplement its claim constructions ... to the extent necessary to ensure that final constructions serve their purpose of genuinely clarifying the scope of claims for the finder of fact." *In re Papst Licensing Digital Camera Patent Litig.*, 778 F.3d 1255, 1261 (Fed. Cir. 2015) (emphasis added); *see also Jack Guttman, Inc. v. Kopykake Enters., Inc.*, 302 F.3d 1352, 1361 (Fed. Cir. 2002) (a district court may "revisit[] and alter[] its interpretation of the claim terms"). "This is particularly true where

issues involved are complex, either due to the nature of the technology or because the meaning of the claims is unclear from the intrinsic evidence.” *Guttman*, 302 F.3d at 1361.

Accordingly, district courts routinely revise constructions—before or even during trial—when disputes arise. *See, e.g., Intervet Inc. v. Merial Ltd.*, 617 F.3d 1282, 1289 (Fed. Cir. 2010) (holding that the district court incorrectly interpreted its earlier construction at summary judgment); *Moba, B.V. v. Diamond Automation, Inc.*, 325 F.3d 1306, 1313 (Fed. Cir. 2003) (per curiam) (hearing a dispute over the district court’s interpretation of its earlier claim construction); *Gen. Surgical Innovations, Inc. v. Origin Medsystems, Inc.*, 250 F.3d 761, 2000 WL 959507, at \*3 (Fed. Cir. 2000) (table) (“[a]lthough neither party appeals the district court’s construction ... the parties disagree as to the interpretation of the district court’s claim construction”).

In *Intervet* (as here) the district court issued a *Markman* order construing a disputed term. 617 F.3d at 1289. And, as here, the district court granted summary judgment of non-infringement based on interpretation of that earlier construction. *Id.* The appellant disputed only the subsequent *interpretation* of that construction. *Id.* This Court agreed that the interpretation was “inconsistent with the district court’s otherwise correct [original] claim construction,” “reverse[d] the district court’s claim construction[],” “clarif[ied] the proper interpretation of the construction,”

and “remand[ed] the question of infringement for a determination consistent with the claim constructions articulated” by the Court. *Id.* at 1289–90.

The fact pattern here is similar. The district court had construed a “PCI bus transaction” as “a transaction, in accordance with the ... PCI Local Bus Specification....” Appx1703–1704. Defining that term with reference to the “PCI Local Bus Specification” left open exactly what information was “in accordance with” that Specification.

At summary judgment, EMC argued that a transaction is “in accordance with” the PCI Specification only if it includes certain physical layer signals defined in that specification. Appx1734–1736. ACQIS timely disagreed in its opposition (Appx3347–3359) and accompanying expert declaration (Appx3394–3420), explaining why a person of ordinary skill would not have understood a “transaction, in accordance with the ... PCI Local Bus Specification” to include the physical layer signals EMC identified. Appx3342, Appx3347–3359.

There was nothing unusual about this routine sequence. As in *Intervet*, a pre-trial dispute over the meaning of an earlier construction arose during summary judgment. As EMC wrote at the time, “the only dispute here ... is a pure legal issue of claim construction.” Appx1743. And “[w]hen the parties present a fundamental dispute regarding the scope of a

claim term, it is the court’s duty to resolve it.” *O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1362 (Fed. Cir. 2008).

But the district court here did not. Instead, it refused to resolve the dispute, dismissing ACQIS’s arguments as “untimely” because it believed “district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs.” Appx9–10 (citing *Function Media, L.L.C. v. Google Inc.*, 708 F.3d 1310, 1325 (Fed. Cir. 2013)). Those are errors of law.

“[L]itigants waive their right to present new claim construction disputes if they are raised for the first time *after trial*.” *Conoco*, 460 F.3d at 1359 (emphasis added); *see also Broadcom Corp. v. Qualcomm Inc.*, 543 F.3d 683, 694 (Fed. Cir. 2008) (same). Accordingly, district courts routinely hear arguments and resolve claim construction disputes that arise as late as the close of evidence. *Eli Lilly & Co. v. Aradigm Corp.*, 376 F.3d 1352, 1360 (Fed. Cir. 2004) (a party waives a claim construction issue raised for the first time “[o]nly after the presentation of all of the evidence to the jury”). (Of course, here, the dispute was *before* trial.)

Thus, for example, it made no difference in *Intervet* “that at the time of the *Markman* hearing, [appellant] did not see any” problem with the original claim construction. 617 F.3d at 1289. What mattered was that a material dispute arose about that construction *pre-trial*. Contrary to the district court’s holding here, it was not incumbent on ACQIS to have

anticipated the dispute back at the claim construction phase and to have “tee[d] up a summary judgment position based on a particular construction” that EMC had not previously advanced. Appx9–10.

The district court was also wrong as a matter of law in holding that “district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs.” Appx10. Indeed, the case the court cited for that proposition (*Function Media*) holds the opposite. In *Function Media*, this Court found *no* waiver because the claim construction dispute “was brought to the district court’s attention *during trial* and the court heard arguments from both sides.” *Function Media*, 708 F.3d at 1325 (emphasis added). Accordingly, *Function Media* does not support the district court’s conclusions that ACQIS’s arguments were untimely and that it had no obligation to hear them.

None of the other authority the district court cited supports that conclusion either. *ePlus, Inc. v. Lawson Software, Inc.* simply held “that a *post-trial* challenge” to claim construction is “inappropriate and untimely,” Appx10 (citing 700 F.3d 509, 520 (Fed. Cir. 2012)) (emphasis added), but ACQIS’s arguments were not made post-trial, but at summary judgment. Accordingly, *ePlus* does not support the district court’s conclusion either.

The district court cited *O2 Micro* for the proposition that district courts are not “required to construe *every* limitation present in a patent’s asserted claims.” Appx10 (citing 521 F.3d at 1360–62). But ACQIS’s



arguments concerned a dispositive claim construction dispute, “not an obligatory exercise in redundancy.” *O2 Micro*, 521 F.3d at 1362. As *O2 Micro* held, “[w]hen the parties present a fundamental dispute regarding the scope of a claim term, it is the court’s duty to resolve it.” *Id.*

Simply put, the district court got the law wrong. And because its waiver holding was “based on erroneous interpretations of the law,” it was an abuse of discretion. *Whitserve*, 694 F.3d at 26. Accordingly, if this Court does not reach the merits and reverse, it should at a minimum vacate the grant of summary judgment and remand to the district court to evaluate ACQIS’s claim construction arguments and uncontradicted evidence in the first instance. On remand, the district court should consider those legal arguments as well as “any appropriate recourse to extrinsic evidence concerning the usage and understanding of the term [‘PCI bus transaction’] in relevant context,” including the expert declarations ACQIS submitted. *Verve, LLC v. Crane Cams, Inc.*, 311 F.3d 1116, 1120 (Fed. Cir. 2002).

**B. The district court erred by holding that a “transaction, in accordance with” the PCI Specification must include physical layer “control” and “parity” signals.**

If the Court determines that the record on appeal is sufficiently developed, it should reach the merits and hold that a “transaction, in accordance with the ... PCI Local Bus Specification” does not include the physical layer signals on which summary judgment was based.

The parties and the district court all agreed that the claims use the phrase “PCI bus transaction” to refer to information that defines a “transaction, as defined by ... the PCI Local Bus Specification.” Appx1700. The dispute is whether a skilled artisan would have understood the term “transaction” as referring to the transaction layer information defined in that standard (as ACQIS argued) or instead as also encompassing certain physical layer signals (as EMC argued and the district court accepted). The record supports only ACQIS’s interpretation.

“[C]laim construction must begin with the words of the claims themselves.” *In re Power Integrations, Inc.*, 884 F.3d 1370, 1376 (Fed. Cir. 2018). The Court then considers the intrinsic evidence, which here includes the written description, the prosecution history, and the PCI Specification.<sup>5</sup> *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315 (Fed. Cir. 2005). Finally, “resolution of any ambiguity arising from the claims and specification may be aided by extrinsic evidence.” *Verve*, 311 F.3d at 1119–20.

Here, the evidence demonstrates that “PCI bus transaction,” as used in the claims, refers to the transaction layer information defined by the PCI Standard.

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<sup>5</sup> The PCI Specification is intrinsic evidence because it is cited on the face of at least one patent in each of the three asserted patent families. *Kumar v. Ovonic Battery Co.*, 351 F.3d 1364, 1368 (Fed. Cir. 2003) (“prior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence”).

1. *Claim language.*

Nothing in the claim language suggests that a “PCI bus transaction” includes physical layer control and parity signals. None of the asserted claims recites that a “transaction” includes such physical layer signals. Neither do any of the unasserted claims.

In contrast, several asserted claims *do* recite that the “transaction” includes *transaction layer* information, such as “address and data bits of [a] (PCI) bus transaction” or the “data bits of [a] PCI bus transaction.” ’171 patent (cl. 24) (Appx332); ’468 patent (cl. 29); (Appx372) ’119 patent (cl. 38) (Appx293); ’814 patent (cl. 31) (Appx246). The claim language therefore suggests that a “transaction” includes transaction layer information (*e.g.*, address and data bits) but not physical layer signals.

The district court’s holding that the claims do not require a PCI Local Bus also supports ACQIS. Appx1700–1704. It is undisputed that the physical layer signals on which summary judgment rests “are only used to facilitate communication over a physical PCI Local Bus.” Appx3396, Appx3403 (¶¶ 15, 38) (ACQIS’s expert declaration); *see also* Appx3398 (¶ 24) (“interface control signals are a requirement specific to communication of a transaction over a physical PCI Local Bus”). In other words, a person of skill would know that physical layer signals are only needed if a physical PCI Local Bus is. With no physical PCI Local bus required, no physical layer signals would be required either.

Given the district court’s holding that the claims include embodiments with no PCI Local Bus, it makes no sense to then construe the claims to read back useless physical layer signals. Simply put, because the claims require no PCI Local Bus, a skilled artisan would have understood that they require no physical layer signals to control a non-existent PCI Local Bus. Appx3400 (¶ 30).

## 2. *Intrinsic record*

The intrinsic record demonstrates that “PCI bus transaction” does not include physical layer control and parity signals. That record contains both (1) the patent specifications and (2) the PCI Specification.

### a) Patent specifications

The patent specifications, like the claim language, disclose embodiments that *exclude* the PCI Local Bus and therefore have no use for physical layer signals. For example, as shown in Figure 8 of the ’415 Patent, PCI components connect directly to interface controllers, or through other bus types, *without any intervening PCI Local Bus*. In the context of such embodiments, it would be illogical to read into the claimed requirement of communicating a “PCI bus transaction” any PCI *physical layer* signals.

Moreover, the specifications *also* describe embodiments where components connect to the interface controllers using a PCI Local Bus. *See, e.g.*, Appx24 (Figure 7). And in those embodiments, interface controllers use

separate hardware to capture and convey physical layer signals coming across that PCI Local Bus. *See, e.g.*, Appx43–44 (16:63-17:54).

This disclosure implies that the physical layer signals are *not* present in *all* embodiments, contrary to the district court’s construction. As described above, where an interface controller receives a “PCI bus transaction” directly from a processor or from an “other bus,” without any intervening PCI Local Bus, it would make little sense to understand the term “PCI bus transaction” as denoting physical layer signals for controlling the non-existent bus. But the district court’s construction does exactly that.

Take oral conversations. Communicating a “PCI bus transaction” is analogous to communicating a “conversation.” Embodiments that communicate the conversation from one telephone network to another (analogous to embodiments that communicate a “PCI bus transaction” from one PCI Local Bus to another) would communicate both the conversation *and* the signals necessary to control the telephone networks. But embodiments that communicate the conversation over a different physical medium would naturally not communicate signals necessary to control a telephone network, because no telephone network exists in those embodiments. Thus, if a claim term applied to both embodiments such as “telephone conversations,” it would make little sense to interpret its instruction to communicate a “telephone conversation” as requiring communicating signals necessary to control a telephone network.

The patent specifications further confirm this understanding by disclosing that, where physical layer PCI signals exist, they are processed separately from the transaction layer information. *Id.* (17:16–54) (processing the transaction layer “address and data information” by encoders 1022 and 1027 and processing physical layer signals by “control encoder & merge data path unit 1025”).

b) PCI Specification

The PCI Specification also confirms that “PCI bus transaction” does not refer to physical layer data, but to transaction layer data. It does so both by (1) defining a “transaction” by reference to the transaction layer data exchanged between components, and (2) repeatedly describing the physical layer signals as separate from the “transaction.”

*First*, the PCI Specification defines a “transaction” by reference to the transaction layer information, not physical signals. In particular, the PCI Specification defines a “transaction” as “an address phase plus one or more data phases,” with an “address phase” defined as “a single address transfer,” and a “data phase” as a “transfer state” “in which [the] data is transferred” (“plus zero or more wait states”). Appx2357–2358; Appx3396–3397 (¶¶ 17–18). The PCI specification thus defines a “transaction” in terms of the information actually transferred between the master and target components, not in terms of physical layer signals never received into the memory of the devices communicating over the bus. Appx3400 (¶ 29) (“the

interface control signals are not received in the memory of the devices communicating over the bus, thus, they are not part of the transaction”).

*Second*, the PCI Specification repeatedly describes the physical layer signals on which the district court relied as separate from the “transaction.” For example, its glossary describes various physical layer control signals as separate from the “transaction”—e.g., the DEVSEL# signals as “allow[ing] a target to claim a transaction,” and the FRAME# signal as “defining the boundary of the transaction.” Appx2355; *see also* Appx3400 (¶ 28). As such, these control signals are not part of the transaction.

The same is true of the “parity signal.” Appx3403–3404 (¶¶ 37–45). The parity bit is calculated to confirm that the *transaction layer* information was transmitted correctly—i.e., is “calculated from the address, data, command, and byte enable bits.” Appx3403 (¶ 40); *see also* Appx2332. Accordingly, “the parity bit itself provides a *transport* function and is not part of the transaction.” Appx3403 (¶ 37) (emphasis added). Thus, the PCI Specification consistently describes the parity bit as something separate from the transaction. For example, it discloses that the parity signal “provides a mechanism to determine *transaction by transaction* if the master is successful in addressing the desired target and if data transfers correctly between them.” Appx2332; *see also* Appx3403 (¶ 39). The PCI Specification describes the parity bit as “lag[ging] the corresponding address or data by one clock.” Appx2332; *see also* Appx3404 (¶ 42). “In other

words, parity is sent *after* the transaction.” Appx3404 (¶ 42) (emphasis added). Thus, a parity signal is not part of the transaction, but separate and sent only after transmission of the transaction to which it pertains to confirm correct transmission of that transaction.

### 3. *Extrinsic record*

The extrinsic evidence confirms that the ordinary meaning of a “PCI bus transaction” is the transaction layer information defining a PCI operation, and not physical layer signals. Appx3396–3400, Appx3403–3404 (¶¶ 16-31, 37–45).

Expert testimony submitted by ACQIS established that the ordinary meaning of “‘transaction,’ within the context of the PCI Standard and the patents, is an exchange of information between interconnected computer components,” and not physical layer signals. Appx1205 (¶ 61). Expert testimony establishes that a transaction would mean the message, not its messenger:

A person of ordinary skill would understand a “transaction” as the data exchanged over a connection, that is, the message communicated and not the messenger that delivers the message. A person of ordinary skill would not consider a particular physical layer, or the control signals necessary for sending information over a particular type of physical layer, to be part of the transaction. Rather, the “transaction” is the information exchange that occurs over a given physical interface, specifically in the case of the PCI Local Bus Specification, writing data to,



or reading data from a particular memory location defined by the specification.

Appx2471 (¶ 52).

Expert testimony confirms that a person of ordinary skill would have understood the PCI Specification as using the term “transaction” consistently with this ordinary meaning. Appx3397 (¶ 19) (“the PCI Local Bus Specification defines a transaction as the information communicated in the address phase and data phase;” parity signals are sent in a later phase); Appx2470 (¶ 50) (“The PCI Local Bus Specification describes the information communicated over the physical layer as a 32-bit ‘transaction.’”); Appx2505 (¶ 110) (a “transaction [as] defined by the PCI Local Bus Specification refers to the information conveyed” between the two PCI components for performing a PCI operation).

Finally, expert testimony establishes that, for many of the reasons already discussed, a skilled artisan would have understood the PCI Specification as treating the physical layer “control” and “parity” signals as separate from the “transaction.” Appx3398–3400, Appx3403–3404 (¶¶ 23–31, 37–45).

The entire record therefore establishes that “transaction” refers to the transaction layer data communicated from one PCI component to another, and not to the physical layer signals used only to facilitate that communication.

Given this understanding, a “transaction” is “in accordance with the PCI Local Bus Specification” if it includes the transaction layer information the PCI Specification requires—typically the address, data, command, and byte enables for most types of transactions. Appx2505 (¶ 110); Appx3397 (¶ 20). Whether transactions communicated by the accused systems are “in accordance with” the PCI Specification is the factual question of infringement. If factual disputes remain, a jury should be empaneled to decide that question.

The Court should “reverse the district court’s claim construction,” “clarify the proper interpretation of the construction,” and “remand the question of infringement for determination consistent with the claim constructions articulated” by the Court. *Intervet*, 617 F.3d at 1290. Because the court’s non-infringement analyses respecting the “communicating” and “encoded” limitations were based entirely on its erroneous interpretation of “PCI bus transaction,” resolution of this issue would also require it to reevaluate those analyses.

**C. The district court’s construction does not preclude infringement of the Address and Data Claims.**

Even if the district court had correctly interpreted “PCI bus transaction” to require the physical layer control and parity signals (it did not), this still would not justify summary judgment of non-infringement against the Address and Data Claims because those claims recite explicitly

that only the “address and data bits of [that] ... PCI bus transaction” are communicated.<sup>6</sup> Because the accused products indisputably transmit those recited bits, the district court erred in granting summary judgment of non-infringement with respect to those claims.

As ACQIS argued repeatedly to the district court (Appx3337–3338; Appx1178; Appx1226 ¶ 129; Appx1635–Appx1636 (220:15–221:6); Appx1393), the Address and Data Claims “state precisely what must be communicated: *only* the “address and data bits of a PCI bus transaction.” Appx3337 (emphasis added). For example, claim 31 of the ’814 patent recites that the peripheral bridge “communicate[s] *address and data bits of [a] PCI bus transaction* in serial form over said second LVDS channel.” Appx246 (cl. 31) (emphasis added). Accordingly, even if a “PCI bus transaction” were to include, as the district court held, physical layer control and parity signals, the requirement of transmitting only the “address and data bits of [a] PCI bus transaction” would clearly not require also transmitting these physical layer control and parity signals.

For purposes of summary judgment, EMC accepted that the accused products communicate all address and data bits. Appx1764 n.26. ACQIS argued that this admission foreclosed summary judgment on the Address

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<sup>6</sup> ’171 patent (cl. 24) (Appx246); ’468 patent (cl. 29) (Appx372); ’814 patent (cl. 31) (Appx246); ’119 patent (cl. 38) (Appx293).

and Data Claims because those claims only required communicating the address and data bits. Appx3337, Appx3338. The district court ignored the argument and granted summary judgment of non-infringement against those claims anyway. For this additional, independent reason, the Court should reverse the grant of summary judgment and remand for trial on infringement of at least the Address and Data Claims.

### **III. The Court should correct the district court’s constructions of “communicating” and “encoded.”**

Though the district court briefly discussed “communicating ... [a] PCI bus transaction” and “encoded ... (PCI) bus transaction,” its non-infringement analysis of each turned entirely on its interpretation of “PCI bus transaction.” Specifically, the district court held that, because the accused products lack a “PCI bus transaction,” they can neither “communicate a PCI bus transaction” nor “encode[] ... [a] (PCI) bus transaction” regardless of what “communicating” or “encoded” mean. Appx3, Appx11–13.

For example, the district court’s only analysis of the “communicating” phrase was to note that it had “already concluded that the claims are limited by the Specification” and that summary judgment was appropriate “for the reasons described above.” Appx12–13. Its analysis of the “encoded” term also turned only on its construction of “PCI bus transaction”: it held that “ACQIS asserts that EMC’s products modify *some data* from parallel to

serial form prior to communicating or transacting that data, but ACQIS does not actually identify a *PCI bus transaction* that is converted from parallel to serial form and communicated by the accused products.” Appx12. Accordingly, the Court can reverse the entire summary judgment order by correcting or vacating the construction of “PCI bus transaction” alone.

Nevertheless, as this Court has explained, “[i]n the interest of judicial economy, we have the discretion to review a non-dispositive claim construction if we believe that the construction may become important on remand.” *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1376 (Fed. Cir. 2014); *see also Lexington Luminance LLC v. Amazon.com Inc.*, 601 F. App’x 963, 970 (Fed. Cir. 2015). The Court has exercised that discretion where, for example, the disputed claim term appears in claims for which the court was vacating summary judgment of non-infringement. *Interval Licensing*, 766 F.3d at 1376 (“Because we are vacating the judgment of non-infringement as to claims 15–18 of the ’652 patent, and because those claims include the [disputed] term ‘instructions,’ we take this opportunity to address the claim construction of that term.”).

The Court should exercise its discretion here and hold that “communicating ... [a] PCI bus transaction” and “encoded ... (PCI) bus transaction” carry their ordinary meanings, in view of the ultimate construction of “PCI bus transaction.” The ordinary meaning is simply to convey code representing a PCI bus transaction, and ACQIS will prove at

trial that EMC's accused systems do just that. Moreover, revising those constructions is necessary because the district court (1) wrongly construed the "communicating" phrase pursuant to an apparent but illusory agreement between the parties, and (2) wrongly construed the "encoded" phrase based on an erroneous finding of prosecution disclaimer.

**A. "Communicating ... [a] PCI bus transaction" should be given its ordinary meaning.**

As ACQIS argued below (Appx1177; Appx1711), "communicating ... [a] PCI bus transaction" carries its ordinary meaning in light of the construction of "PCI bus transaction." At the *Markman* hearing, ACQIS consented to EMC's proposal that this meaning was "communicating a PCI bus transaction, including all address, data, and control bits." Appx1711–1712.

Unfortunately, as now apparent, the parties assigned materially different meanings to the term "control bits." ACQIS made it clear that it understood that term as it always had—*i.e.*, the transaction layer's command and byte enable bits (which the accused products communicate)—whereas EMC claimed at summary judgment that the phrase referred to the physical layer's interface control signals (which EMC says the accused products do not communicate). Appx1725.

Because the court's construction of "communicating ... [a] PCI bus transaction" was adopted based on EMC's version of the agreement—a

version that was inconsistent with what ACQIS made clear it was agreeing to, it should be vacated. The Court should then hold that the phrase carries its ordinary meaning in light of the Court's resolution of the "PCI bus transaction" phrase, or alternatively, remand for the district court to consider the issue in the first instance.

Relief is appropriate here because the disagreement over the meaning of "control bits" is genuine and timely. When ACQIS agreed to construe "communicating ... [a] PCI bus transaction" as communicating "all the address, data, and *control bits*," it made explicit that it understood "control bits" to mean command information:

THE COURT: If I took their definition and deleted like the last six words, you'd be okay with that?

MR. BROGAN: ... I think that's right. Because I think you would communicate, in a PCI bus transaction you do communicate the address, **you do communicate a command that tells you what you have to do** and then you send the data. So I think that's right. That's all right.

...

And if you have no PCI address and no **command** that tells you what transaction is going to take place, you can't say that's a PCI bus transaction.

...

If you only have some of the bits and you don't have a **command**, then you wouldn't be able to carry out a PCI bus transaction.

Appx1642–1643 (227:25–228:15) (emphasis added).

ACQIS's understanding was no surprise because the phrase "control bits" is used in the art to refer to the transaction layer's command and byte enable bits (Appx2473 (¶ 57); Appx3419–3420 (¶ 83)), and both ACQIS and had used it that way throughout the litigation.

For example, at the IPR hearing, ACQIS represented that "control bits" describe the PCI *command*. See, e.g., Appx1034–1035 (describing "address and the *control bits*" indicating the type of *command*, such as "interrupt acknowledge") (emphasis added). To remove any confusion, ACQIS told the district court explicitly at the *Markman* hearing that it had used the term "control bits" in the IPR hearing to "refer[] to the command." Appx1641 (226:12–15).

ACQIS's expert (Dr. Gafford) had also used the term "control bits" in his reports to refer to command bits and byte enables. E.g., Appx2601 (¶ 243) (expert report). And at his deposition, he too clarified that that he used "control bits" to refer to the command and byte enables. Appx2158 (457:8-10) ("Q: And by control bits, you're referring to command and byte enables; correct? A: That's right.").

Throughout the *Markman* hearing, ACQIS also used "control bits" to refer to the transaction layer's command information and byte enables. E.g., Appx1629 (214:14–16) ("a PCI bus transaction that's defined by the standard. You know the three portions, address, data and control. So those things that tell you what it is that you're going to do when you exchange the



information.”); Appx1641 (226:12–15) (“That includes data, that includes address except for interrupt acknowledge, and that includes the control bits.’ He says every time. He’s referring to the command.”).

Even *EMC* used “control bits” to refer to command and byte enable information. For example, at the *Markman* hearing, EMC argued that ACQIS’s expert had agreed “with no ambiguity” that “*control bits*” must be communicated. Appx1533 (118:10–119:23) (emphasis added). To show this agreement, EMC pointed to deposition testimony where ACQIS’s expert had agreed that “*command information and byte enable[s]*” must be communicated. Appx1533 (118:10–119:23) (emphasis added). EMC thus equated “control bits” with “command information and byte enables,” even at the *Markman* hearing.

EMC never disputed ACQIS’s statements equating “control bits” with command and byte enables. Just the opposite. When ACQIS agreed that “communicating ... [a] PCI bus transaction” requires communicating “control bits,” it stated expressly that this was “all right” only if “control bits” referred to “command bits.” Appx1643 (228:2–15). Rather than object, EMC took a short recess, and upon returning, simply declared that “we’re comfortable proceeding with the construction to which [ACQIS’s counsel] agreed,” thus acquiescing in ACQIS’s position. Appx1645 (230:10–13).

At summary judgment, EMC unexpectedly revealed that it interpreted “control bits” to mean *physical layer* control signals. Appx1765.

When ACQIS reiterated that “control bits” refers to command and byte enables (Appx3338, Appx3373–3376; Appx3417–3420 (¶¶ 75–83)), EMC responded with indignance to what it called “the fiction that the Court actually construed ‘control bits’ to mean command and byte enable bits.” Appx3457.

It was not a fiction. It was what ACQIS explicitly had agreed to. And given ACQIS’s other arguments throughout the litigation and the *Markman* hearing—*i.e.*, that a “PCI bus transaction” “has to involve the transaction layer” and “not the physical bus” (Appx1560 (145:22–25); *see also supra* § I.A.1)—it would have been impossible to reasonably interpret ACQIS’s agreement on “control bits” as an agreement that physical layer signals are required.

In any event, it has become clear that the district court adopted a materially ambiguous construction of “communicating ... [a] PCI bus transaction,” based on a purported agreement between the parties that in fact never existed. To avoid further confusion, the Court should either vacate the construction and hold that the phrase carries its ordinary meaning in light of “PCI bus transaction,” as ultimately construed, or, in the alternative, remand for the district court to construe the phrase in the first instance.

**B. ACQIS made no disavowal requiring an “encoded ... (PCI) bus transaction” to be serialized from parallel signals.**

The Court should vacate the erroneous construction of “encoded ... (PCI) bus transaction.” Appx1704–1711. Judge Davis construed “encoded ... PCI bus transaction” to simply mean “code representing a PCI bus transaction.” Appx508. The district court revised that construction to a “transaction that has been serialized *from a parallel form*,” based on EMC’s false narrative that ACQIS had “defeat[ed] the IPRs” by disavowing broader claim scope. Appx1704–1711; Appx1137. But “for prosecution disclaimer to attach, [Federal Circuit] precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable.” *Omega Eng’g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325–26 (Fed. Cir. 2003) (noting also that “[a]mbiguous language cannot support disavowal”). That is not the case here.

At the IPR, ACQIS never distinguished the prior art based on conversion of parallel signals. The district court was led astray by EMC’s false narrative, cherry-picked citations to the IPR hearing, and the court’s own misunderstanding that “serialization” (*i.e.*, formatting data for serial transmission) requires the data to start as *parallel* signals rather than, for example, simply data in memory. The Court should therefore hold that

ACQIS made no disavowal, vacate the district court’s order based on that finding, and hold that Judge Davis’s original construction controls.

1. *ACQIS never argued that “encoded” requires serializing data from parallel signals.*

ACQIS did not defeat the IPRs, as EMC contends, by arguing that “encoded” requires serializing data from parallel signals. Indeed, ACQIS had never distinguished the prior art based on the “encoded” limitation at all, let alone by arguing that the limitation required converting parallel signals. Just the opposite. ACQIS had formally asked for a broader construction and then *conceded* that the prior art met the encoded limitation based on that broader construction, without converting parallel signals.

*First*, ACQIS had formally asked the Board for a construction of “encoded” that did *not* require serializing parallel signals. Appx798–799. Specifically, ACQIS requested a construction that included any reversible operation that “(1) turns a signal into bits, (2) groups bits into a specified size block, or (3) orders bits onto one or more serial transmission lines.” Appx799. At the very least, the second two options have no relationship to parallel signals. Accordingly, ACQIS requested a construction of “encoded ... (PCI) bus transaction” that did not require the transaction to have been encoded from parallel signals. This alone should be sufficient to reverse the finding of waiver.

*Second*, ACQIS did not even attempt to defend the IPR based on the “encoded” limitation, let alone on the basis that “encoded” requires converting parallel signals. Just the opposite. ACQIS *conceded* that the prior art *satisfied* the “encoding” limitation *without encoding parallel signals*. Appx817. Specifically, ACQIS conceded that the prior art’s “8b/9b line encoding”—which fits ACQIS’s second option—satisfied the “encoded” limitation. Appx817. EMC itself characterizes that type of encoding as “not parallel-to-serial conversion” (Appx1782 (¶ 57)).

*Third*, both EMC and the Board accepted ACQIS’s concession. Appx972–973, Appx1099–1100, Appx1104 n.4. The Board therefore held (and both parties agreed) that the prior art *satisfied* the “encoded” limitation *without* serializing parallel signals. Appx1099–1100, Appx1104 n.4.

In other words, the “encoded” limitation played no role whatsoever in defeating the IPRs, but EMC told the district court the opposite. EMC argued that “encoded” “require[s] the parallel data to be serialized” because:

ACQIS made that representation in the IPRs when it considered it necessary to do so to differentiate the prior art in order to save its patents. Having done so—and having obtained the benefit of doing so by defeating the IPRs—ACQIS is bound (and the claims are limited) by those statements.

Appx1137. That is false.

2. *The statements the district court relied on do not constitute disavowal.*

To support that false narrative, EMC cited quotations from the IPR hearing suggesting that some dispute existed regarding the “encoded” term and whether it required serializing parallel signals. Appx1705–1711. In adopting that narrative, the district court (1) failed to consider the totality of the prosecution history, (2) considered certain quotations out of context and not others, and (3) mistakenly conflated “serialization”—*i.e.*, formatting for serial transmission (Appx1221 (¶ 111)—with converting the data “from a parallel form” rather than, for example, from data in memory.

*First*, the district court failed to consider the quotations in the context of the full prosecution history. The standard for finding prosecution disclaimer is “exacting,” *Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016), and must be informed by “the ‘totality of the prosecution history.’” *Comput. Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1379 (Fed. Cir. 2008). “To find disavowal, [courts] must find that the specification is “both so clear as to show reasonable clarity and deliberateness, and so unmistakable as to be unambiguous evidence of disclaimer.” *Openwave Sys., Inc. v. Apple Inc.*, 808 F.3d 509, 513 (Fed. Cir. 2015).

The prosecution history here includes ACQIS’s formal request to construe “encoded” without encoding parallel signals *and* ACQIS’s accepted

concession that the prior art teaches “encod[ing]” without that feature. That context alone renders it near impossible to find anything ACQIS may have said at the IPR hearing as having distinguished its claims from the prior art based on serializing parallel signals, let alone having done so clearly and unambiguously.

*Second*, the district court cited instances in which ACQIS had purportedly “reiterated the importance of parallel-to-serial conversion” (Appx1706–1708), but each was taken out of context. For example, the district court observed that counsel for ACQIS had purportedly explained that “[t]he whole point [of ACQIS’s invention] is you ... start with the PCI address that’s in the parallel slow form, serialize it and then take it back to the PCI form at the end.” Appx1706 (quoting Appx1028–1029).

Read in context, however, ACQIS was plainly not attempting to distinguish the prior art based on parallel-to-serial conversion, but based on the wholly unrelated issue of using *virtual* rather than *physical* addressing. Appx1026–1029 (29:22–32:4). The Board had asked “[w]hy do you have to have a physical address to start with,” (Appx1028 (31:11–12)), and ACQIS’s counsel responded that “[t]he whole point is that ... [y]ou start with the [*physical*] PCI address.” (Appx1028–1029). Read in this context, ACQIS was clearly not attempting to distinguish the prior art based on parallel-to-serial conversion.

*Third*, the district court misunderstood many of the quotations it cited because it conflated “serialized”—*i.e.*, formatted for serial transmission (Appx1221 (¶ 111))—with a supposed requirement that the data start as parallel signals. For example, the district court cited ACQIS’s representations that a “key to the invention was to serialize the otherwise parallel PCI bus transactions to increase communication speeds.” Appx1705–1708. But those representations imply only that ACQIS’s invention communicates PCI bus transactions in serial form, not that the invention first converts the transactions from parallel signals.

The district court’s apparent mistake was to conflate “serialized” with conversion “from a parallel form,” but those are two separate concepts. A “serialized” PCI bus transaction is one formatted for serial transmission. The serialized data could certainly start as parallel signals (*e.g.*, those from a PCI Local Bus). But a “serialized” transaction can also be created from data in memory. Appx1221 (¶ 111) (“Serialization ... also refers to operations where *a data object* is converted into a stream of bits in order to store or transmit that data”). In that case, “serialized” transaction would not be converted from parallel signals. Appx1221 (¶ 111). Consequently, ACQIS’s statements that the invention transmits “serialized” PCI bus transactions does not imply that the transactions started as parallel signals.

For the reasons stated above, none of ACQIS’s IPR statements about the importance of serialization represent a clear and unmistakable



disclaimer that the claims require parallel-to-serial conversion. Moreover, other record statements make clear on the totality of the record that the claims do not require serializing parallel signals. Accordingly, because ACQIS made no such disclaimer, the Court should vacate the district court's revised claim construction order and hold that Judge Davis's original construction continues to control.

As noted above, the claim construction regarding serialization of parallel signals is non-dispositive because (1) the district court did not rely on it to grant summary judgment (Appx11–12), and (2) ACQIS presented an alternative infringement theory under this construction.<sup>7</sup> Nevertheless, in the interests of judicial economy, the Court should reach the issue now rather than waiting to correct the error after a jury trial.

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<sup>7</sup> Because the district court's construction of "encoded" relied on characterizing serialization from memory as "parallel-to-serial" conversion, ACQIS argued at summary judgment that the accused systems transmit "encoded" transactions at least because the transactions are serialized from memory. Appx3363; Appx3409–3410 (¶ 63).

## CONCLUSION

The Court should reverse the district court’s grant of summary judgment, hold that (1) a “PCI bus transaction” does not require any physical layer signals, including interface control and parity bits, and (2) “communicating ... [a] PCI bus transaction” carries its ordinary meaning, and vacate the district court’s construction of “encoded ... (PCI) bus transaction.”

Respectfully submitted,

/s/Anne M. Voigts

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August 16, 2021

## CERTIFICATE OF COMPLIANCE

Pursuant to Federal Rule of Appellate Procedure 32(g), the undersigned counsel for Appellee certifies that this brief:

(i) complies with the type-volume limitation of Federal Circuit Rule 32(b)(1) because it contains 13,660 words, including footnotes and excluding the parts of the brief exempted by Federal Circuit Rule 32(b)(2) and Federal Rule of Appellate Procedure 32(f); and

(ii) complies with the typeface and style requirements of Federal Rules of Appellate Procedure 32(a)(5) and 32(a)(6) because this document has been prepared using Microsoft Office Word 365 ProPlus and is set in Century Schoolbook font in a size equivalent to 14 points or larger.

Dated: August 16, 2021

/s/ Anne M. Voigts  
Anne M. Voigts

*Counsel for Plaintiff-Appellant  
ACQIS, LLC*

## **ADDENDUM**

UNITED STATES DISTRICT COURT  
DISTRICT OF MASSACHUSETTS

ACQIS, LLC,

Plaintiff,

v.

EMC CORPORATION,

Defendant.

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Civil Action No. 14-cv-13560-ADB

**MEMORANDUM AND ORDER ON EMC’S MOTION FOR SUMMARY JUDGMENT**

BURROUGHS, D.J.

Plaintiff ACQIS, LLC (“ACQIS”) brings claims against Defendant EMC Corporation (“EMC”) alleging infringement of several patents relating to modular computing systems. Among the twenty-four motions currently pending before the Court is EMC’s motion for summary judgment of non-infringement of eight patents. [ECF No. 502]. EMC argues that critical elements of the asserted claims are not present in its accused products and that, as a result, there has been no infringement. ACQIS opposes the motion. For the reasons stated below, EMC’s motion for summary judgment of non-infringement, [ECF No. 502], is GRANTED, and the remaining pending motions, [ECF Nos. 237, 354, 356, 413, 418, 419, 450, 452, 455, 461, 464, 466, 494, 498, 506, 509, 511, 513, 515, 518, 521, 524, 527], are DENIED as moot.

**I. BACKGROUND**

**A. The Patents-in-Suit**

ACQIS alleges that certain of EMC’s computer storage products infringe the following eleven claims of eight patents owned by ACQIS: U.S. Patent No. 7,363,416, claim 60; U.S.

Patent No. 7,818,487, claims 38 and 49; U.S. Patent No. 8,041,873, claims 9, 29, and 61; U.S. Patent No. RE41,294, claim 44; U.S. Patent No. RE42,814, claim 31; U.S. Patent No. RE43,119, claim 39; U.S. Patent No. RE43,171, claim 24; and U.S. Patent No. RE44,468, claim 29. [ECF No. 504 ¶ 1].

The EMC products at issue are modular computer systems, and the patents-in-suit each describe and claim one or more computer modules that can be removed from one console and placed in another. [ECF No. 102 at 1]. The console (e.g., keyboard, mouse, display, and disk drive) is a platform into which a module containing the core computing hardware (e.g., central processing unit (“CPU”), memory, input/output, and hard drive) can be inserted in order to form a complete personal computer. [ECF No. 71 at 2].

## **B. Procedural Background**

On September 9, 2013, ACQIS filed its initial complaint against EMC in the United States District Court for the Eastern District of Texas. Complaint, ACQIS LLC v. EMC Corp., No. 13-cv-00639 (E.D. Tex. Sept. 9, 2013), Dkt. No. 1. On December 6, 2013, EMC moved to transfer the action to the District of Massachusetts pursuant to 28 U.S.C. § 1404(a). Motion to Change Venue, ACQIS LLC v. EMC Corp., No. 6:13-cv-00639 (E.D. Tex. Dec. 6, 2013), Dkt. No. 21. On April 30, 2014, before ruling on the motion to transfer, the court consolidated the action against EMC with three related lawsuits brought by ACQIS against other defendants in the Eastern District of Texas. Order of Consolidation, ACQIS LLC v. EMC Corp., No. 6:13-cv-00639 (E.D. Tex. Apr. 30, 2014), Dkt. No. 38. On September 10, 2014, Judge Leonard Davis conditionally granted EMC’s motion to transfer the action to the District of Massachusetts, retaining jurisdiction over EMC through the claim construction process and noting that the transfer would become effective upon the issuance of his claim construction opinion. [ECF No.

44]. On February 12, 2015, Judge Davis held a Markman hearing concerning the disputed claim terms. [ECF No. 71 at 1]. On April 13, 2015, he issued a claim construction opinion and an order transferring the case against EMC to this Court. [ECF Nos. 71, 72].

On April 27, 2015, EMC filed a motion to stay the case pending *inter partes* review (“IPR”) of two of the patents-in-suit. [ECF No. 80]. IPR is an expedited procedure for challenging the validity of a patent before the United States Patent and Trademark Office and its Patent Trial and Appeal Board (“PTAB”). [ECF No. 102 at 4]; see 35 U.S.C. §§ 311–19. On June 10, 2015, the Court stayed the case in its entirety until a decision issued in the IPRs. [ECF No. 102 at 2]. On March 8, 2016, the PTAB issued final written decisions finding that EMC had not proven that the challenged claims were unpatentable. [ECF No. 140 at 1]. On August 10, 2016, this Court lifted its stay. [Id.].

On July 27 and July 28, 2017, this Court held a second Markman hearing and issued a Memorandum and Order ruling on disputed issues of claim construction. [ECF No. 389]. Three terms or phrases were construed for purposes of this litigation (either by the Court or by stipulation between the parties) as follows:

Term	Court’s Construction
“Peripheral Component Interconnect (PCI) bus transaction”	“a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.”
“Encoded . . . serial bit stream of Peripheral Component Interconnect (PCI) bus transaction and related terms”	“a PCI bus transaction that has been serialized from a parallel form”
“communicating . . . PCI bus transaction.”	“communicating a PCI bus transaction, including all address, data, and control bits”

On July 19, 2018, EMC filed the pending motion for summary judgment on non-infringement. [ECF No. 502]. On August 22, 2018, ACQIS filed its opposition, [ECF No. 574], and on September 21, 2018, EMC filed its reply, [ECF No. 626].

## II. LEGAL STANDARD

Summary judgment is appropriate where the moving party can show that “there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law.” Fed. R. Civ. P. 56(a). “[A]n issue is ‘genuine’ if it ‘may reasonably be resolved in favor of either party.’” Robinson v. Cook, 863 F. Supp. 2d 49, 60 (D. Mass. 2012) (alteration in original) (quoting Vineberg v. Bissonnette, 548 F.3d 50, 56 (1st Cir. 2008)). “A fact is material if its resolution might affect the outcome of the case under the controlling law.” Cochran v. Quest Software, Inc., 328 F.3d 1, 6 (1st Cir. 2003). Thus, “[a] genuine issue exists as to such a fact if there is evidence from which a reasonable trier could decide the fact either way.” Id. By invoking summary judgment, “the moving party in effect declares that the evidence is insufficient to support the nonmoving party’s case.” United States v. Plat 20, Lot 17, Great Harbor Neck, New Shoreham, R.I., 960 F.2d 200, 204 (1st Cir. 1992) (citing Celotex Corp. v. Catrett, 477 U.S. 317, 325 (1986)).

“To succeed in showing that there is no genuine dispute of material fact, the moving party must . . . ‘affirmatively produce evidence that negates an essential element of the non-moving party’s claim,’ or, using ‘evidentiary materials already on file . . . demonstrate that the non-moving party will be unable to carry its burden of persuasion at trial.’” Ocasio-Hernández v. Fortuño-Burset, 777 F.3d 1, 4–5 (1st Cir. 2015) (quoting Carmona v. Toledo, 215 F.3d 124, 132 (1st Cir. 2000)). Conversely, “[t]o defeat a properly supported motion for summary judgment, the nonmoving party must establish a trial-worthy issue by



presenting enough competent evidence to enable a finding favorable to the nonmoving party.” ATC Realty, LLC v. Town of Kingston, N.H., 303 F.3d 91, 94 (1st Cir. 2002) (quoting LeBlanc v. Great Am. Ins. Co., 6 F.3d 836, 842 (1st Cir. 1993)). That is, the nonmoving party must set forth specific, material evidence showing that there is a genuine disagreement as to some material fact. Plat 20, Lot 17, Great Harbor Neck, 960 F.2d at 204 (citing Anderson v. Liberty Lobby, Inc., 477 U.S. 242, 247–48 (1986)).

In reviewing the record, the Court “must take the evidence in the light most flattering to the party opposing summary judgment, indulging all reasonable inferences in that party’s favor.” Cochran, 328 F.3d at 6. The First Circuit has noted that this review “is favorable to the nonmoving party, but it does not give him a free pass to trial.” Hannon v. Beard, 645 F.3d 45, 48 (1st Cir. 2011). “The factual conflicts upon which he relies must be both genuine and material[,]” Gomez v. Stop & Shop Supermarket Co., 670 F.3d 395, 397 (1st Cir. 2012), and the Court may discount “conclusory allegations, improbable inferences, and unsupported speculation.” Cochran, 328 F.3d at 6 (quoting Medina-Munoz v. R.J. Reynolds Tobacco Co., 896 F.2d 5, 8 (1st Cir. 1990)).

Patent infringement analysis involves two steps: (1) the threshold construction of the meaning and scope of the asserted claim, followed by (2) a determination of whether the accused product infringes the properly construed claim. Athletic Alts., Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1578 (Fed. Cir. 1996). “To support a summary judgment of noninfringement it must be shown that, on the correct claim construction, no reasonable jury could have found infringement on the undisputed facts or when all reasonable factual inferences are drawn in favor of the patentee.” Netword, LLC v. Centraal Corp., 242 F.3d 1347, 1353 (Fed. Cir. 2001). “Literal infringement requires that every limitation of the patent claim be found in the accused device.”

Durel Corp. v. Osram Sylvania, Inc., 256 F.3d 1298, 1303 (Fed. Cir. 2001) (quoting Gen. Mills, Inc. v. Hunt-Wesson, Inc., 103 F.3d 978, 981 (Fed. Cir. 1997)).<sup>1</sup> “If no reasonable jury could possibly find that an accused product satisfies every claim limitation of the asserted claims . . . then summary judgment of noninfringement must be granted.” EveryScape, Inc. v. Adobe Sys., Inc., 8 F. Supp. 3d 38, 45 (D. Mass. 2014).

### III. DISCUSSION

This Court, together with Judge Davis, has fulfilled the first part of the infringement analysis through the claim construction process. The Court must now determine whether, under the construction for each claim term, EMC’s accused devices fall within the scope of those claims.

EMC argues that its products do not infringe because, pursuant to this Court’s construction of the relevant terms, every limitation set forth in the claims cannot be found in the accused devices. [ECF No. 503 at 29]. Specifically, EMC avers that the accused devices do not include (1) a PCI bus transaction in accordance with the PCI Local Bus Specification, (2) serialization of that transaction from parallel form, and (3) communication of all bits of that transaction over a serial channel. [Id.]. ACQIS contends that EMC misinterprets this Court’s construction of the relevant claim terms and, as a result, identifies limitations that are not present in the claims. [ECF No. 560-15 at 6].

#### A. Compliance with the PCI Local Bus Specification

EMC’s primary argument is that ACQIS’s claims require compliance with the PCI Local Bus Specification (the “Specification”) in its entirety, and, as the accused products do not

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<sup>1</sup> ACQIS has not alleged infringement under the doctrine of equivalents. [ECF No. 560-16 ¶ 1 (“ACQIS does not presently assert infringement under the doctrine of equivalents . . . .”)]; ECF No. 503 at 29]. See generally [ECF No. 560-15].

comply with the Specification, there is no infringement. [ECF No. 503 at 20, 30]. ACQIS responds that its claims require compliance only with the aspects of the Specification that are relevant to its products. [ECF No. 560-15 at 20].

“To establish literal infringement, ‘every limitation set forth in a claim must be found in an accused product, exactly.’ Thus, ‘if any claim limitation is absent from the accused device, there is no literal infringement as a matter of law.’” Becton, Dickinson and Co. v. Tyco Healthcare Grp., LP, 616 F.3d 1249, 1253 (Fed. Cir. 2010) (internal citations and alterations omitted) (first quoting Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1575 (Fed. Cir. 1995), then quoting Amgen Inc. v. F. Hoffman–La Roche, Ltd., 580 F.3d 1340, 1374 (Fed. Cir. 2009)).

The crux of this dispute is the interpretation of this Court’s construction of the claim term “Peripheral Component Interconnect (PCI) bus transaction.” Prior to the Markman hearing, the parties agreed to include a reference to the relevant industry standard, the Specification, in the construction. [ECF No. 389 at 6; ECF No. 192-1 at 1 (joint claim construction brief, with both parties’ proposed constructions for “PCI bus transaction” including a reference to “the PCI standard” or Specification)]. During the hearing, the parties further agreed on the inclusion of the word “transaction” in the claim construction. [ECF No. 350 at 27 (July 27 Tr. at 27:9–28:20); ECF No. 389 at 6–7]. The remaining dispute was whether the term required the presence of a PCI bus. The Court declined to read the presence of a PCI bus on the peripheral side into the claim language and construed “PCI bus transaction” to mean “a transaction, in accordance with the industry standard PCI Local Bus Specification, for communication with an interconnected peripheral component.” [ECF No. 389 at 9–10].

EMC contends that, under this claim construction, each of the asserted claims requires a PCI bus transaction in accordance with every element of the Specification, including an address phase followed by one or more data phases as well as control signals and parity signals. [ECF No. 503 at 29–30]. As EMC’s products do not contain these limitations, EMC argues that there is no infringement. [*Id.*].

ACQIS does not dispute that EMC’s products do not include these features. [ECF No. 560-16 ¶¶ 13, 14 (ACQIS response to paragraphs 27 and 28 of EMC’s statement of facts, disputing EMC’s inclusive definition of signals without disputing that EMC’s products do not communicate those signals through transactions)]. Instead, ACQIS argues that these features are not limitations set forth in their claims and are therefore irrelevant to a non-infringement analysis. [ECF No. 560-15 at 17]. ACQIS first reasons that this Court’s refusal to construe a PCI bus transaction as requiring a physical bus necessarily modified the Specification to excise any elements pertaining to a physical bus, such as interface control signals, phase timing, parity signals, and bit-for-bit identical command encodings. [*Id.* at 20–21]. Next, ACQIS contends that the elements noted above apply only to the methodology used to convey the PCI bus transaction and are therefore outside the scope of the PCI bus transaction itself. [*Id.* at 22]. Finally, ACQIS asserts that the Specification defines a PCI bus transaction as an “address transfer plus one or more data transfers” and any additional elements are merely part of one embodiment of the Specification. [*Id.* at 26–27].

All of ACQIS’s arguments are attempts to skirt the claim construction set forth by Judge Davis and this Court. During claim construction before Judge Davis, the parties agreed to construe the term “PCI bus transaction” according to the Specification. [ECF No. 350 at 27:9–28:20; ECF No. 189 at 19]. Judge Davis noted that “a PCI bus transaction must include all

information required by the PCI standard.” [ECF No. 71 at 10]. Subsequently, in connection with this Court’s Markman proceeding, the parties once again agreed to construe the term “PCI bus transaction” according to the Specification. [ECF No. 192-1 at 1]. Although ACQIS argued strenuously and successfully that a PCI bus was not required in a PCI bus transaction, ACQIS never sought to disavow the elements of the Specification pertaining to a physical bus. See [ECF No. 389 at 15 (discussing required elements of PCI bus transaction in context of Specification and requiring aspects of PCI bus to be present in a transaction (e.g., parallel communications) even though PCI bus itself was not required); id. at 13 (“And so the claims don’t require a bus. They require a PCI transaction to take place. *You are looking at the standard the whole time.*” (emphasis added) (quoting ECF No. 189-21 at 47))].

Similarly, ACQIS never attempted to parse the Specification in order to differentiate the elements that describe the methodology of the PCI bus transaction from those that describe the substance of the transaction. See [ECF No. 189 at 16 (ACQIS’s responsive claim construction brief, stating “the claims do not require a PCI bus. They require a transaction defined by the PCI Standard (i.e., memory read, memory write, I/O read, I/O write, etc.) to take place.”)]. Nor did ACQIS contend that the Specification’s relevance was limited to its definition of transaction as “address transfer plus one or more data transfers.” Only now, at summary judgment, does ACQIS seek to disavow the parts of the Specification unfavorable to its infringement claims. Put simply, ACQIS is attempting to reopen claim construction. Despite not asking Judge Davis or this Court to construe “PCI Local Bus Specification,” ACQIS is now arguing that the Specification is less specific than it is.

As an initial matter, ACQIS’s attempt to reduce the import of the Specification is untimely. If ACQIS wanted to tee up a summary judgment position based on a particular

construction, “it could (and should) have sought a construction to that effect.” ePlus, Inc. v. Lawson Software, Inc., 700 F.3d 509, 520 (Fed. Cir. 2012) (concluding that a post-trial challenge to the sufficiency of the evidence of infringement was an inappropriate and untimely attempt to give a narrow definition to “determining”); Function Media, L.L.C. v. Google Inc., 708 F.3d 1310, 1325 (Fed. Cir. 2013) (concluding that district courts are not obligated to rule on claim construction arguments presented for the first time in summary judgment briefs). Although the Court has a duty to resolve fundamental disputes about claim scope, O2 Micro Int’l v. Beyond Innovation Tech. Co., 521 F.3d 1351, 1360 (Fed. Cir. 2008), it is “not (and should not be) required to construe every limitation present in a patent’s asserted claims,” id. at 1362. ACQIS had ample opportunity to argue for a modified definition of the Specification during either court’s claim construction proceedings, but chose not to do so. Judge Davis construed a PCI transaction as “information, in accordance with the PCI standard.” [ECF No. 71 at 10]. Then, in connection with this Court’s claim construction, ACQIS agreed with EMC to use the relevant industry standard, the Specification. [ECF No. 189 at 19; ECF No. 192-1 at 1; ECF No. 389 at 7]. There is no need to now construe a readily understandable term that ACQIS itself thought clear when offering proposed constructions of related terms and the Court will not do so.

“Where, as here, the parties do not dispute any relevant facts regarding the accused product but disagree over which of two possible meanings of [a term] is the proper one, the question of literal infringement collapses to one of claim construction and is thus amenable to summary judgment.” Athletic Alts., 73 F.3d at 1578. The Court rejects ACQIS’s proffered modification of the claim term “PCI bus transaction” to narrow the application and meaning of the Specification. Accordingly, because the accused products do not contain the limitations set forth in the asserted claims, which recite a PCI bus transaction with reference to the

Specification, the Court concludes that there is no infringement and summary judgment is appropriate. See Durel, 256 F.3d at 1303.

Given the Court's entry of summary judgment on EMC's first theory of non-infringement, the Court will only briefly address each of EMC's remaining theories, which further support the entry of summary judgment for EMC.

#### **B. Serialization of a Parallel PCI Bus Transaction**

EMC next argues that ACQIS's claims require the serialization of a PCI bus transaction from parallel form. [ECF No. 503 at 44]. According to EMC, the accused products never create or communicate a PCI bus transaction in parallel form, let alone a PCI bus transaction that is converted from parallel to serial form. [Id.]. ACQIS responds that the accused products do serialize data from parallel form, as evidenced by the presence of parallel-to-serial converters in the products. [ECF No. 560-15 at 15, 43].

As discussed supra, Section III.A, the Court construed a PCI bus transaction to mean "a transaction . . . for communication" that incorporates the requirements set forth in the Specification, see [ECF No. 389 at 10]. In addition, the Court construed the term "encoded . . . serial bit stream of [PCI] bus transaction and related terms" to mean "a PCI bus transaction that has been serialized from a parallel form." [Id. at 16–17]. Despite this, ACQIS now suggests that information that is serialized from a parallel form but is not communicated as a PCI bus transaction infringes the asserted claims. [ECF No. 560-16 ¶ 14 (disputing that the Specification's requirements for a PCI bus transaction, including the use of control signals, apply); id. ¶ 15 (claiming that EMC's accused products, which do not include the control signals identified in the Specification, nonetheless generate PCI bus transactions)]. ACQIS's own expert, Dr. Thomas Gafford, testified at his deposition that he was unaware of whether the

accused products communicate a PCI bus transaction in a parallel form. [ECF No. 504 ¶ 53]. At best, ACQIS asserts that EMC's products modify *some data* from a parallel to serial form prior to communicating or transacting that data, [ECF No. 560-3 ¶ 59], but ACQIS does not actually identify a *PCI bus transaction* that is converted from parallel to serial form and communicated by the accused products, [ECF No. 504 ¶¶ 52–53; ECF No. 503 at 46–48].

ACQIS does not dispute that “[t]he asserted claims require a PCI bus transaction, beginning in parallel form, to be converted into serial form for transmission across a serial interface.” [ECF No. 504 ¶ 49]; see also [ECF No. 560-16 ¶ 24]. As the Court stated in its Order on claim construction, “ACQIS repeatedly represented that ‘the whole point’ of the invention is to convert a PCI bus transaction from parallel to serial and back to parallel.” [ECF No. 389 at 14]. ACQIS has not shown that EMC's accused products serialize a PCI bus transaction from a parallel form consistent with the asserted claims and has therefore failed to demonstrate that the products infringe those claims. See Network, 242 F.3d at 1353 (noting that summary judgment is appropriate where “no reasonable jury could have found infringement on the undisputed facts or when all reasonable factual inferences are drawn in favor of the patentee”).

### **C. Communication of All Bits of a PCI Transaction**

This Court has construed the term “communicating . . . PCI bus transaction” to mean “communicating a PCI bus transaction, including all address, data, and control bits.” [ECF No. 389 at 17–18]. EMC contends that the terms “address, data, and control bits” should be given the meaning ascribed to them in the Specification. [ECF No. 503 at 52–53]. ACQIS argues that these terms should exclude any address, data, or control bits that pertain to PCI interface control



signals, as this Court has construed the claims as not requiring a physical PCI bus. [ECF No. 560-15 at 46].

This Court has already concluded that the claims are limited by the Specification in its entirety. Therefore, for the reasons described above, there is no infringement, and summary judgement is appropriate.

#### **IV. CONCLUSION**

Accordingly, EMC's motion for summary judgement of non-infringement, [ECF No. 502], is GRANTED. The remaining pending motions, [ECF Nos. 237, 354, 356, 413, 418, 419, 450, 452, 455, 461, 464, 466, 494, 498, 506, 509, 511, 513, 515, 518, 521, 524, 527], are DENIED as moot.

**SO ORDERED.**

February 19, 2021

/s/ Allison D. Burroughs  
ALLISON D. BURROUGHS  
U.S. DISTRICT JUDGE

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**UNITED STATES DISTRICT COURT  
DISTRICT OF MASSACHUSETTS**

ACQIS, LLC

Plaintiff

CIVIL ACTION

V.

NO. 14-13560-ADB

EMC Corporation

Defendant

**ORDER OF DISMISSAL**

Burroughs, D. J.

In accordance with the Court's Memorandum and Order dated February 19, 2021 it is hereby ORDERED that the above-entitled action be and hereby is DISMISSED.

By the Court,

2/19/2021  
Date

/s/ Christina McDonagh  
Deputy Clerk



US007363416B2

(12) **United States Patent**  
**Chu**

(10) **Patent No.:** **US 7,363,416 B2**

(45) **Date of Patent:** **\*Apr. 22, 2008**

(54) **COMPUTER SYSTEM UTILIZING  
MULTIPLE COMPUTER MODULES WITH  
PASSWORD PROTECTION**

(58) **Field of Classification Search** ..... 710/300-317,  
710/62-64, 72-73; 709/214-219, 226-227  
See application file for complete search history.

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(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
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(Continued)

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This patent is subject to a terminal dis-  
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(Continued)

(21) Appl. No.: **11/124,851**

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*Primary Examiner*—Raymond N Phan

(74) *Attorney, Agent, or Firm*—Townsend and Townsend  
and Crew LLP

(65) **Prior Publication Data**

US 2005/0204083 A1 Sep. 15, 2005

(57) **ABSTRACT**

**Related U.S. Application Data**

(63) Continuation of application No. 11/097,694, filed on  
Mar. 31, 2005, which is a continuation of application  
No. 10/772,214, filed on Feb. 3, 2004, now Pat. No.  
7,099,981, which is a continuation of application No.  
09/569,758, filed on May 12, 2000, now Pat. No.  
6,718,415.

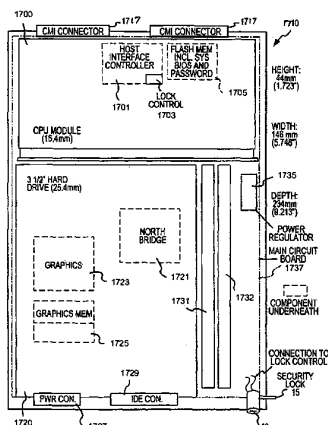
(60) Provisional application No. 60/134,122, filed on May  
14, 1999.

(51) **Int. Cl.**  
**G06F 13/20** (2006.01)

(52) **U.S. Cl.** ..... **710/313; 710/301; 710/315;  
709/227**

A computer system for multi-processing purposes. The  
computer system has a console comprising a first coupling  
site and a second coupling site. Each coupling site comprises  
a connector. The console is an enclosure that is capable of  
housing each coupling site. The system also has a plurality  
of computer modules, where each of the computer modules  
is coupled to a connector. Each of the computer modules has  
a processing unit, a main memory coupled to the processing  
unit, a graphics controller coupled to the processing unit,  
and a mass storage device coupled to the processing unit.  
Each of the computer modules is substantially similar in  
design to each other to provide independent processing of  
each of the computer modules in the computer system.

**94 Claims, 18 Drawing Sheets**



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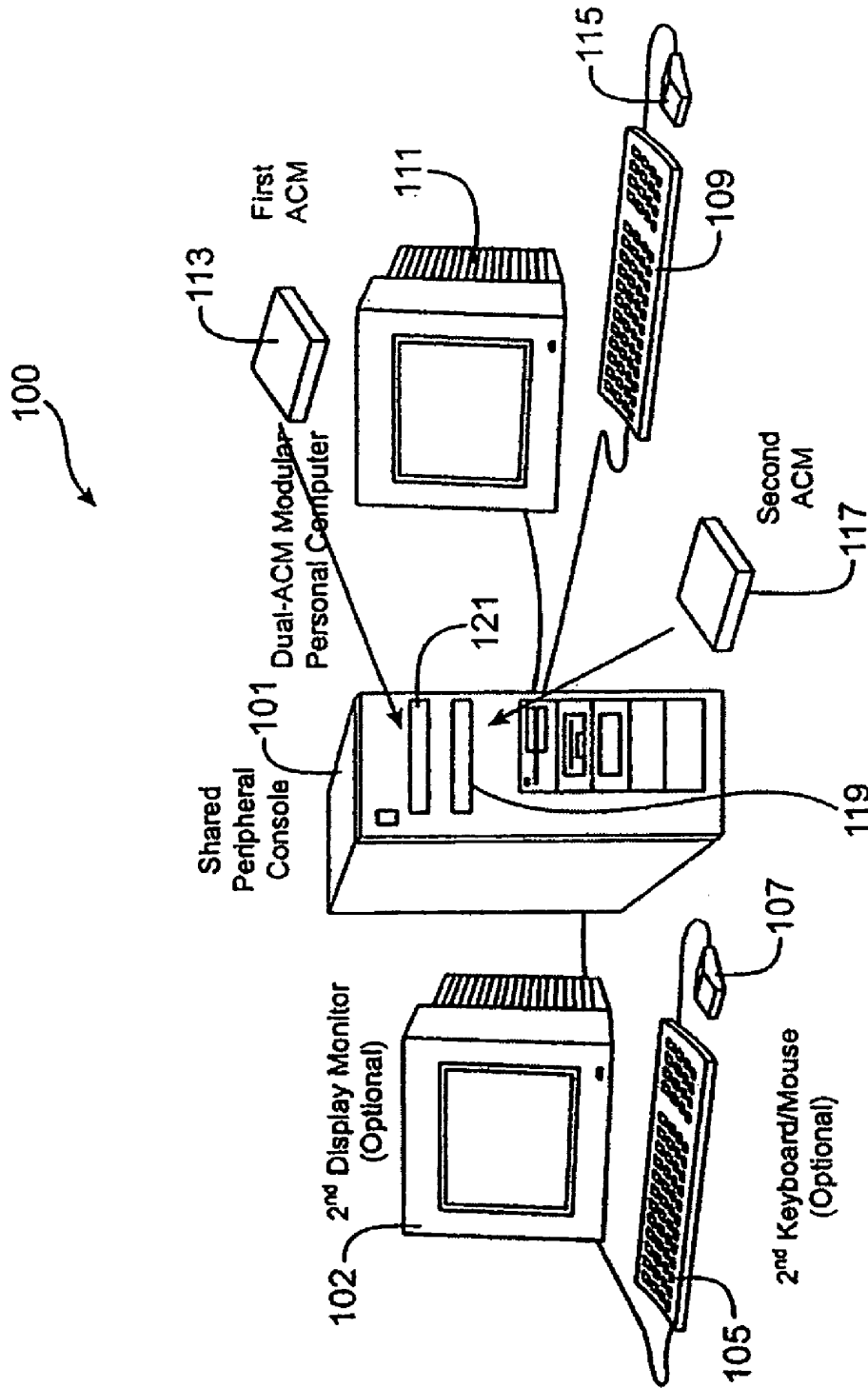


FIG. 1

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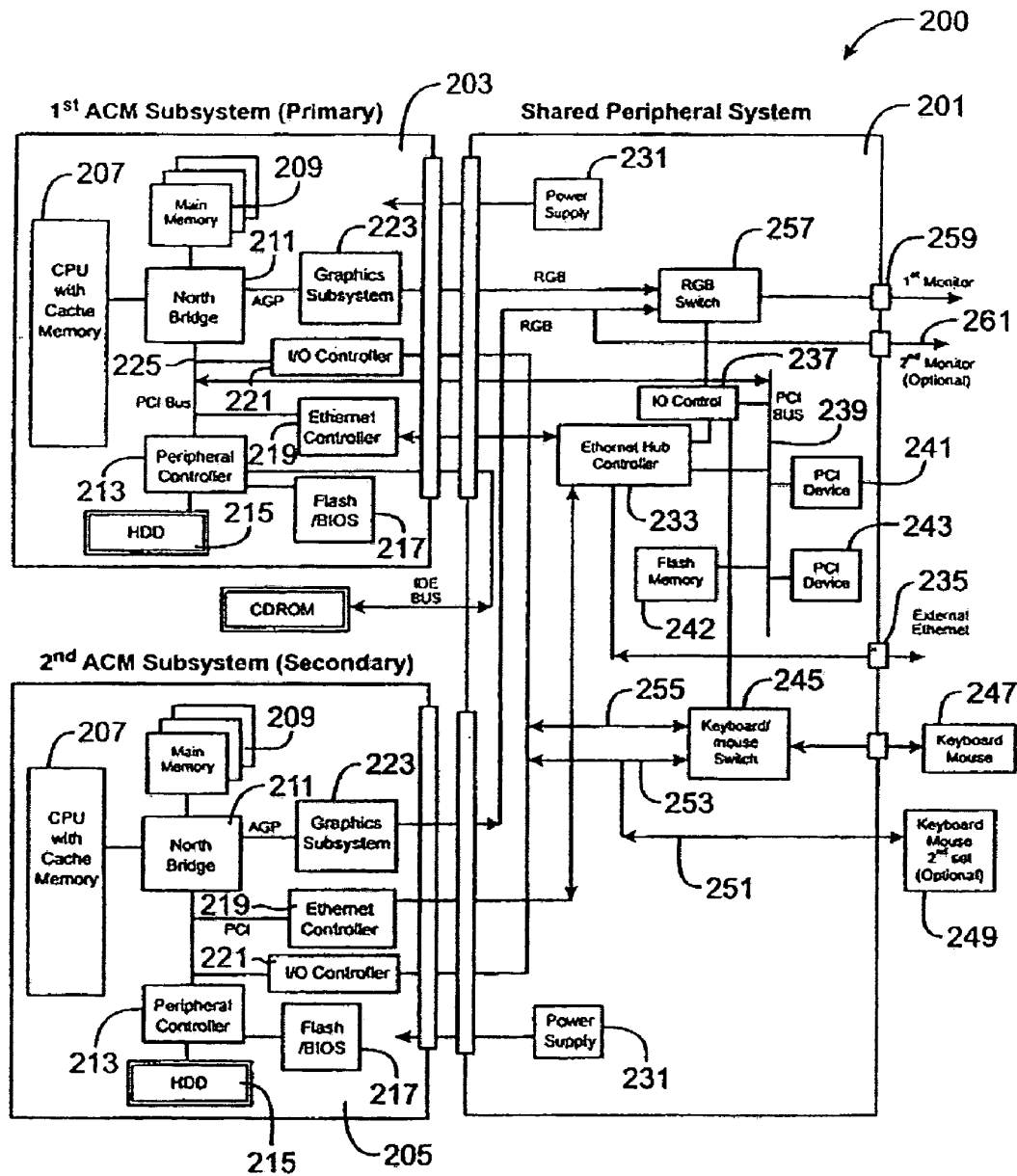


FIG. 2

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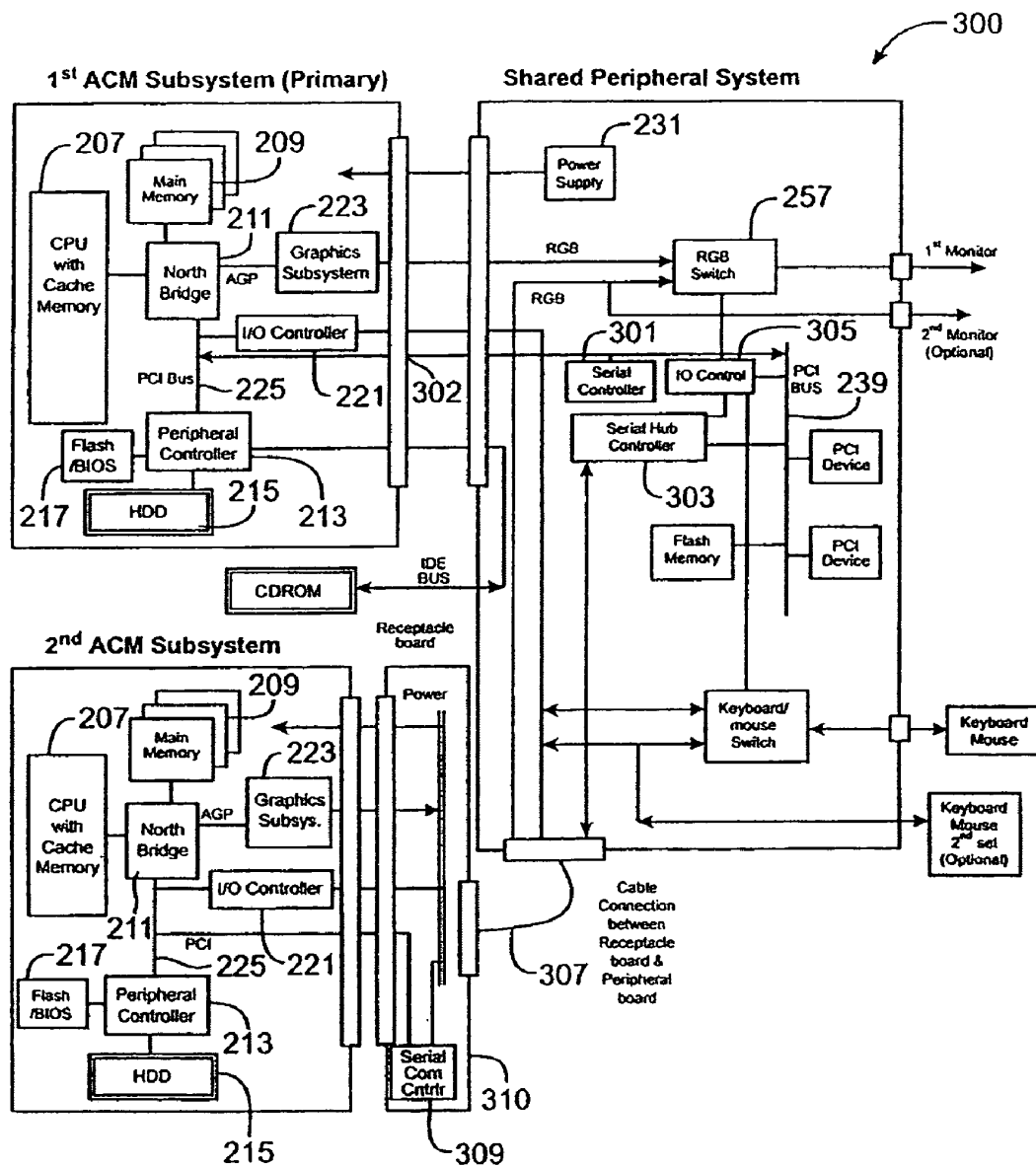


FIG. 3



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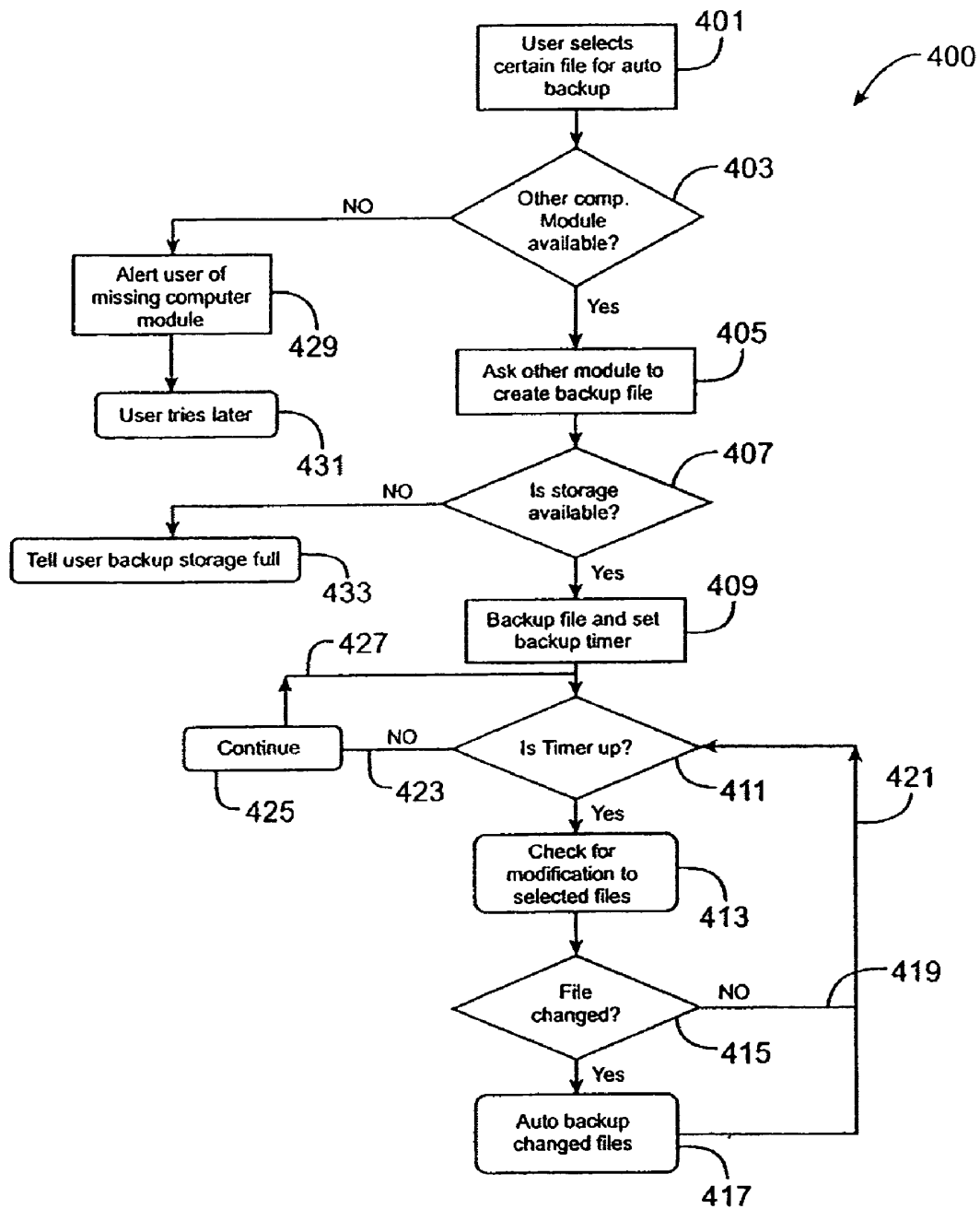


FIG. 4

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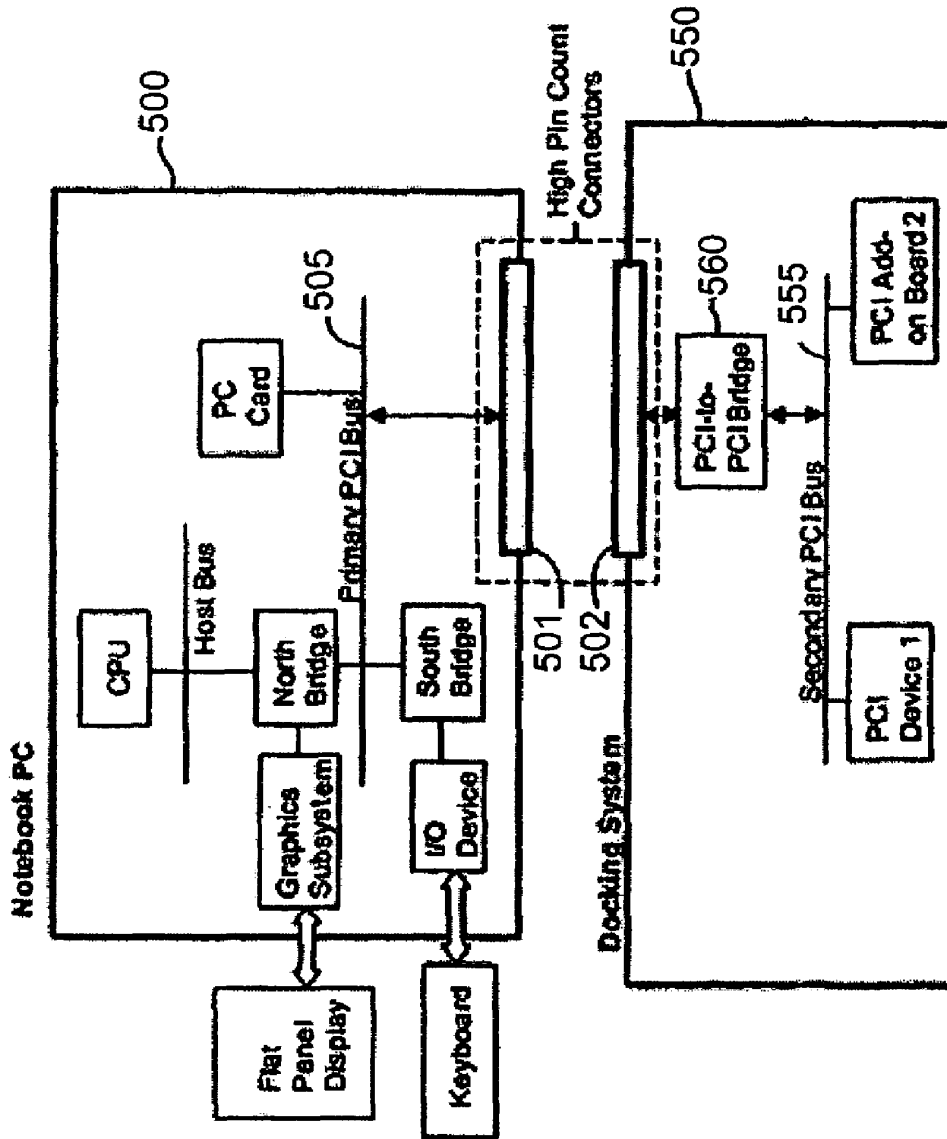


Fig. 5

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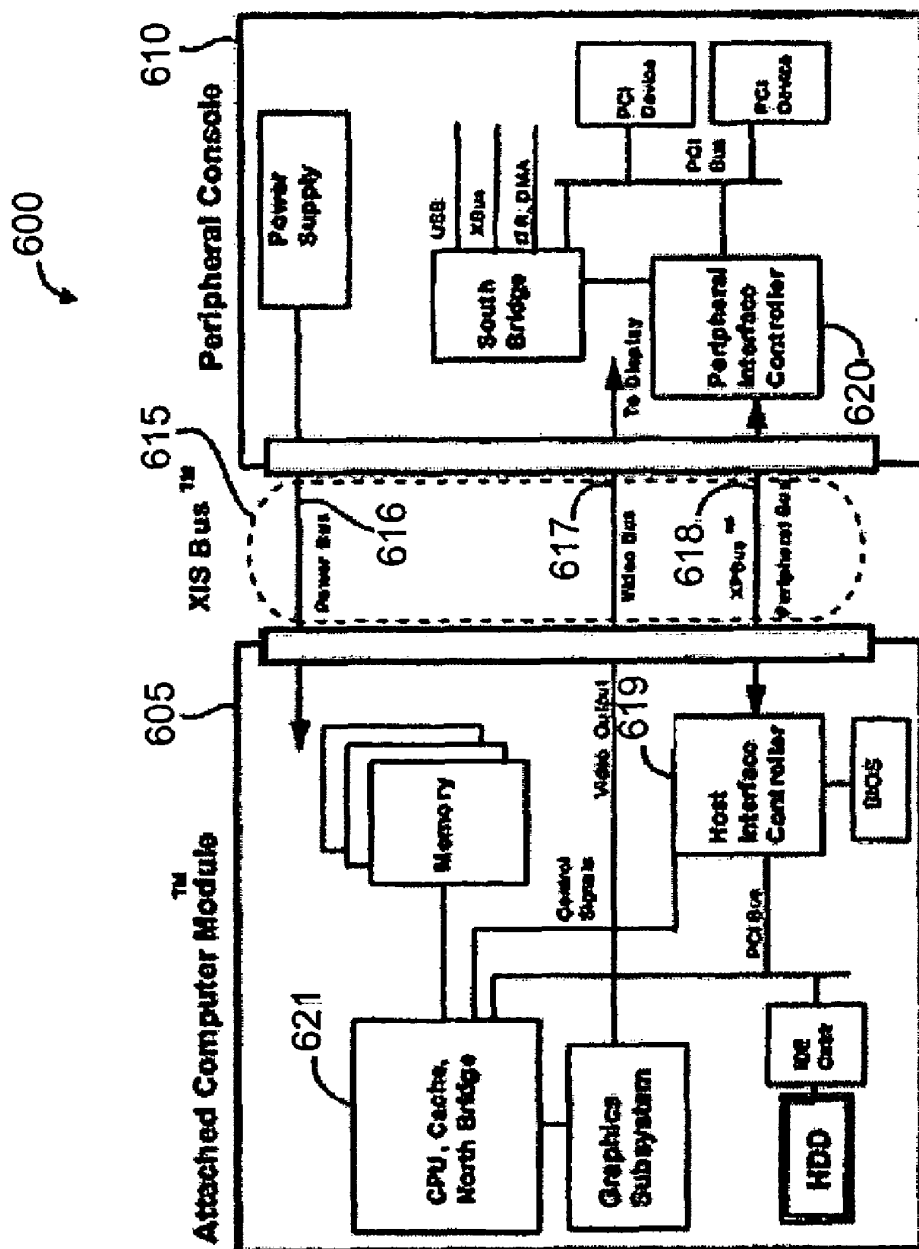


FIG. 6

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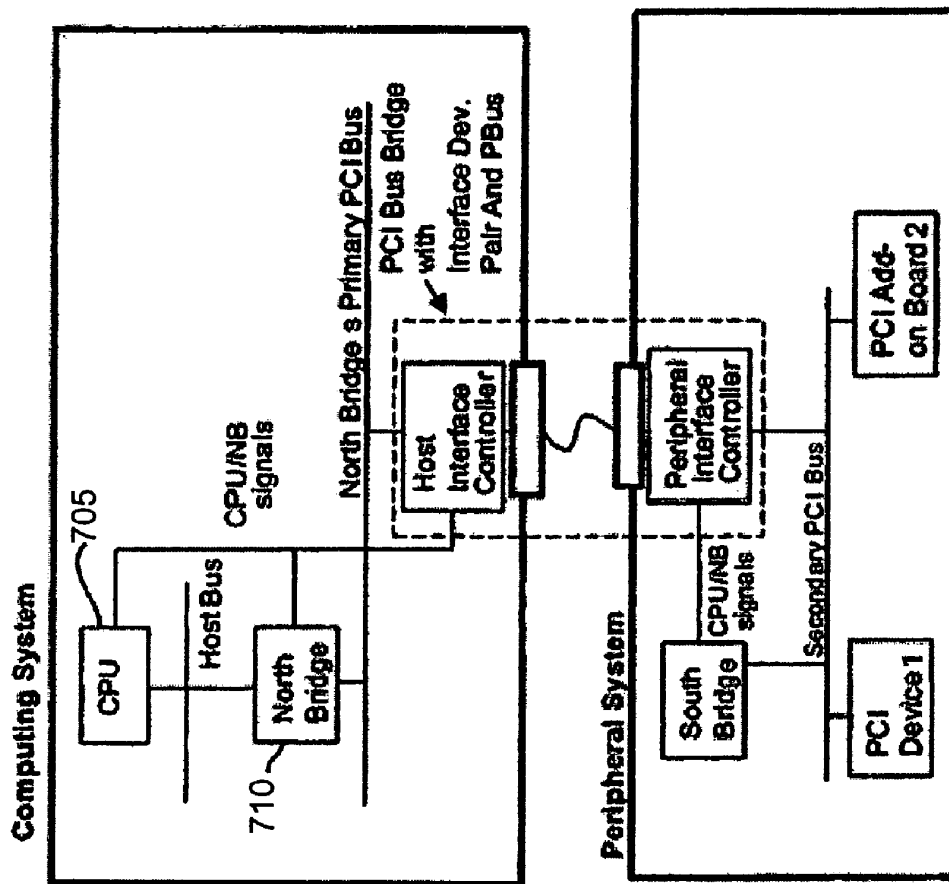


FIG. 7

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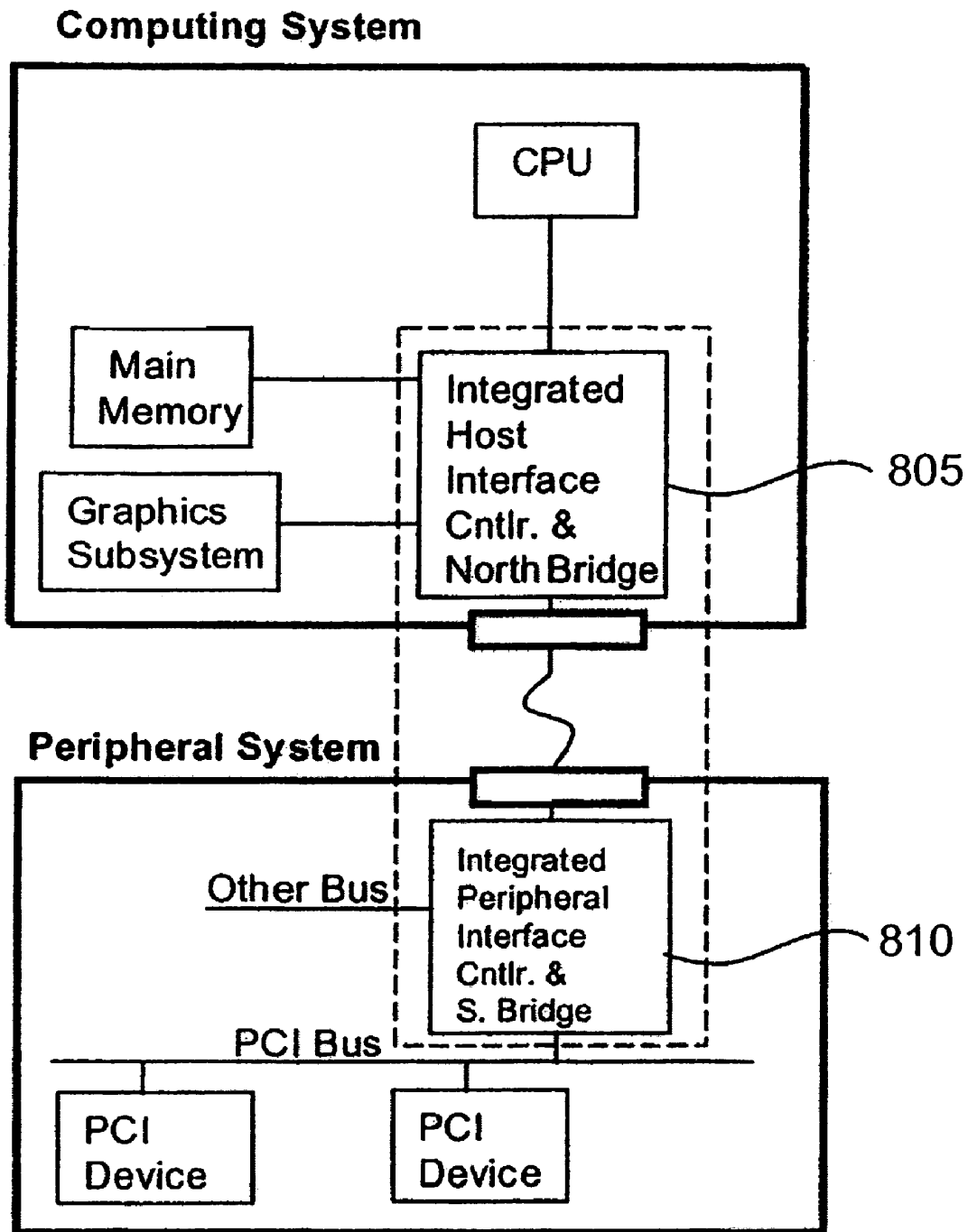


FIG. 8



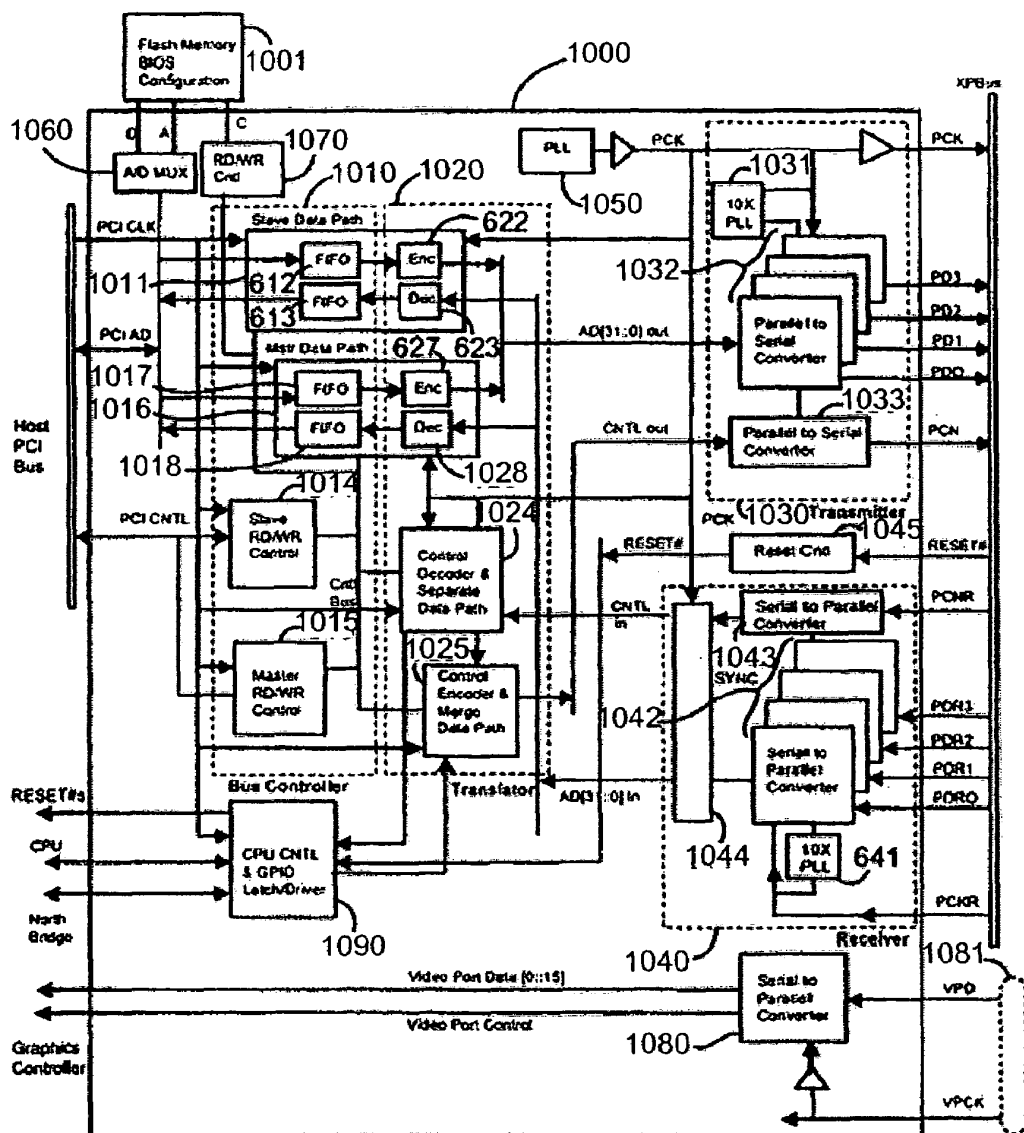


FIG. 10





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	Symbol	Signal	Data Rate	Description
1	PDO RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	-Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	POR0 RTN			GND
20	POR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	POR0 -			Peripheral to Computer LVDS Data 0 -
22	POR1 RTN			GND
23	POR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	POR1 -			Peripheral to Computer LVDS Data 1 -
25	POR2 RTN			GND
26	POR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	POR2 -			Peripheral to Computer LVDS Data 2 -
28	POR3 RTN			GND
29	POR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	POR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIG.12

**FIG. 13**

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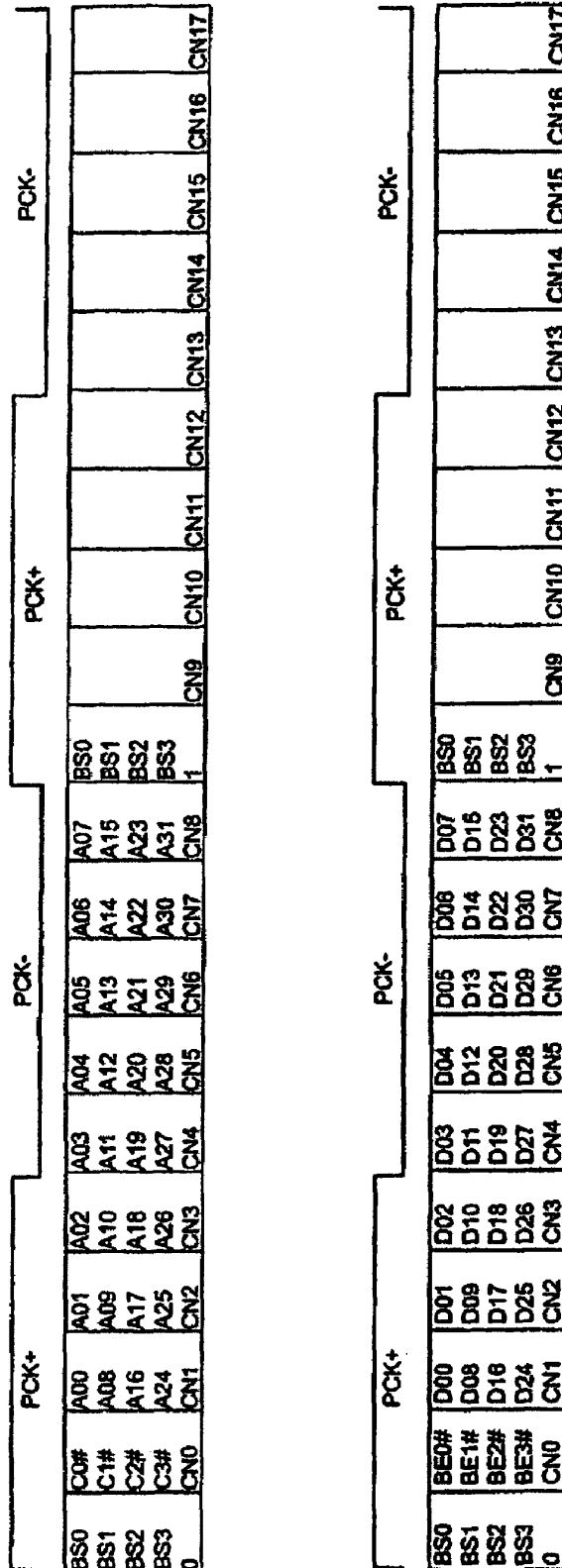


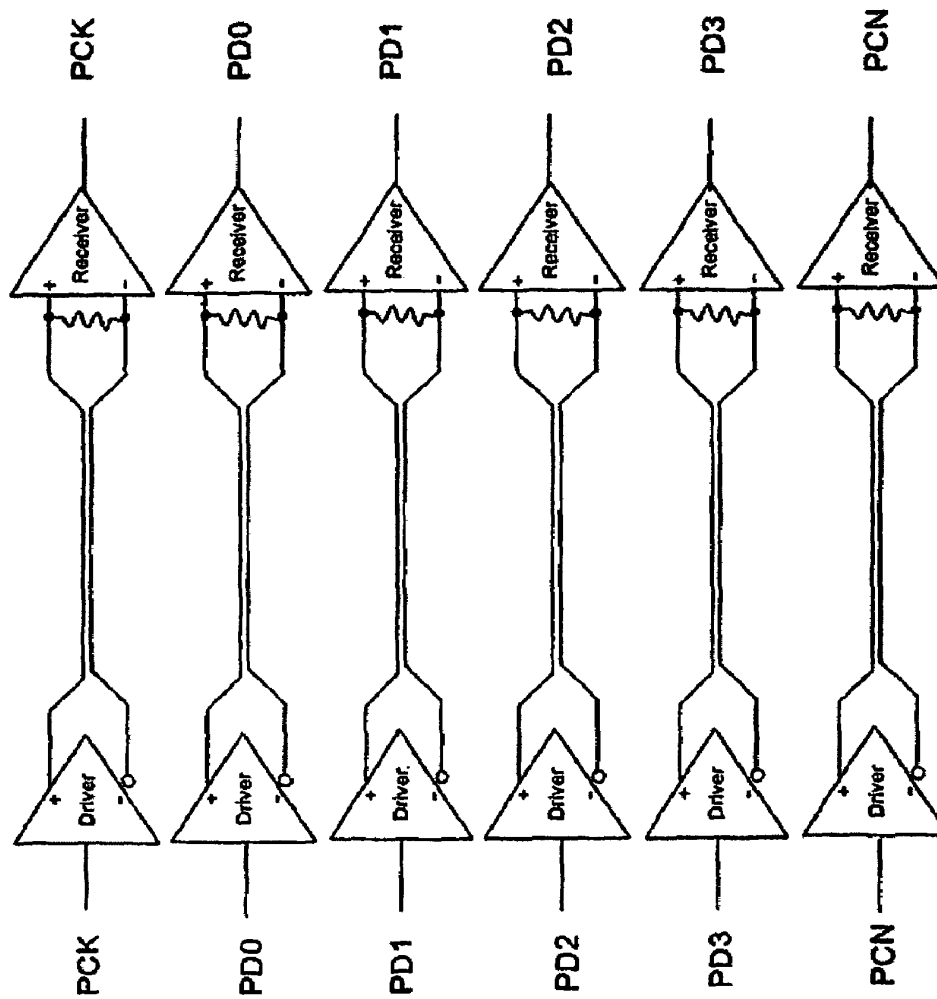
FIG. 14

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Name	Type	Pins	Description
AD[31:0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3:0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type. C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP# & TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error, Secondary bus SERR# asserted. Posted write transaction: data parity error on target bus, Posted write transaction discarded, Master abort, Target abort Delayed read or write transaction discarded, and
REQ#	TS	1	Delayed transaction master timeout.
GNT#	Input	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
CLKRUN#	I/OD	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
PCICK	Input	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
			PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

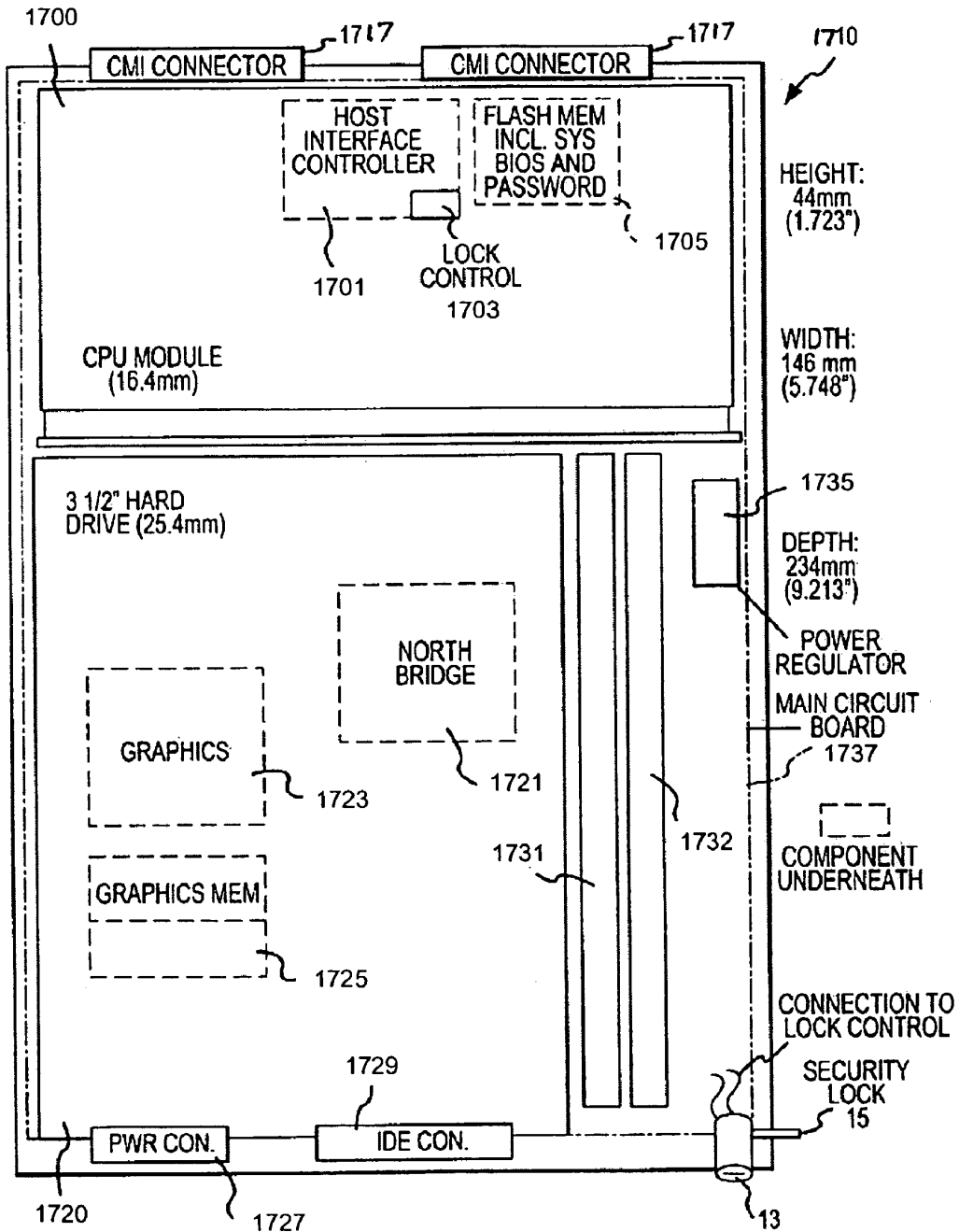
FIG. 16

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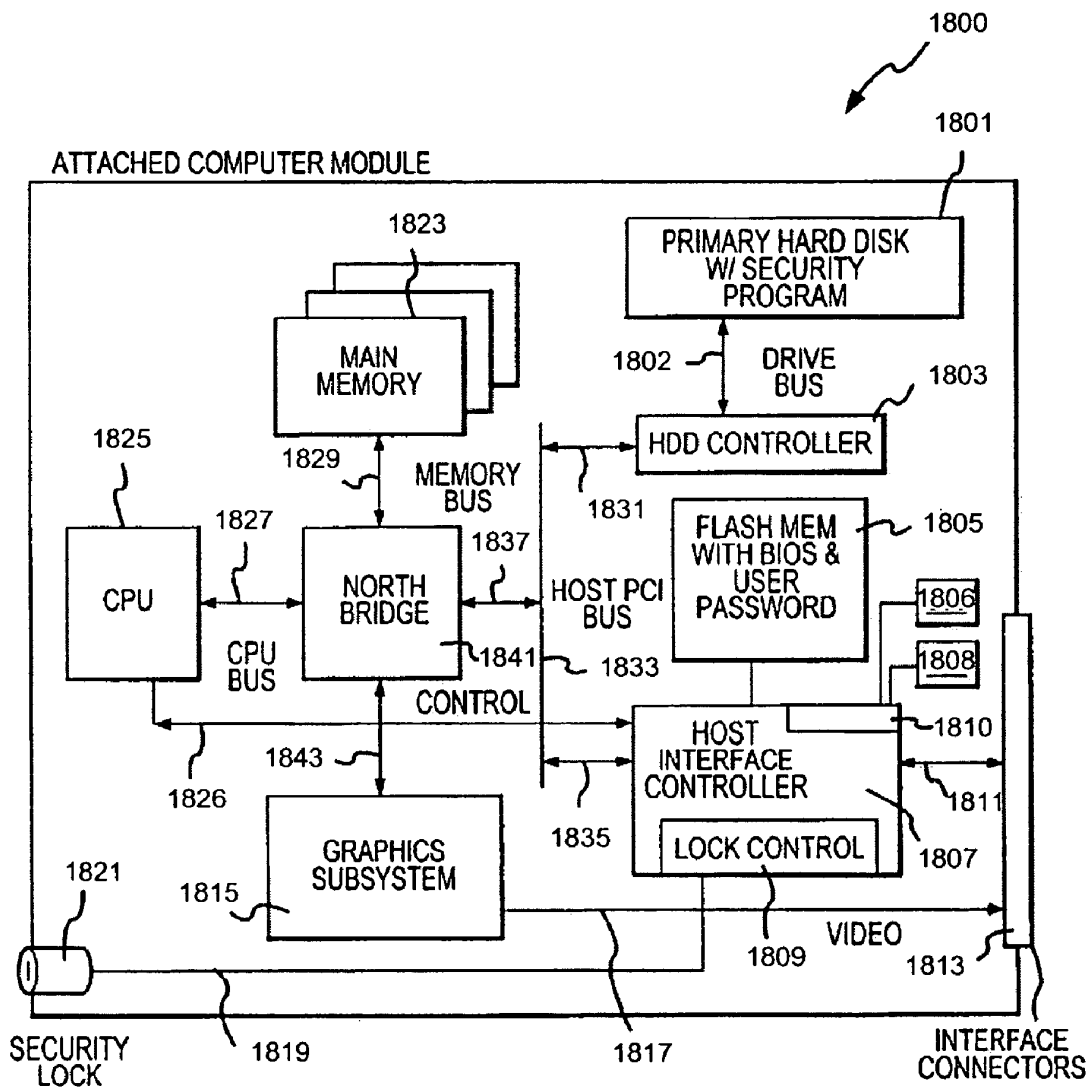


FIG. 18

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# COMPUTER SYSTEM UTILIZING MULTIPLE COMPUTER MODULES WITH PASSWORD PROTECTION

## CROSS REFERENCE TO RELATED APPLICATIONS

The present application claims priority as a continuation of U.S. nonprovisional patent application Ser. No. 11/097,694, filed Mar. 31, 2005, which is a continuation of U.S. nonprovisional patent application Ser. No. 10/772,214, filed Feb. 3, 2004 now U.S. Pat. No. 7,099,981, which is a continuation of U.S. nonprovisional patent application Ser. No. 09/569,758, filed May 12, 2000 (Now U.S. Pat. No. 6,718,415), which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999, commonly assigned, and hereby incorporated by reference.

## BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller

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flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use.

Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel's slot 1 architecture. For example, two Pentium II cartridges can be plugged into two "slot 1" card slots on a motherboard to form a Dual-processor system. The two CPU's share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.



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The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in FIG. 5. In FIG. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

An interface such as that shown in FIG. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W.Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

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Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

## BRIEF SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

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In still further embodiments, the present invention provides methods of using multiple computer modules.

The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed

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address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module "ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive

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and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent "finger print" on the attached computer module.

In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module "ACM") into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., flat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached Figs.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

FIG. 3 is a simplified block diagram of a computer system according to a further alternative embodiment of the present invention; and

FIG. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

FIG. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

FIG. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

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FIG. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

FIG. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

FIG. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

FIG. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits transmitted in each clock cycle of the XPBus.

FIG. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

FIG. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

FIG. 17 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention.

FIG. 18 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

FIG. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.



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In the present embodiment, each ACM **113** includes computer components, as will be described below, including a central processing unit "CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) **121** is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998, commonly assigned, and hereby incorporated by reference for all purposes.

In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs' graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly, input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive "HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be

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used for the primary ACM if a high bandwidth peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

The shared peripheral console has a chassis and a motherboard that connects the following devices:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. RGB monitor,
- 3) Add-on means, e.g. PCI add-on slots,
- 4) Two Computer Module Bays (CMB) with connectors to two ACMs,
- 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
- 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
- 7) Communication device, e.g. modem,
- 8) Power supply, and others.

The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of FIG. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM **203** is connected to PCI peripheral devices in the peripheral console through the PCI bus **225** that passes through the connection between primary ACM **203** and peripheral console **201**. As shown, ACM has a CPU module **207** coupled to the PCI bus through a North Bridge **211**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, peripheral controller **213** is coupled to BIOS/flash memory **217**. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module **215**. Among other elements, the ACM includes north bridge **215**, graphics subsystem **223** (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module **215** is the PCI bus. In a specific embodiment, North Bridge unit **211** often couples to a computer memory **209**, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the

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IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **215** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **215** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection.

The ACM also has a network controller, which can be an Ethernet controller **219**, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub **233** in the console, which includes shared peripheral system **201**.

Also shown is the second ACM **205**. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM **219** accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g. CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port **235**, which connects to an external network.

The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g. Windows 98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

The Ethernet hub also couples to PCI bus **239**, which connects to PCI devices **241**, **243**, e.g., modem, SCSI controller. A flash memory **242** can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those implementations described in U.S. Ser. No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub **233** also couples

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to an I/O control **237**, which connects to keyboard/mouse switch **245**, which couples to keyboard/mouse **247**. Optionally, the keyboard/mouse switch also couples to a second keyboard/house **259** via PS2 or USB signal line **251**. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller **221** in each ACM via lines **253**, **255**. The I/O control **237** also couples to an RGB switch **257**, which allows video signals to pass to the first monitor **259**. Alternatively, the RGB switch couples to a second monitor **261**. The RGB switch includes analog video switches such as MAXIM's MAX4545.

The peripheral system **201** also has an independent power supply **231** for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 3 is a simplified block diagram **300** of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this FIG. as the previous FIGS. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous FIG. A primary ACM **203** is connected to PCI peripheral devices in the peripheral console through the PCI bus **225** that passes through the connection between primary ACM **203** and peripheral console **201**. As shown, ACM has a CPU module **207** coupled to the PCI bus through a North Bridge **211**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, peripheral controller **213** is coupled to BIOS/flash memory **217**. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module **215**. Among other elements, the ACM includes north bridge **215**, graphics subsystem **223** (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module **215** is the PCI bus. In a specific embodiment, North Bridge unit **211** often couples to a computer

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memory 209, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit 215 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 215 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection.

The ACM also has a network controller, which can be coupled to a serial port 302, which is coupled to the PCI bus in the ACM. The serial port is coupled to the peripheral console through a serial controller 301 in the serial console. The serial controller is connected to PCI bus 239. The serial controller is also coupled to a serial hub controller 303, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board 310 is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection 307 to the peripheral board 300. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

The Dual ACM system can support different usage models:

1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.
2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

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A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting, firewall, etc.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step 401) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step 403. If so, the method in the originating module requests the other computer module to create (step 405) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step 429. The method then has the user try later 431, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step 433) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step 409), the software in the originating ACM sets a timer to check (step 411) for file modification via branches 423, 427 through continue, step 425 process. If a file selected for backup has been modified (step 415), then the file is automatically back up to the other ACM again, step 417. Alternatively, the method returns to step 411 through branch 421.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present



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embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 6 is a block diagram of one embodiment of a computer system 600 using the interface of the present invention. Computer system 600 includes an attached computer module (ACM) 605 and a peripheral console 610, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference. The ACM 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615. The XIS bus 615 includes power bus 616, video bus 617 and peripheral bus (XPBus) 618, which is also herein referred to as an interface channel. The power bus 616 transmits power between ACM 605 and peripheral console 610. In a preferred embodiment power bus 616 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 617 transmits video signals between the ACM 605 and the peripheral console 610. In a preferred embodiment, the video bus 617 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 618 is coupled to host interface controller (HIC) 619 and to peripheral interface controller (PIC) 620, which is also sometimes referred to as a bay interface controller.

In the embodiment shown in FIG. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 8, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge.

FIG. 9 is a more detailed block diagram of one embodiment of an HIC 905 and a PIC 955 of the present invention. HIC 905 includes a peripheral component interconnect (PCI) bus controller 910, an XPBus controller 915, a phase lock loop (PLL) clock 920 and an input/output (IO) control 925. Similarly, PIC 955 includes a PCI bus controller 960, an XPBus controller 965, a PLL clock 970 and an IO control 975. PCI bus controllers 910 and 960 are coupled to the primary and secondary PCI buses 930 and 980, respectively, and manage PCI transactions on the primary and secondary PCI buses 930 and 980, respectively. Similarly, XPBus Controllers 915 and 965 are coupled to XPBus 990. XPBus controller 915 drives the PCK line 991 and PD[0:3] and PCN lines 992 while XPBus controller 965 drives the PCKR lines 993, the PDR[0:3] and PCNR lines 994 and the RESET# line 995.

PCI bus controller 910 receives PCI clock signals from the primary PCI bus 930 and is synchronized to the PCI clock. However, as indicated in FIG. 9, the XPBus controller 915 is asynchronous with the PCI bus controller 910. Instead, the XPBus controller receives a clock signal from the PLL clock 920 and is synchronized therewith. PLL clock 920 generates a clock signal independent of the PCI clock. The asynchronous operation of the PCI bus and the XPBus allows the PCI Bus to change in frequency, for example as in a power down situation, without directly affecting the XPBus clocking. In the embodiment shown in FIG. 9, the

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PLL clock 920 generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock 920 generates a clock signal having a frequency of 132 MHz.)

The XPBus 990 operates at the clock speed generated by the PLL clock 920. Therefore, PCK, the clock signal from the XPBus controller 915 to XPBus controller 965 has the same frequency as the clock signal generated by PLL clock 920. XPBus controller 965 receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock signal PCKR, the clock signal from the XPBus controller 965 to XPBus controller 915. Accordingly, PCKR also has the same frequency as that generated by the PLL clock 920. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XPBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

As indicated in FIG. 9, PLL clock 970 is asynchronous with the XPBus controller 965. Instead, PLL clock 970 independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus 980. The secondary PCI bus 980 operates at the same clock speed as the primary PCI bus 930, namely at a frequency of 33 MHz.

FIG. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in FIG. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.

HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.

Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder 1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to

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transmittal on the XDBus. Similarly, address and data information from the receivers is decoded by decoders **1023** and **1028** to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs **1013** and **1018** prior to being transferred to the host PCI bus. FIFOs **1012**, **1013**, **1017** and **1018**, allow bus controller **1010** to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller **1010** also comprises slave read/write control (RD/WR Cntl) **1014** and master read/write control (RD/WR Cntl) **1015**. RD/WR controls **1014** and **1015** are involved in the transfer of PCI control signals between bus controller **1010** and the host PCI bus.

Bus controller **1010** is coupled to translator **1020**. Translator **1020** comprises encoders **1022** and **1027**, decoders **1023** and **1028**, control decoder & separate data path unit **1024** and control encoder & merge data path unit **1025**. As discussed above encoders **1022** and **1027** are part of slave data unit **1011** and master data unit **1016**, respectively, receive PCI address and data information from FIFOs **1012** and **1017**, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XDBus. Similarly, decoders **1023** and **1028** are part of slave data unit **1011** and master data unit **1016**, respectively, and format address and data information from receiver **1040** into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit **1025** receives PCI control signals from the slave RD/WR control **1014** and master RD/WR control **1015**. Additionally, control encoder & merge data path unit **1025** receives control signals from CPU CNTL & GPIO latch/driver **1090**, which is coupled to the CPU and north bridge (not shown in FIG. 10). Control encoder & merge data path unit **1025** encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter **1030**, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XDBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit **1024** receives control bits from receiver **1040** which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XDBus. Control decoder & separate data path unit **1024** separates the control bits it receives from receiver **1040** into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

Transmitter **1030** receives multiplexed parallel address/data (A/D) bits and control bits from translator **1020** on the AD[31::0] out and the CNTL out lines, respectively. Transmitter **1030** also receives a clock signal from PLL **1050**. PLL **1050** takes a reference input clock and generates PCK that drives the XDBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XDBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

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The multiplexed parallel A/D bits and some control bits input to transmitter **1030** are serialized by parallel to serial converters **1032** of transmitter **1030** into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XDBus. Other control bits are serialized by parallel to serial converter **1033** into 10 bit packets and send out on control line PCN of the XDBus.

A 10× multiplier **1031** receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters **1032** and **1033**. The parallel to serial converters **1032** and **1033** perform bit shifting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters **1032** and **1033** shift bits at 10 times the PCK rate, the bit rate for the serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XDBus is the same as the PCK rate, i.e., 106 MHz. As the PCI buses operate at a clock and bit rate of 33 MHz, the XDBus has a clock rate that is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

Receiver **1040** receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver **1040** also receives PCKR on the XDBus as well as the clock signal PCK from PLL **1050**. The synchronizer (SYNC) **1044** of receiver **1040** synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XDBus into PCK clock timing.

Serial to parallel converters **1042** convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders **1023** and **1028** and control decoder and separate data path unit **1024**, respectively. Serial to parallel converter **1043** receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path **1024**.

A 10× multiplier **1041** receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters **1042** and **1043**. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters **1042** and **1043** perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted that the rate at which bit packets are transmitted on the XDBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders **1023** and **1028** by way of the AD[3::0] in line and to control decoder & separate data path unit **1024** by way of CNTL in lines, respectively.

Reset control unit **1045** of HIC **1000** receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit **1045** then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit **1090**.

As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XDBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XDBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XDBus is able to interface such PCI buses without backup delays because the XDBus operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver **1090** is responsible for latching input signals from the CPU and north bridge and sending the



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signals to the translator. It also takes decoded signals from the control decoder & separate data path unit **1024** and drives the appropriate signals for the CPU and north bridge.

In the embodiment shown in FIG. **10**, video serial to parallel converter **1080** is included in HIC **1000**. In another embodiment, video serial to parallel converter **1080** may be a separate unit from the HIC **1000**. Video serial to parallel converter **1080** receives serial video data on line VPD and a video clock signal VPCK from line VPCK of video bus **1081**. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in FIG. **10**) on the video port data [0:15] and video port control lines, respectively.

HIC **1000** handles the PCI bus control signals and control bits from the XDBus representing PCI control signals in the following ways:

1. HIC **1000** buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XDBus;
2. HIC **1000** manages the signal locally; and
3. HIC **1000** receives control bits from XDBus, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

FIG. **11** is a detailed block diagram of one embodiment of the PIC of the present invention. PIC **1100** is nearly identical to HIC **1000** in its function, except that HIC **1000** interfaces the host PCI bus to the XDBus while PIC **1100** interfaces the secondary PCI bus to the XDBus. Similarly, the components in PIC **1100** serve the same function as their corresponding components in HIC **1000**. Reference numbers for components in PIC **1100** have been selected such that a component in PIC **1100** and its corresponding component in HIC **1000** have reference numbers that differ by **500** and have the same two least significant digits. Thus for example, the bus controller in PIC **1100** is referenced as bus controller **1110** while the bus controller in HIC **1000** is referenced as bus controller **1010**. As many of the elements in PIC **1100** serve the same functions as those served by their corresponding elements in HIC **1000** and as the functions of the corresponding elements in HIC **1000** have been described in detail above, the function of elements of PIC **1100** having corresponding elements in HIC **1000** will not be further described herein. Reference may be made to the above description of FIG. **10** for an understanding of the functions of the elements of PIC **1100** having corresponding elements in HIC **1000**.

As suggested above, there are also differences between HIC **1000** and PIC **1100**. Some of the differences between HIC **1000** and PIC **1100** include the following. First, receiver **1140** in PIC **1100**, unlike receiver **1040** in HIC **1000**, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC **1000** synchronizes the PCKR clock to the PCK clock locally generated by PLL **1050**. PIC **1100** does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC **1000**. Another difference between PIC **1100** and HIC **1000** is the fact that PIC **1100** contains a video parallel to serial converter **1189** whereas HIC **1000** contains a video serial to parallel converter **1080**. Video parallel to serial converter **1189** receives 16 bit parallel video capture data and video control signals on the Video Port Data [0:15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. **11**) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of

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video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC **1100**, unlike HIC **1000**, contains a clock doubler **1182** to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter **1182** through buffer **1183** and is sent to serial to parallel converter **1080** through buffer **1184**. Additionally, reset control unit **1135** in PIC **1100** receives a reset signal from the CPU CNTL & GPIO latch/driver unit **1190** and transmits the reset signal on the RESET# line to the HIC **1000** whereas reset control unit **1045** of HIC **1000** receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit **1090** because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC **1100** to the HIC **1000**.

Like HIC **1000**, PIC **1100** handles the PCI bus control signals and control bits from the XDBus representing PCI control signals in the following ways:

1. PIC **1100** buffers clocked control signals from the secondary PCI bus, encodes them and sends the encoded control bits to the XDBus;
2. PIC **1100** manages the signal locally; and
3. PIC **1100** receives control bits from XDBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

PIC **1100** also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

FIG. **12** is a table showing the symbols, signals, data rate and description of signals on the XDBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

FIG. **13** is a table showing the information transmitted on the XDBus during two clock cycles of the XDBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XDBus. In FIG. **13**, A00 to A31 represent 32 bits of PCI address A[31:0], D00 to D31 represent 32 bits of PCI data D[31:0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XDBus, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information sent in each clock cycle. As shown in FIG. **13**, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight A/D bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in FIG. **13** comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31:0] signals, 4 PCI C/BE# [3:0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

In the embodiment shown in FIG. **13**, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address

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transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.

Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBus between the HIC and the PIC.

FIG. 14 is a table showing the information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In this embodiment, the XPBus clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBus cycle. As can be seen in FIG. 14, there are no address or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

In the embodiment shown in FIG. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XPBus clock cycles. The first bit transmitted on the control line in each XPBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example, BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicate that a PCI bus is used whereas a BS3 value of one may indicate that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

FIG. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 15, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 15 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the

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target requiring communication in the reverse direction, target busy, and transmission error detected.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIG. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive "HDD" that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements.

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Some details of these elements with the present security system are described in more detail below.

FIG. 17 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 1710, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit "CPU" module 1700, and a second portion, which includes a hard drive module 1720. A common printed circuit board 1737 houses these modules and the like. Among other features, the ACM includes the central processing unit module 1700 with a cache memory 1705, which is coupled to a north bridge unit 1721, and a host interface controller 1701. The host interface controller includes a lock control 1703. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 1717. Here, the CPU module is spatially located near connector 1717.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 1701 is coupled to BIOS/flash memory 1705. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 1703 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 1720. Among other elements, the hard drive module includes north bridge 1721, graphics accelerator 1723, graphics memory 1725, a power controller 1727, an IDE controller 1729, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface "PCI" bus 1731, 1732. A power regulator 1735 is disposed near the PCI bus.

In a specific embodiment, north bridge unit 1721 often couples to a computer memory, to the graphics accelerator 1723, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 1723 typically couples to a graphics memory 1723, and other elements. IDE controller 1729 generally supports and provides timing signals necessary for the WDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit 1720 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Win-

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dows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 1720 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 1720 may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

FIG. 18 is a simplified block diagram 1800 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 1800 has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram is an attached computer module 1800. The module 1800 has a central processing unit, which communicates to a north bridge 1841, by way of a CPU bus 1827. The north bridge couples to main memory 1823 via memory bus 1829. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory "DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 617 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 1815 via bus 1842. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2½



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inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **1802** and **1831**. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus **1837** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **1805** with a BIOS. The flash memory device **1805** also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller **1807** communicates to the north bridge via bus **1835** and host PCI bus. The host interface controller also has a lock control **1809**, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller **1807** communicates to the console using bus **1811**, which couples to connection **1813**.

In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device **1805**. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

In a specific embodiment, the present invention also includes a real-time clock **1810** in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz **1808** that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source **1806** such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such

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device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

1. A computer system comprising:
  - a console comprising a power supply, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing
  - the coupling sites,
  - a serial communication hub controller powered by the power supply, and

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a plurality of computer modules; each computer module coupled to one of the coupling site through the connector and the slot, comprising

a processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a main memory coupled to the processing unit, and

wherein each of the computer modules is substantially similar in design to each other and operates fully independent of each other; and wherein each computer module communicates with the console through two sets of unidirectional serial, differential signal channels which transmit data in opposite directions.

2. The computer system of claim 1 wherein each computer module further comprises a communication controller coupled to the serial communication controller in the console adapted to transfer data between any two of the computer modules and to an external network.

3. The computer system of claim 1 further comprises a hard disk drive coupled to the computer module.

4. The computer system of claim 1 wherein the computer module further comprises an interface controller coupled to a differential signal channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

5. The computer system of claim 4 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

6. A computer system comprising:

a console comprising a power supply, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing

the coupling sites,

an Ethernet hub controller coupled to an external network and powered by the power supply, and

a plurality of computer modules; each computer module coupled to one of the coupling site through the connector and the slot, comprising

a processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a main memory coupled to the processing unit,

an interface controller coupled to a differential signal channel for communicating an encoded serial data stream of Peripheral Component Interconnect (PCI) bus transaction, and

a network controller coupled to the Ethernet hub controller through the connector of the coupling site, wherein each of the computer modules is substantially similar in design to each other.

7. The computer system of claim 6 wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

8. The computer system of claim 6 wherein the encoded serial bit stream comprises 10 bit packets.

9. The computer system of claim 6 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

10. The computer system of claim 6 wherein the Ethernet hub controller adapted to transfer data between any two of the computer modules and to the external network.

11. A computer system comprising:

a console comprising a power supply, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being a first enclosure housing

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an Ethernet hub controller powered by the power supply, each coupling site, and

a plurality of computer modules, each coupled to one of the coupling sites through the connector and the slot; each computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device storing a security program that provides password protection for the computer module,

an interface controller coupled to a differential signal channel for communicating an encoded serial data stream of Peripheral Component Interconnect (PCI) bus transaction, and

an Ethernet controller coupled to the Ethernet hub controller through the connector of the coupling site; and wherein each of the computer modules operates fully independent of each other.

12. The computer system of claim 11 wherein the differential signal channel comprises two sets of unidirectional serial channels which transmit data in opposite directions.

13. The computer system of claim 11 wherein the Ethernet controllers of the computer modules are used for sharing peripheral devices residing in the console.

14. The computer system of claim 12 wherein each of the unidirectional serial channels comprises one or more pairs of differential signal lines.

15. The computer system of claim 11 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

16. A computer system comprising:

a console comprising a power supply, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being a first enclosure housing

the coupling sites,

a serial communication hub controller powered by the power supply, and

a plurality of computer modules; each computer module coupled to one of the coupling site through the connector and the slot, comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device storing a security program that provides password protection for the computer module,

a communication controller coupled to the serial communication hub controller through the connector of the coupling site, and

an interface controller coupled to a differential signal channel for communicating encoded serial data stream of Peripheral Component Interconnect (PCI) bus transaction;

wherein each of the computer modules operates fully independent of each other.

17. The computer system of claim 16 wherein the encoded serial bit stream comprises 10 bit packets.

18. The computer system of claim 16 wherein the interface controller couples to a flash memory with PCI configuration information.

19. The computer system of claim 16 wherein the computer module further comprises a second enclosure and a hard disk drive wherein the second enclosure houses the hard disk drive.

20. The computer system of claim 16 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

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21. A computer system comprising:  
a console comprising a video switch, a first coupling site  
and a second coupling site, each coupling site comprising a connector and a slot; the console being an enclosure housing  
the video switch,  
an Ethernet hub controller coupled to an external network,  
and  
a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector and the slot, and comprising  
a processing unit,  
a main memory coupled to the processing unit,  
a mass storage device storing a security program that provides password protection for the computer module,  
a graphics controller coupled to the video switch, and  
an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating encoded serialized Peripheral Component Interconnect (PCI) bus transaction data;  
wherein each of the computer modules operates fully independent of each other.

22. The computer system of claim 21 wherein the interface controller couples to a flash memory with PCI configuration information.

23. The computer system of claim 21 wherein the serial bit stream comprises one or more pairs of differential signal lines.

24. The computer system of claim 21 wherein the serial bit stream comprises 10 bit packets.

25. The computer system of claim 21 wherein the serial bit stream comprises PCI bus transaction with encoded PCI address and data bits.

26. A computer system comprising:  
a console comprising an Ethernet hub controller, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing  
the Ethernet hub controller,  
each coupling site, and  
a plurality of computer modules, each coupled to one of the coupling sites through the connector and the slot; each computer module comprising  
a processing unit,  
a main memory coupled to the processing unit,  
a mass storage device storing a security program that provides password protection for the computer module,  
an interface controller coupled to a differential signal channel for communicating encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and  
an Ethernet controller coupled to the Ethernet hub controller through the connector of the coupling site for communication between the computer modules;  
wherein each of the computer modules operates independent of each other, and wherein one of the computer modules can replace another one of the computer modules in operation.

27. The computer system of claim 26 wherein the interface controller couples to a flash memory with PCI configuration information.

28. The computer system of claim 26 wherein the Ethernet controllers of the computer modules are used for sharing peripheral devices residing in the console.

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29. The computer system of claim 26 wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

30. The computer system of claim 26 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

31. A computer system comprising:  
a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector and a slot; the console being an enclosure housing each coupling site, and  
a plurality of computer modules; each computer module coupled to the coupling site through the connector and the slot, and comprising  
a processing unit,  
a main memory coupled to the processing unit,  
a mass storage device storing a security program that provides password protection for the computer module,  
an interface controller coupled to a differential signal channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and  
a SCSI hard disk drive;  
wherein each of the computer modules is substantially similar in design to each other, and wherein one of the computer modules can provide protection against failure of another one of the computer modules.

32. The computer system of claim 31 wherein the encoded serial bit stream comprises 10 bit packets.

33. The computer system of claim 31 wherein the SCSI hard disk drive is removable while the computer module is in operation.

34. The computer system of claim 31 wherein the interface controller couples to a flash memory with PCI configuration information.

35. The computer system of claim 31 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

36. A computer system comprising:  
a console comprising an Ethernet controller coupled to an external network, a keyboard/mouse multi-port switch, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing the Ethernet controller, each coupling site, and  
a plurality of computer modules, each coupled to one of the coupling sites through the connector and the slot; each computer module comprising  
a processing unit,  
a main memory coupled to the processing unit,  
an interface controller coupled to a differential signal channel for communicating encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and  
a mass storage device storing a security program that provides password protection for the computer module;  
wherein each of the computer modules operates fully independent of each other; and wherein the keyboard/mouse multi-port switch switches between keyboard/mouse connection of the computer modules based on a command from a user.

37. The computer system of claim 36 wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

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38. The computer system of claim 36 wherein the interface controller couples to a flash memory with PCI configuration information.

39. The computer system of claim 36 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

40. The computer system of claim 36 wherein the command from the user is in the form of either a key on the keyboard or an icon on the screen that the mouse can click on.

41. A computer system comprising:

a console comprising a first coupling site, a second coupling site, each coupling site comprising a connector, the console being an enclosure that is capable of housing

each coupling site,

a serial communication hub controller coupled to an external network, and

a plurality of computer modules inserted into said console; each computer module coupled to one of the connectors of the console and comprising,

a processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a communication controller coupled to the serial communication hub controller,

a main memory coupled to the processing unit,

an interface controller coupled to a differential signal channel for communicating encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

wherein each of the computer modules provide independent processing in the computer system; and wherein one of the computer modules is configured to provide protection against failure of another of the plurality of computer modules.

42. The computer system of claim 41 wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

43. The computer system of claim 41 wherein the interface controller couples to a flash memory with PCI configuration information.

44. The computer system of claim 41 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

45. The computer system of claim 41 further comprises a hard disk coupled to the computer module.

46. A computer system comprising:

a console comprising a power supply, a first coupling site, and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing

each coupling site,

a plurality of computer modules, each coupled to one of the coupling sites through the connector and the slot; each computer module comprising

a processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a main memory coupled to the processing unit,

a graphics controller, and

an interface controller coupled to a differential signal channel for communicating encoded serialized bit stream of Peripheral Component Interconnect (PCI) bus transaction;

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wherein each of the computer modules operates fully independent of each other; and wherein the differential signal channel comprises two sets of unidirectional serial channels which transmit data in opposite directions, and wherein one of the computer modules can replace another one of the computer modules in operation.

47. The computer system of claim 46 wherein the encoded serial bit stream comprises 10 bit packets.

48. The computer system of claim 46 wherein each of the unidirectional serial channels comprises one or more pairs of differential signal lines.

49. The computer system of claim 46 wherein the console further houses a power supply that supplies DC power to the Ethernet controller and the computer modules.

50. The computer system of claim 46 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

51. A computer system comprising:

a console comprising an Ethernet hub controller, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing the Ethernet hub controller and the coupling sites; and

more than two computer modules, each coupled to one of the coupling site through the connector and the slot, comprising

a processing unit,

a main memory coupled to the processing unit,

an Ethernet controller coupled to the Ethernet hub controller through the connector of the coupling site for communication between the computer modules, and an interface controller coupled to a differential signal channel for communicating encoded serialized Peripheral Component Interconnect (PCI) bus transaction data;

wherein each of the computer modules operates fully independent of each other; and wherein the differential signal channel comprises two sets of unidirectional serial channels which transmit data in opposite directions; and wherein one of the computer modules is configured to provide protection against failure of any one of the other computer modules.

52. The computer system of claim 51 wherein the Ethernet controllers of the computer modules are used for sharing peripheral devices residing in the console.

53. The computer system of claim 51 wherein the encoded serial bit stream comprises 10 bit packets.

54. The computer system of claim 51 wherein each of the unidirectional serial channels comprises one or more pairs of differential signal lines.

55. The computer system of claim 51 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

56. A computer system comprising:

a console comprising an Ethernet hub controller, a first coupling site and a second coupling site, the console being an enclosure housing the Ethernet hub controller, the coupling sites, and

a plurality of computer modules, each coupled to one of the coupling sites; each computer module comprising a processing unit,

a main memory coupled to the processing unit,

an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating



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encoded serialized Peripheral Component Interconnect (PCI) bus transaction data to a connector, and an Ethernet controller coupled to the Ethernet hub controller for communication between the computer modules;

wherein each of the computer modules operates fully independent of each other.

57. The computer system of claim 56 wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

58. The computer system of claim 11 wherein the Ethernet controllers of the computer modules are used for sharing peripheral devices residing in the console.

59. The computer system of claim 56 wherein the encoded serial bit stream comprises 10 bit packets.

60. The computer system of claim 56 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

61. A computer system comprising:

a console comprising an Ethernet controller coupled to an external network, a video switch, a first coupling site and a second coupling site, the console being an enclosure housing

the Ethernet controller,

the video switch,

each coupling site, and

a plurality of computer modules, each coupled to one of the coupling sites; each computer module comprising a processing unit,

a main memory coupled to the processing unit,

a graphics controller coupled to the video switch, and an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating encoded serial Peripheral Component Interconnect (PCI) bus transaction data to a connector;

wherein each of the computer modules operates fully independent of each other.

62. The computer system of claim 61 wherein the interface controller couples to a flash memory with PCI configuration information.

63. The computer system of claim 61 further comprises a hard disk drive coupled to the computer module.

64. The computer system of claim 61 wherein the console further houses a power supply that supplies DC power to the Ethernet controller and the computer modules.

65. The computer system of claim 61 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

66. A computer system comprising:

a console comprising a first coupling site and a second coupling site, the console being an enclosure housing a serial communication hub controller,

each coupling site, and

a plurality of computer modules, each coupled to one of the coupling sites; each computer module comprising a processing unit,

a main memory coupled to the processing unit,

a mass storage device storing a security program that provide password protection for the computer module, an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating encoded serial Peripheral Component Interconnect (PCI) bus transaction data to a connector, and

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a communication controller coupled to the serial communication hub controller through the connector of the coupling site for communication between the computer modules;

wherein each of the computer modules operates independent of each other.

67. The computer system of claim 66 wherein the interface controller couples to a flash memory with PCI configuration information.

68. The computer system of claim 66 wherein the hard disk drive is removable while the computer module is in operation.

69. The computer system of claim 66 wherein the encoded serial bit stream comprises 10 bit packets.

70. The computer system of claim 66 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

71. A computer system comprising:

a console comprising a first coupling site, and a second coupling site; the console being an enclosure housing each coupling site,

a serial communication hub controller coupled to an external network, and

a plurality of computer modules, each coupled to one of the coupling sites; each computer module comprising a processing unit,

a main memory coupled to the processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a communication controller coupled to the serial communication controller to support communication with the external network, and

an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating encoded serial Peripheral Component Interconnect (PCI) bus transaction data to a connector;

wherein each of the computer modules operates fully independent of each other; and wherein one of the computer modules can replace another one of the computer modules in operation.

72. The computer system of claim 71 wherein the interface controller couples to a flash memory with PCI configuration information.

73. The computer system of claim 71 further comprises a hard disk drive coupled to the computer module.

74. The computer system of claim 71 wherein the serial bit stream comprises 10 bit packets.

75. The computer system of claim 71 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

76. A computer system comprising:

a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being a first enclosure housing each coupling site, and

a plurality of computer modules, each coupled to one of the coupling sites through the connector and the slot; each computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

an interface controller coupled to a differential signal channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and



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wherein each of the computer modules operates fully independent of each other; and wherein the differential signal channel comprises two sets of unidirectional serial channels which transmit 10 bit packets in opposite directions.

77. The computer system of claim 76 wherein the interface controller couples to a flash memory with PCI configuration information.

78. The computer system of claim 76 wherein each of the unidirectional serial channels comprises one or more pairs of differential signal lines.

79. The computer system of claim 76 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

80. The computer system of claim 76 wherein the console further houses a power supply that supplies DC power to the Ethernet controller and the computer modules.

81. A computer system comprising:

a console comprising an Ethernet controller coupled to an external network, a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing the Ethernet controller, each coupling site, and

a plurality of computer modules, each coupled to one of the coupling sites through the connector and the slot; each computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a SCSI hard disk drive, and

an interface controller coupled to a differential signal channel for communicating encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction;

wherein each of the computer modules operates independent of each other; and wherein the differential signal channel couples to the console through the connector of the coupling site; and wherein the encoded serial bit stream transmits 10 bit packets.

82. The computer system of claim 81 wherein the interface controller couples to a flash memory with PCI configuration information.

83. The computer system of claim 81 wherein the SCSI hard disk drive is removable while the computer module is in operation.

84. The computer system of claim 81 wherein the console further houses a power supply that supplies DC power to the Ethernet controller and the computer modules.

85. The computer system of claim 81 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

86. A computer system comprising:

a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing each coupling site,

a serial communication controller, and

a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector and the slot; each computer module comprising a processing unit,

a main memory coupled to the processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which

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transmit data in opposite directions for communicating encoded serial, 10 bit packet data stream of Peripheral Component Interconnect (PCI) bus transaction;

wherein each of the computer modules operates independent of each other.

87. The computer system of claim 86 further comprises a hard disk drive coupled to the computer module.

88. The computer system of claim 86 wherein the encoded PCI bus transaction comprises encoded PCI address and data bits.

89. A computer system comprising:

a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing each coupling site, and

a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector and the slot; each computer module comprising a processing unit,

a main memory coupled to the processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a mass storage device coupled to the processing unit,

an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating encoded serial, 10 bit packet data stream of Peripheral Component Interconnect (PCI) bus transaction; and

wherein each of the computer modules operates independent of each other; and wherein one of the computer modules can replace another one of the computer modules in operation.

90. The computer system of claim 89 wherein the encoded PCI bus transaction comprises encoded PCI address and data bits.

91. The computer system of claim 89 wherein each of the unidirectional serial differential signal channels comprises one or more pairs of differential signal lines.

92. A computer system comprising:

a console comprising a first coupling site and a second coupling site, the console being an enclosure housing each coupling site, and

more than two computer modules; each computer module coupled to one of the coupling sites; each computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a flash memory device configured to store a password for controlling access to the computer module,

a mass storage device coupled to the processing unit,

an interface controller coupled to a differential signal channel of two unidirectional serial bit streams which transmit data in opposite directions for communicating encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction to a connector; and

wherein each of the computer modules operates independent of each other; and wherein one of the computer modules is configured to provide protection against failure of any one of the other computer modules.

93. The computer system of claim 92 wherein the encoded PCI bus transaction comprises encoded PCI address and data bits.

94. The computer system of claim 92 wherein each of the unidirectional serial differential signal channels comprises one or more pairs of differential signal lines.

\* \* \* \* \*



US007363416C1

(12) **INTER PARTES REEXAMINATION CERTIFICATE** (471st)**United States Patent****Chu**(10) **Number:** **US 7,363,416 C1**(45) **Certificate Issued:** **\*Oct. 11, 2012**(54) **COMPUTER SYSTEM UTILIZING MULTIPLE COMPUTER MODULES WITH PASSWORD PROTECTION**(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)(73) Assignee: **ACQIS LLC**, McKinney, TX (US)**Reexamination Request:**

No. 95/001,476, Oct. 27, 2010

**Reexamination Certificate for:**

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 Appl. No.: **11/124,851**  
 Filed: **May 4, 2005**

(\*) Notice: This patent is subject to a terminal disclaimer.

**Related U.S. Application Data**

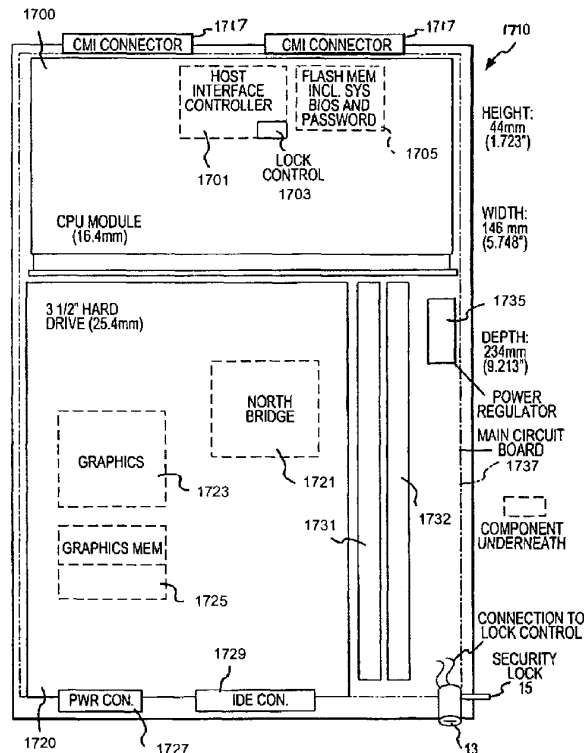
- (63) Continuation of application No. 11/097,694, filed on Mar. 31, 2005, now Pat. No. 7,363,415, which is a continuation of application No. 10/772,214, filed on Feb. 3, 2004, now Pat. No. 7,099,981, which is a continuation of application No. 09/569,758, filed on May 12, 2000, now Pat. No. 6,718,415.
- (60) Provisional application No. 60/134,122, filed on May 14, 1999.

(51) **Int. Cl.**  
**G06F 13/20** (2006.01)(52) **U.S. Cl.** ..... **710/313; 709/227; 710/301; 710/315**(58) **Field of Classification Search** ..... None  
See application file for complete search history.(56) **References Cited**

To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 95/001,476, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

*Primary Examiner* — Majid Banankhah(57) **ABSTRACT**

A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.



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**1**  
**INTER PARTES**  
**REEXAMINATION CERTIFICATE**  
**ISSUED UNDER 35 U.S.C. 316**

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

**2**  
AS A RESULT OF REEXAMINATION, IT HAS BEEN  
DETERMINED THAT:  
The patentability of claims ~~4-94~~ is confirmed.  
5 Claims ~~1-3~~ are cancelled.

\* \* \* \* \*



US007818487B2

(12) **United States Patent**  
**Chu**

(10) **Patent No.:** **US 7,818,487 B2**

(45) **Date of Patent:** **\*Oct. 19, 2010**

(54) **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD USING DIFFERENTIAL SIGNAL CHANNEL INCLUDING UNIDIRECTIONAL, SERIAL BIT CHANNELS**

(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)

(73) Assignee: **ACQIS LLC**, McKinney, TX (US)

(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(21) Appl. No.: **12/378,197**

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(63) Continuation of application No. 12/077,503, filed on Mar. 18, 2008, which is a continuation of application No. 11/166,656, filed on Jun. 24, 2005, now Pat. No. 7,376,779, which is a continuation of application No. 11/097,694, filed on Mar. 31, 2005, now Pat. No. 7,363,415, which is a continuation of application No. 10/772,214, filed on Feb. 3, 2004, now Pat. No. 7,099,981, which is a continuation of application No. 09/569,758, filed on May 12, 2000, now Pat. No. 6,718,415.

(60) Provisional application No. 60/134,122, filed on May 14, 1999.

(51) **Int. Cl.**  
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(52) **U.S. Cl.** ..... **710/313; 710/301; 710/315; 709/227**

(58) **Field of Classification Search** ..... **710/300-317, 710/62-64, 72-74; 709/214-219, 226-27, 709/227; 714/43, 44, 11, 13; 708/1, 2**

See application file for complete search history.

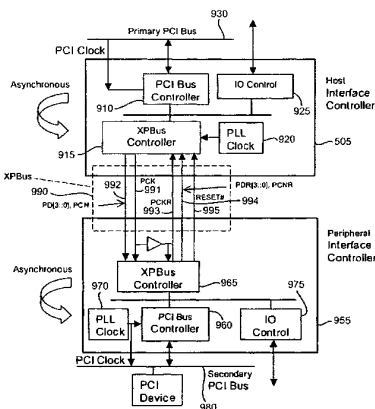
*Primary Examiner*—Raymond N Phan

(74) *Attorney, Agent, or Firm*—Cooley LLP

(57) **ABSTRACT**

A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

**58 Claims, 24 Drawing Sheets**



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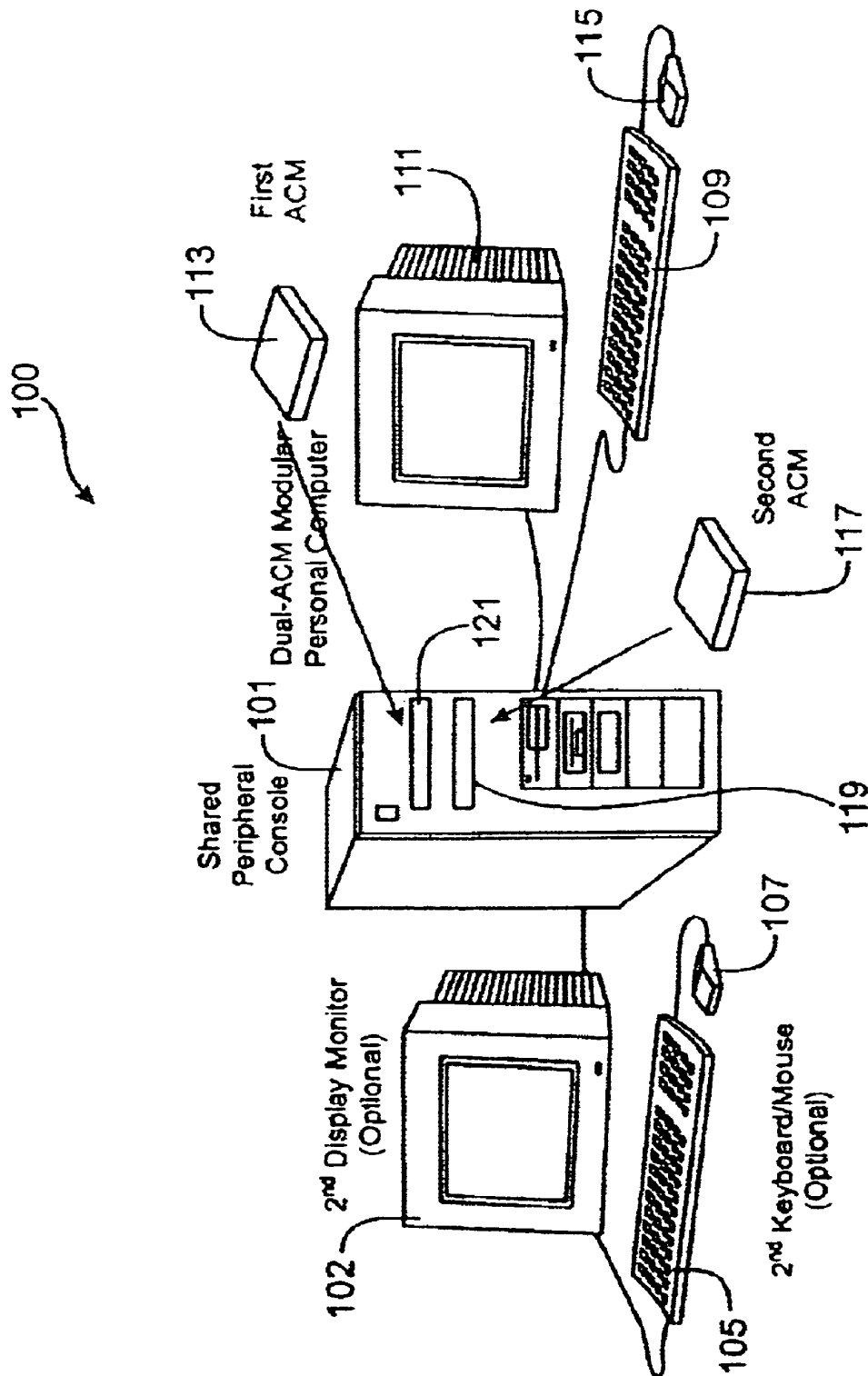


FIGURE 1

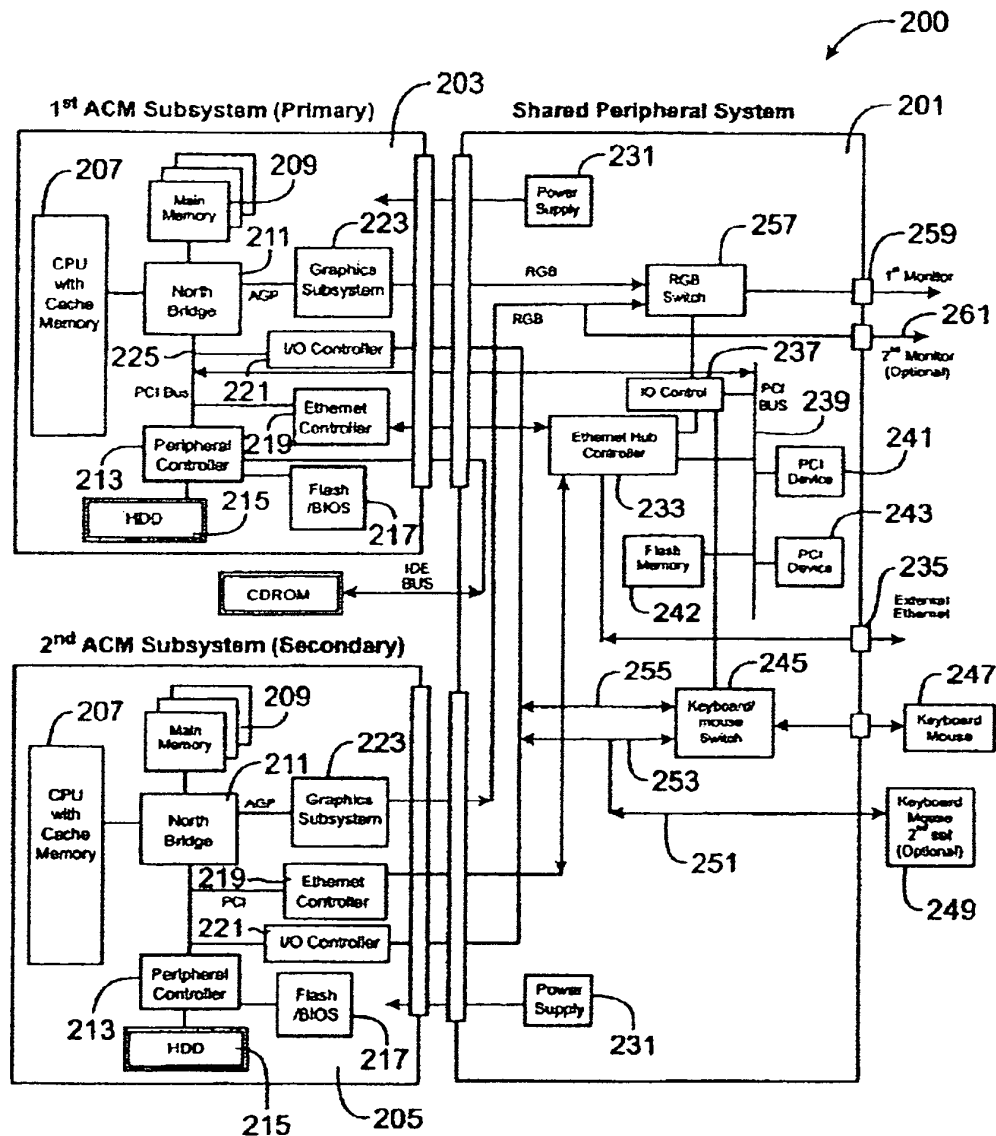


FIGURE 2

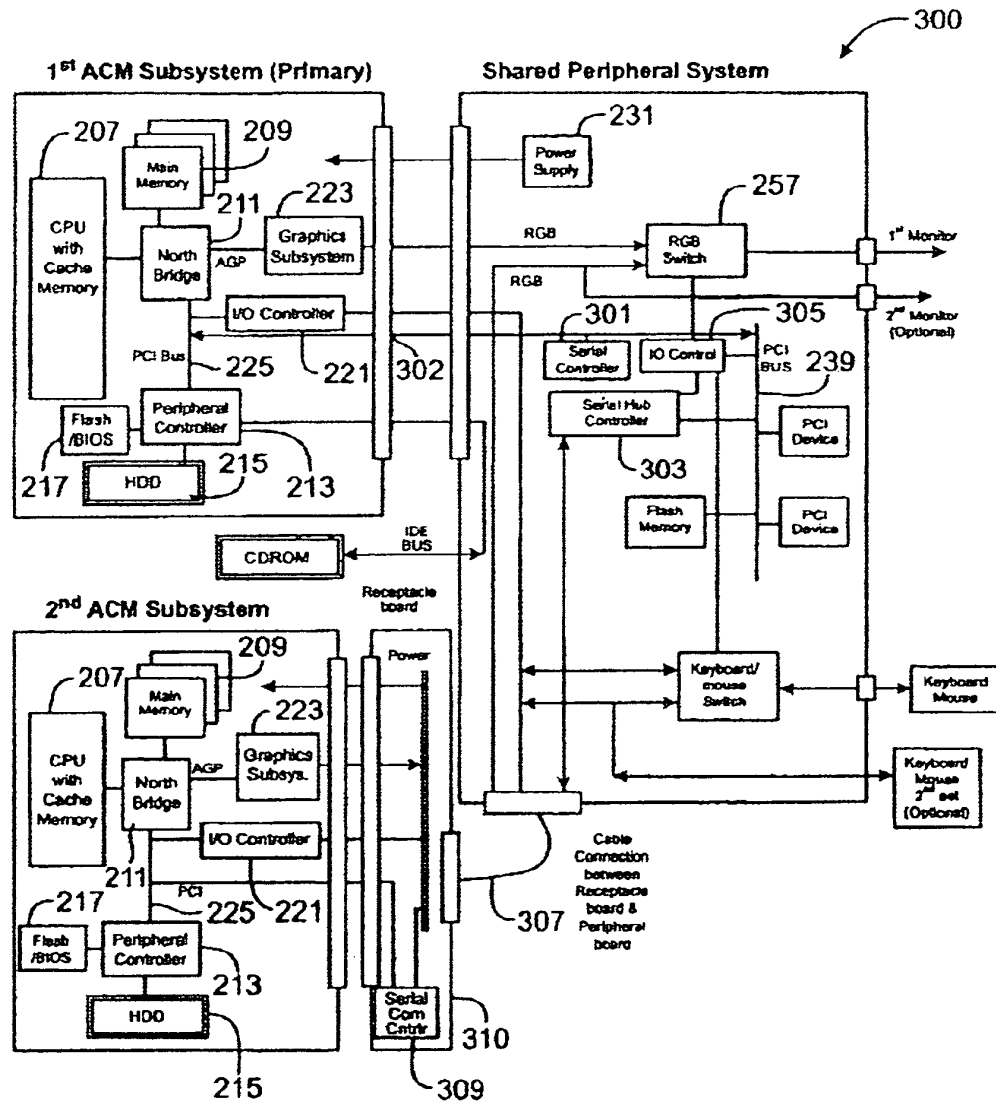


FIGURE 3

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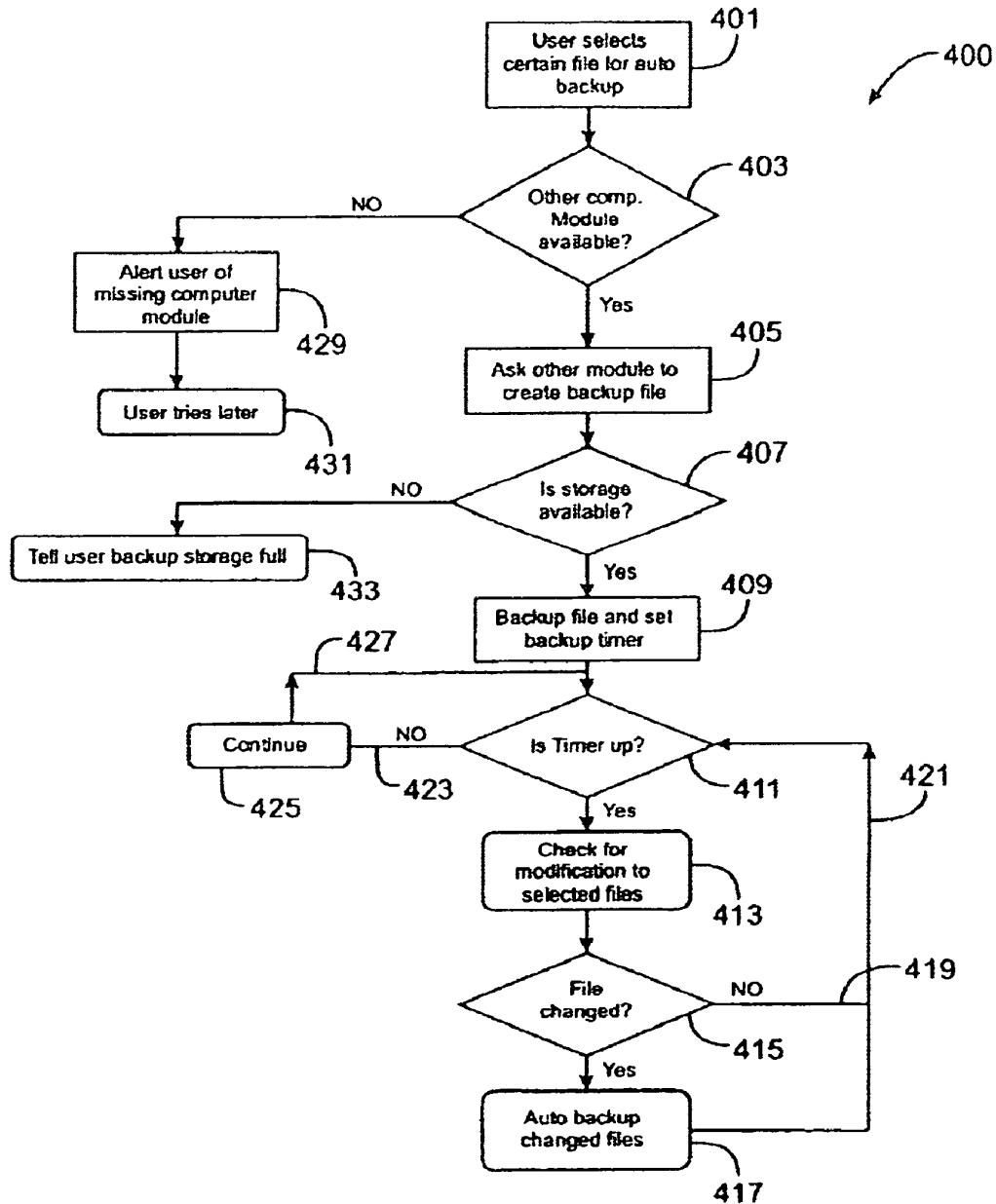


FIGURE 4

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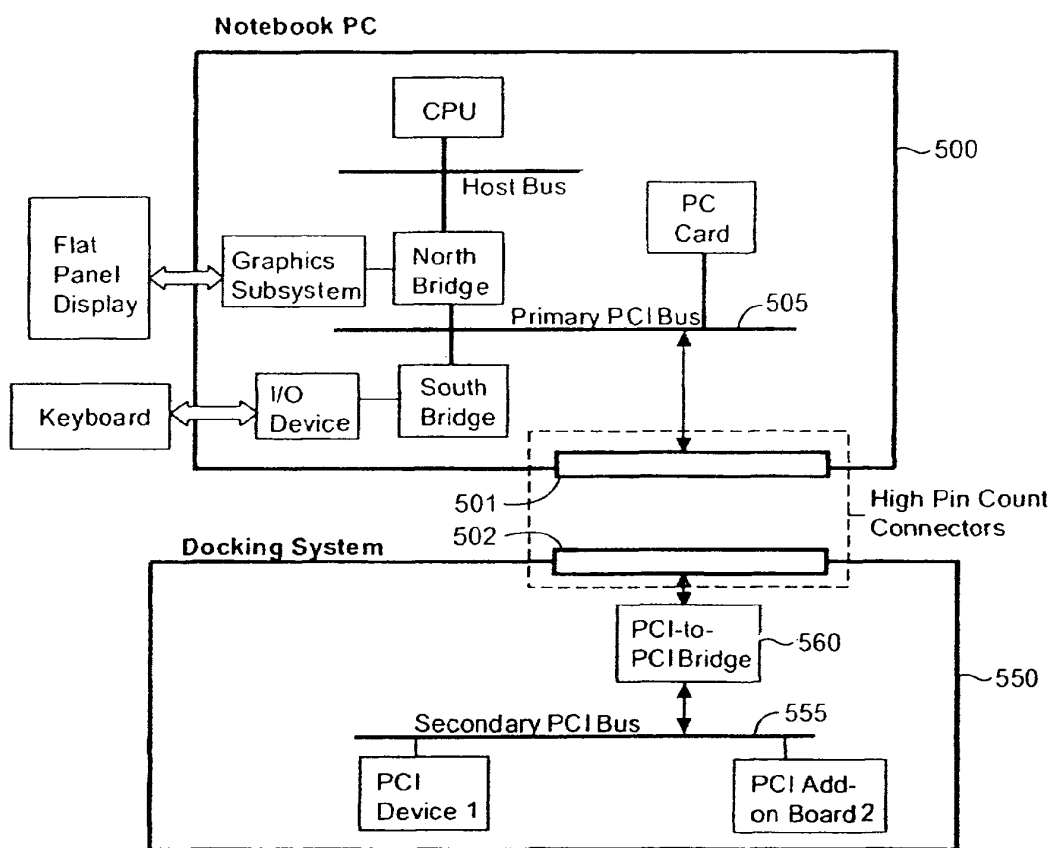


FIGURE 5

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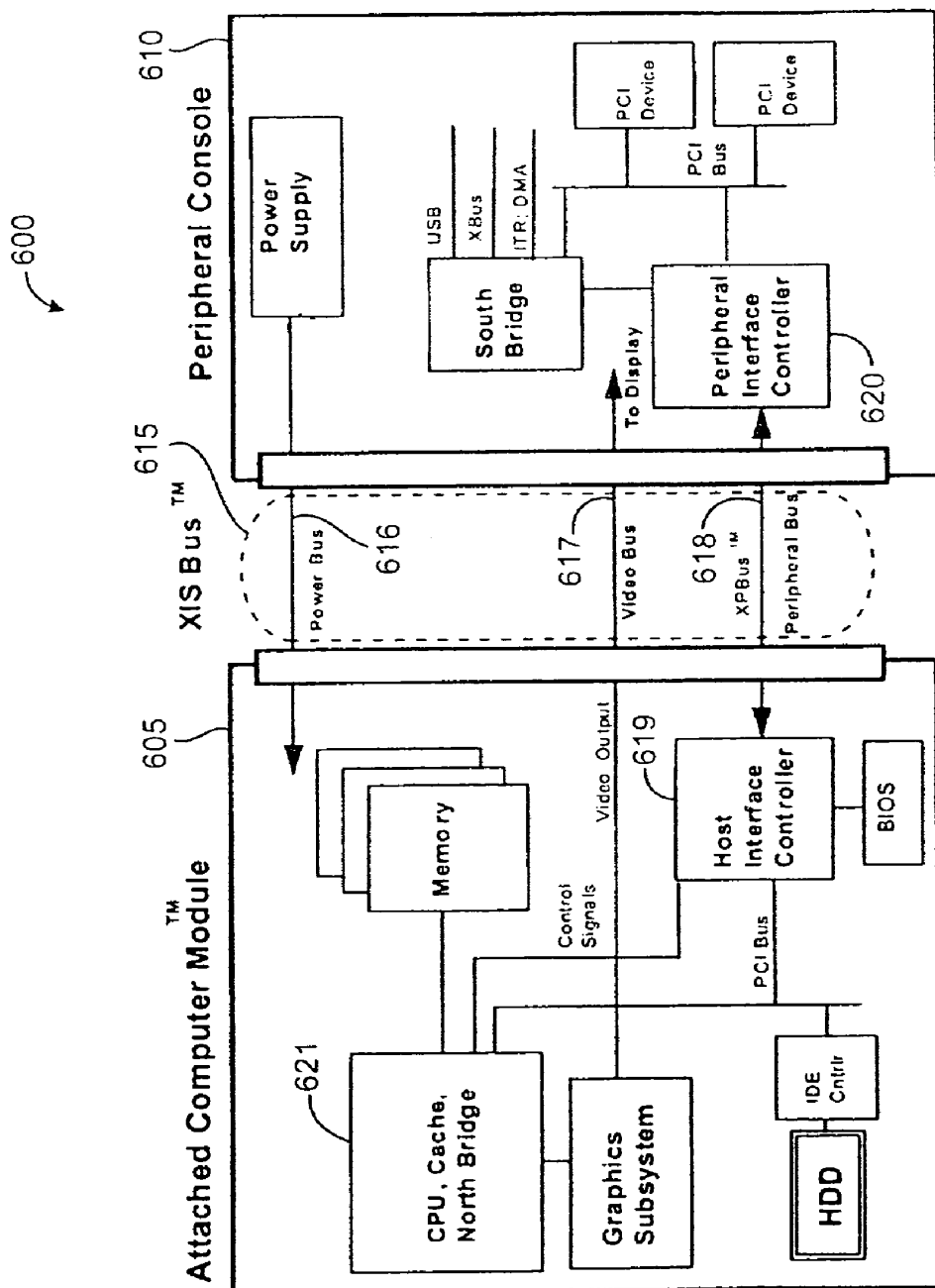


FIGURE 6

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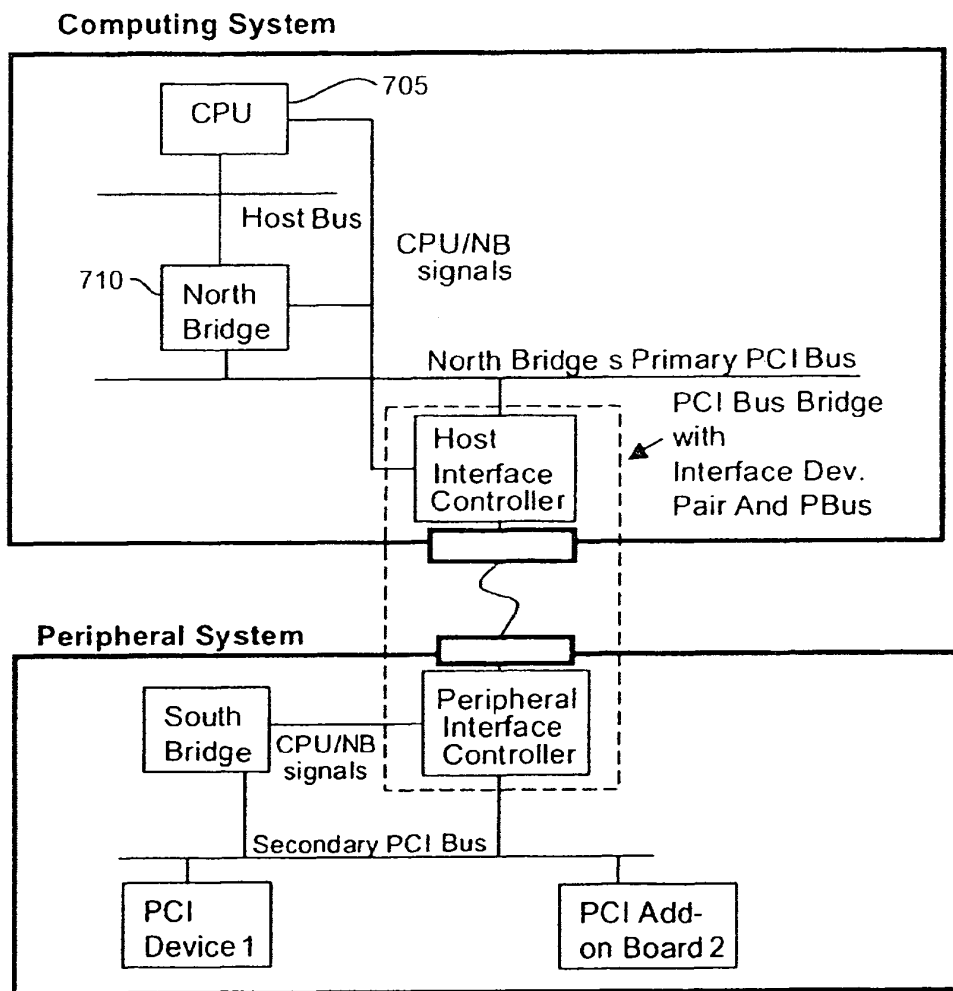


FIGURE 7

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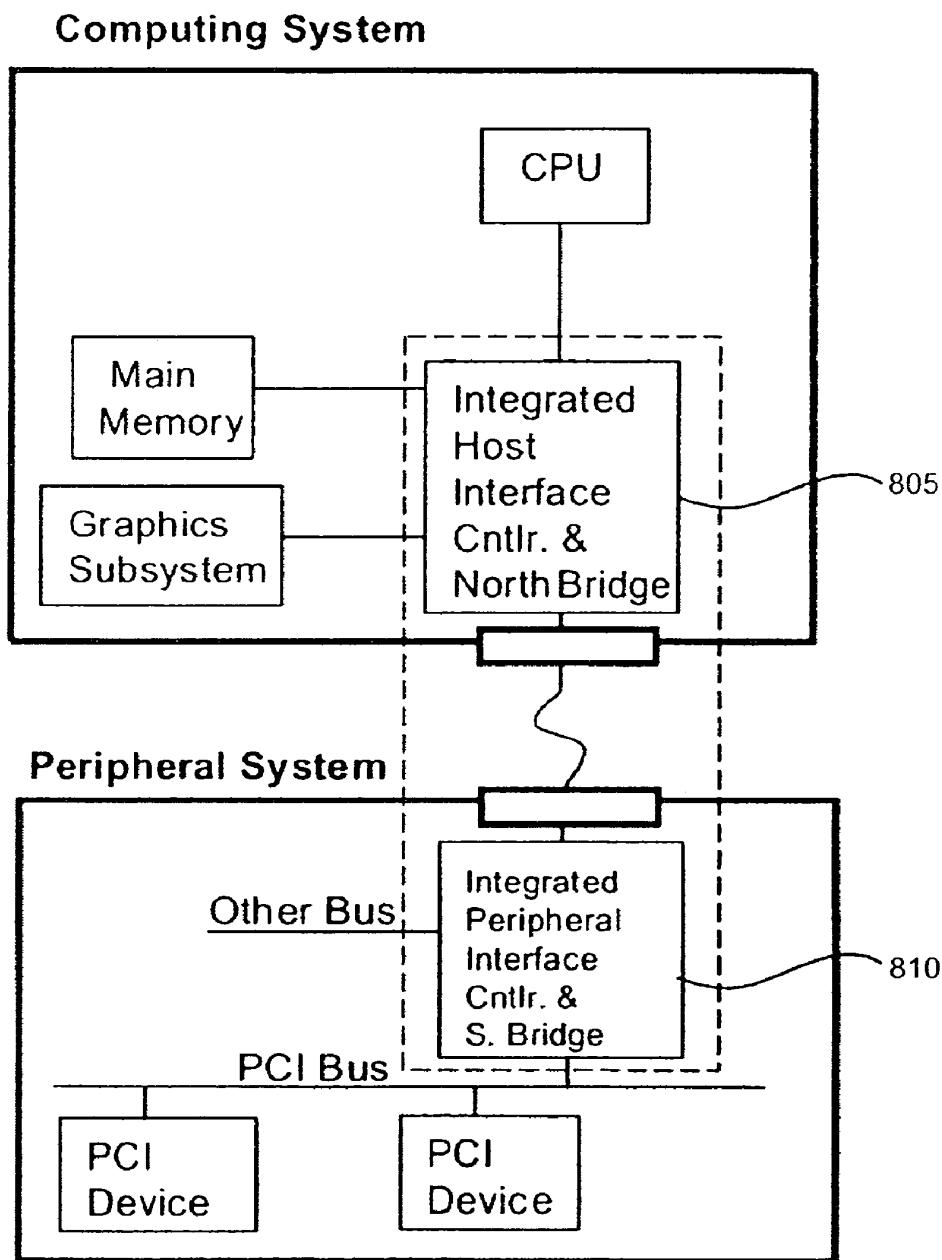


FIGURE 8



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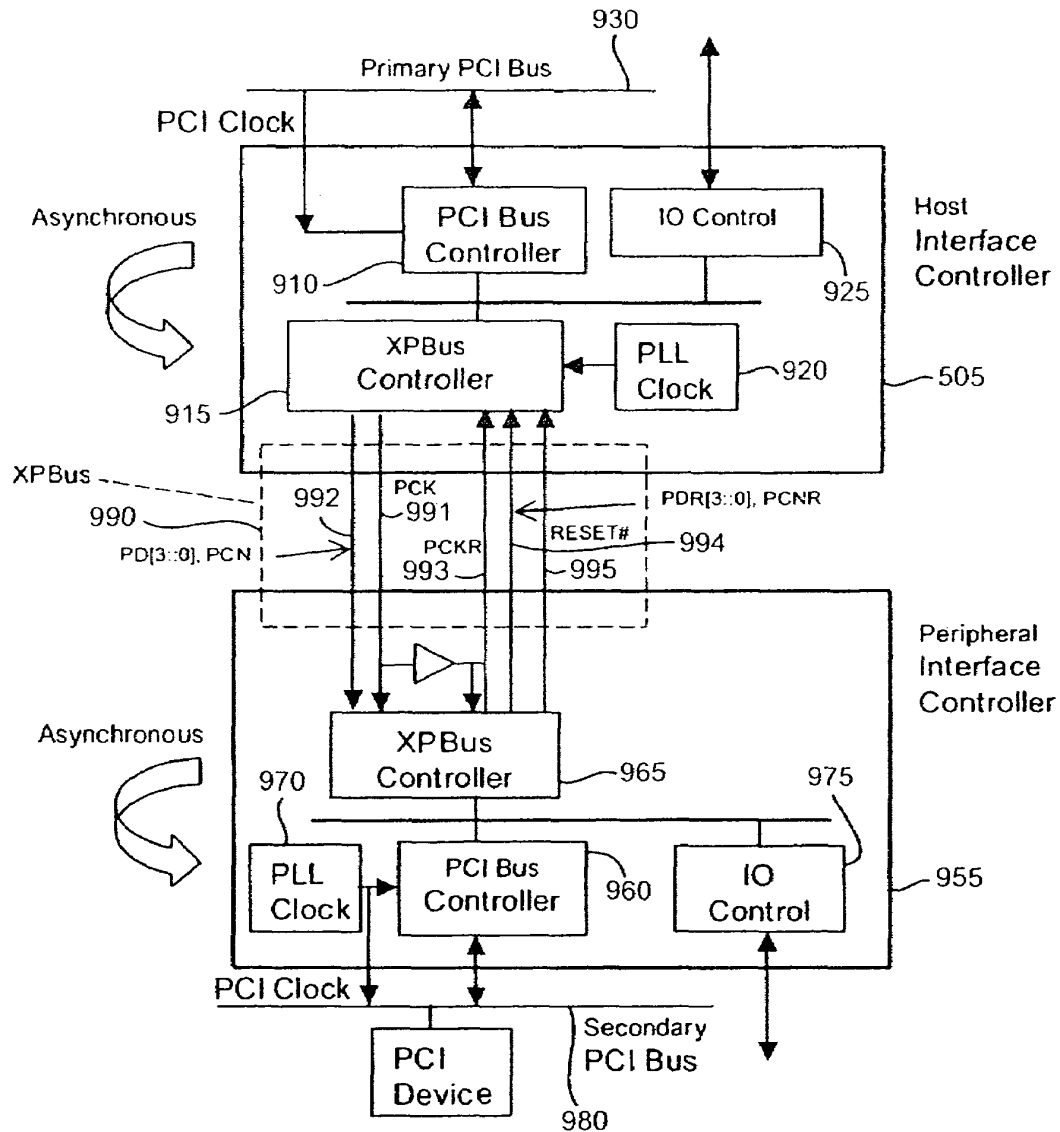


FIGURE 9

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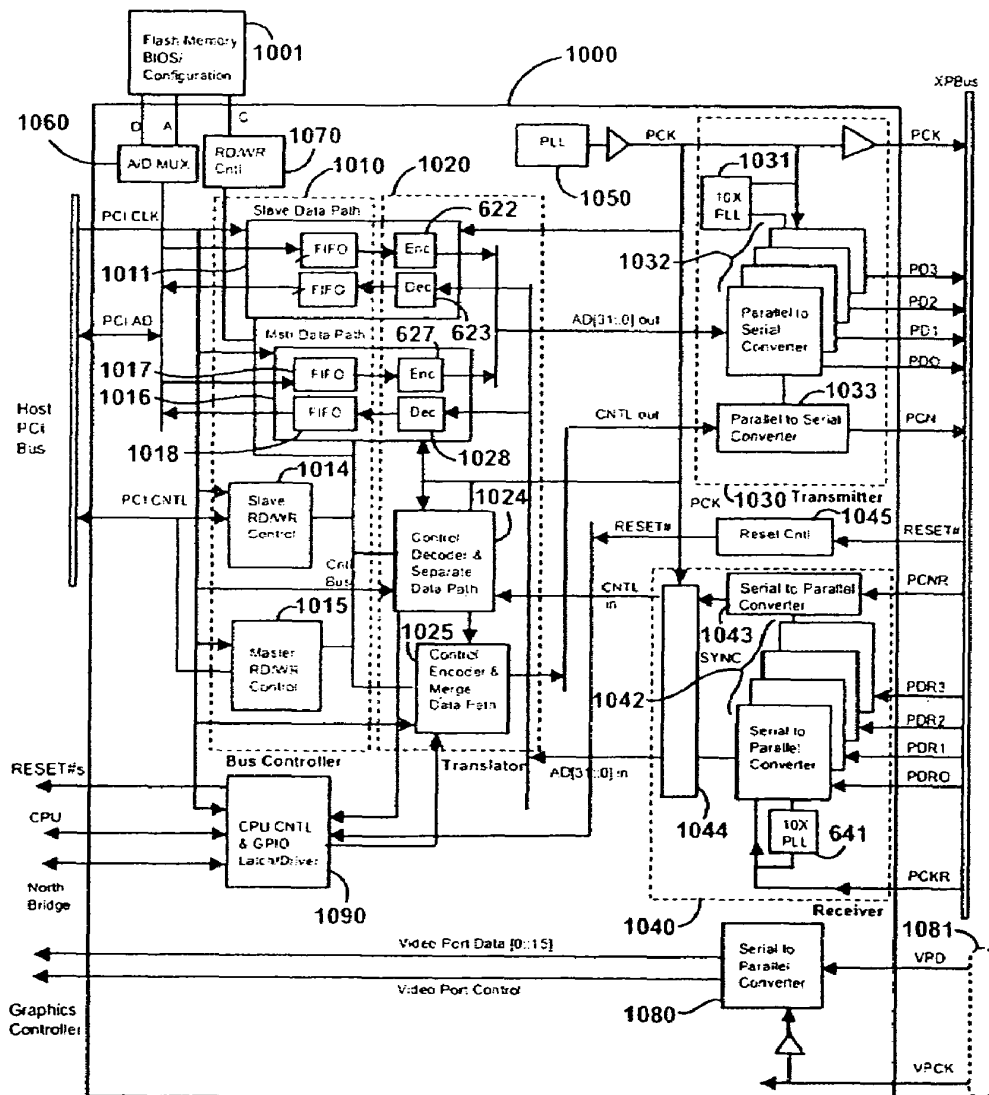


FIGURE 10

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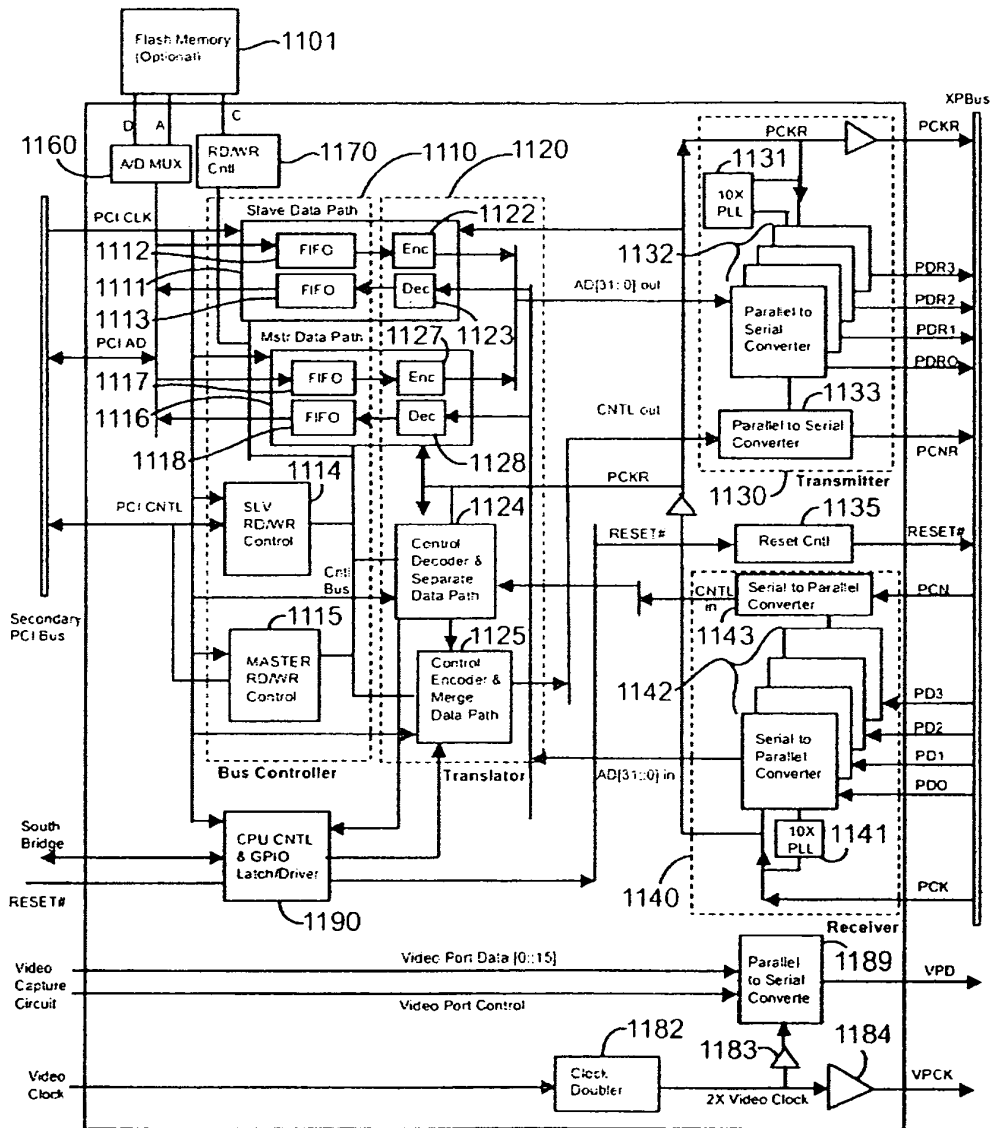


FIGURE 11

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	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 12



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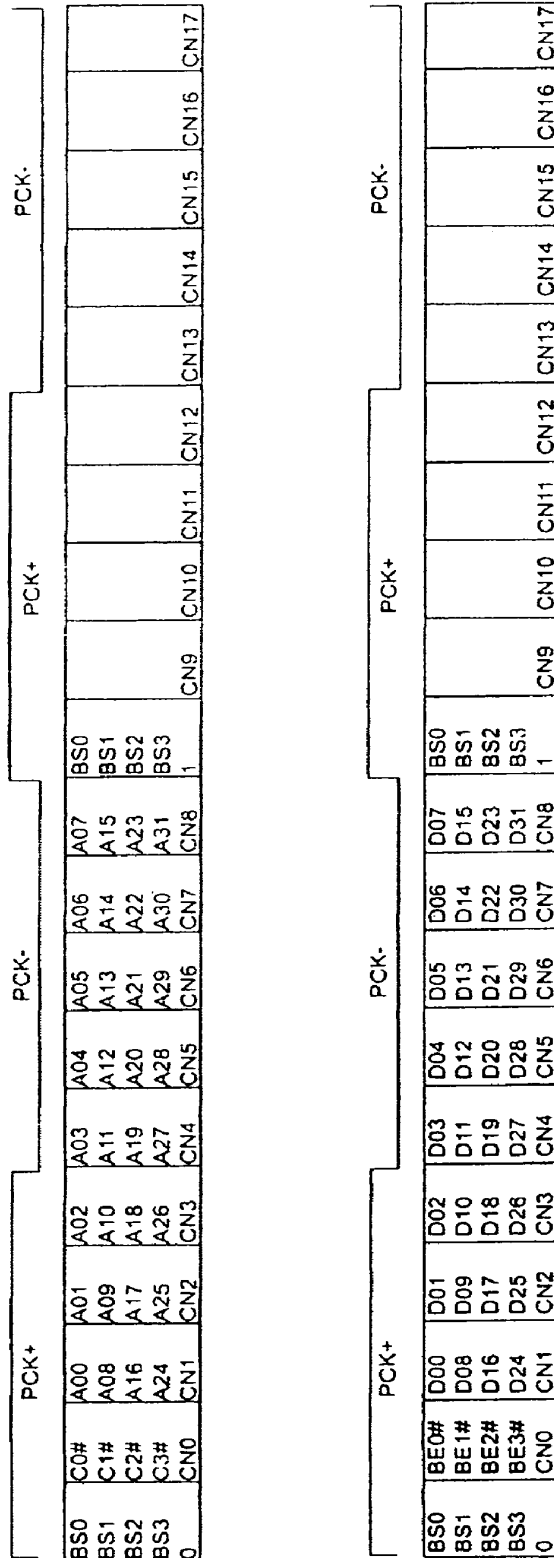


FIGURE 14

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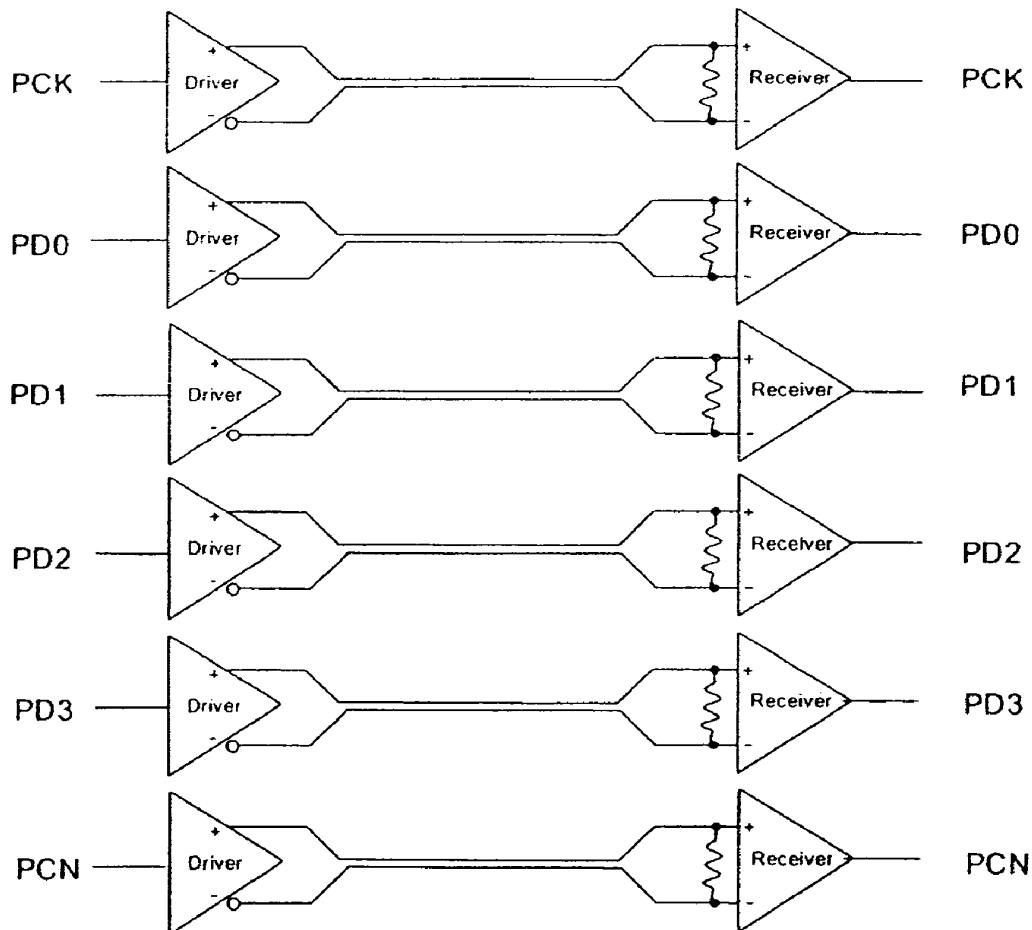


FIGURE 15

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Name	Type	Pins	Description
AD[31:0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3:0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type. C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error, Secondary bus SERR# asserted, Posted write transaction: data parity error on target bus, Posted write transaction discarded, Master abort, Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

FIGURE 16



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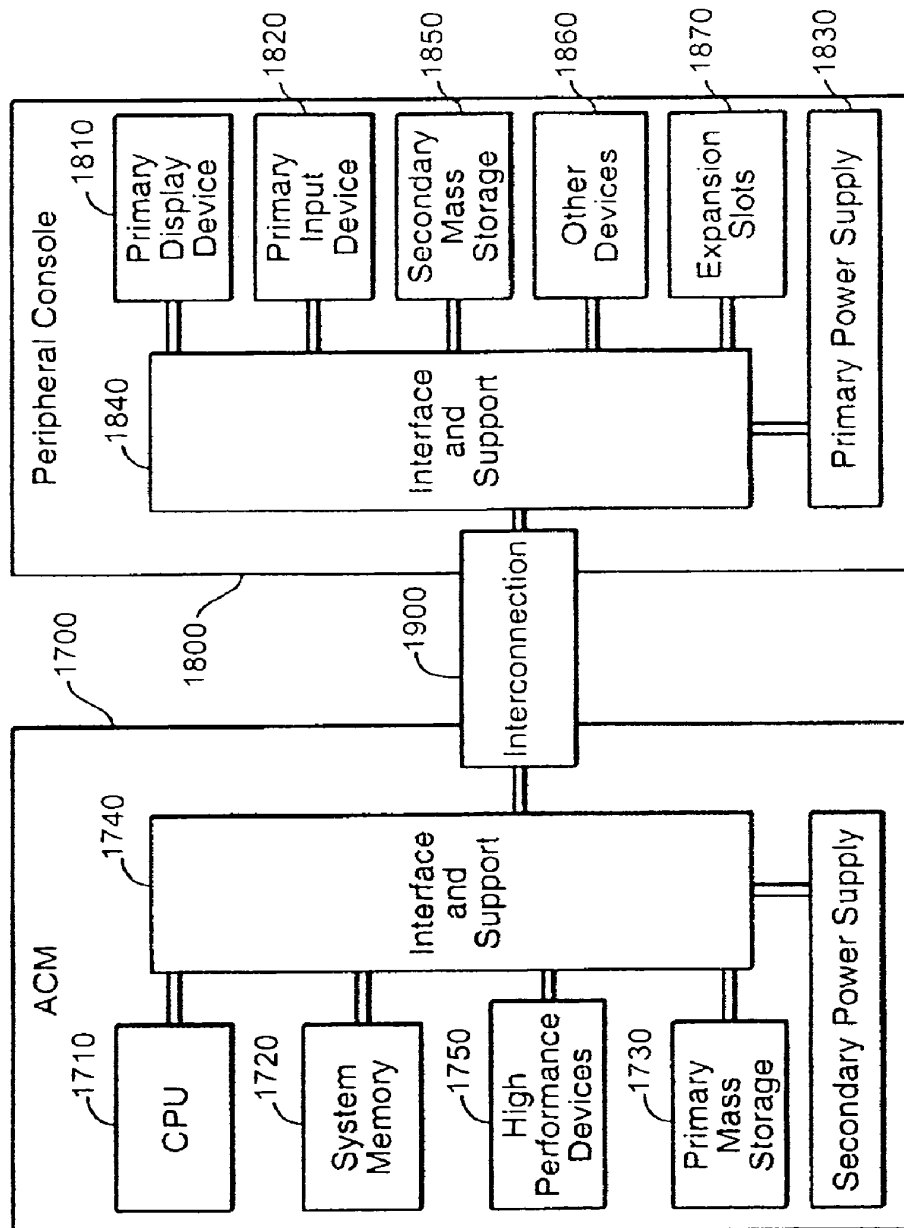


FIGURE 17

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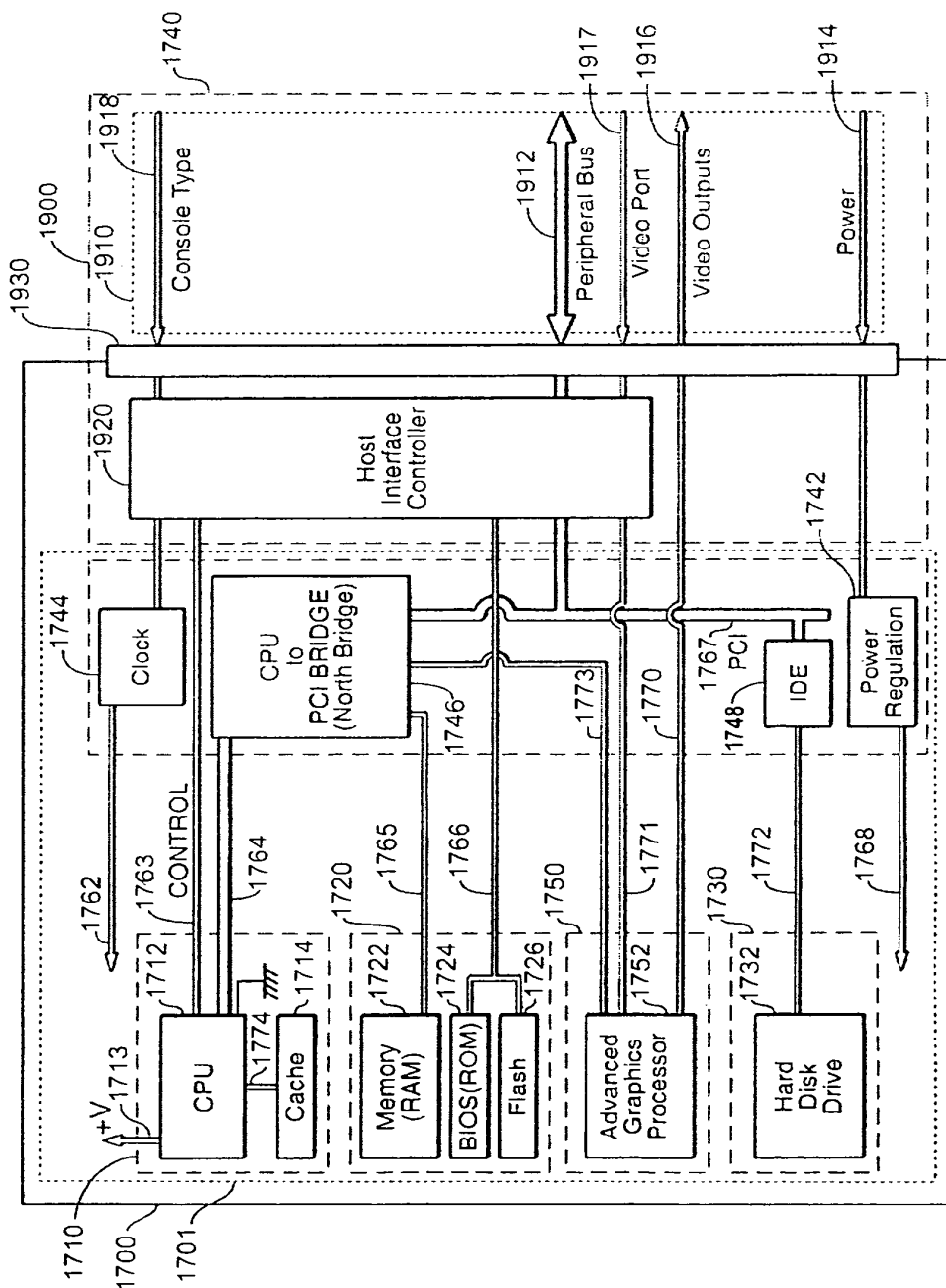


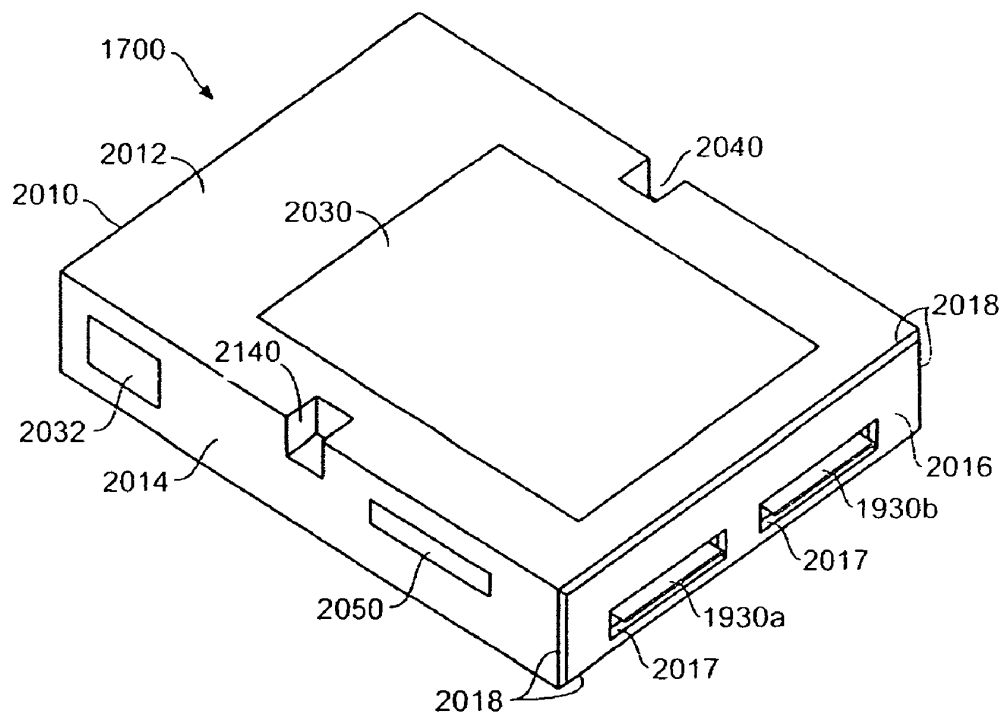
FIGURE 18

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**FIGURE 19**

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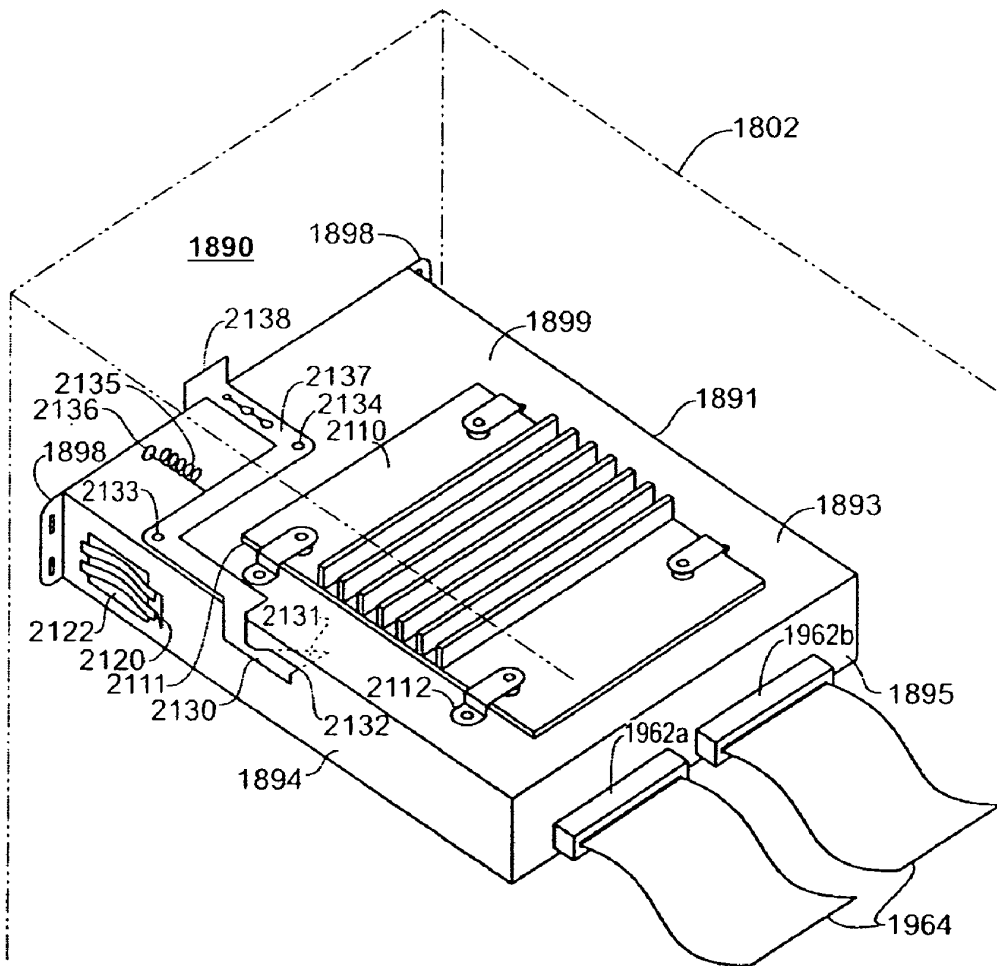


FIGURE 19B

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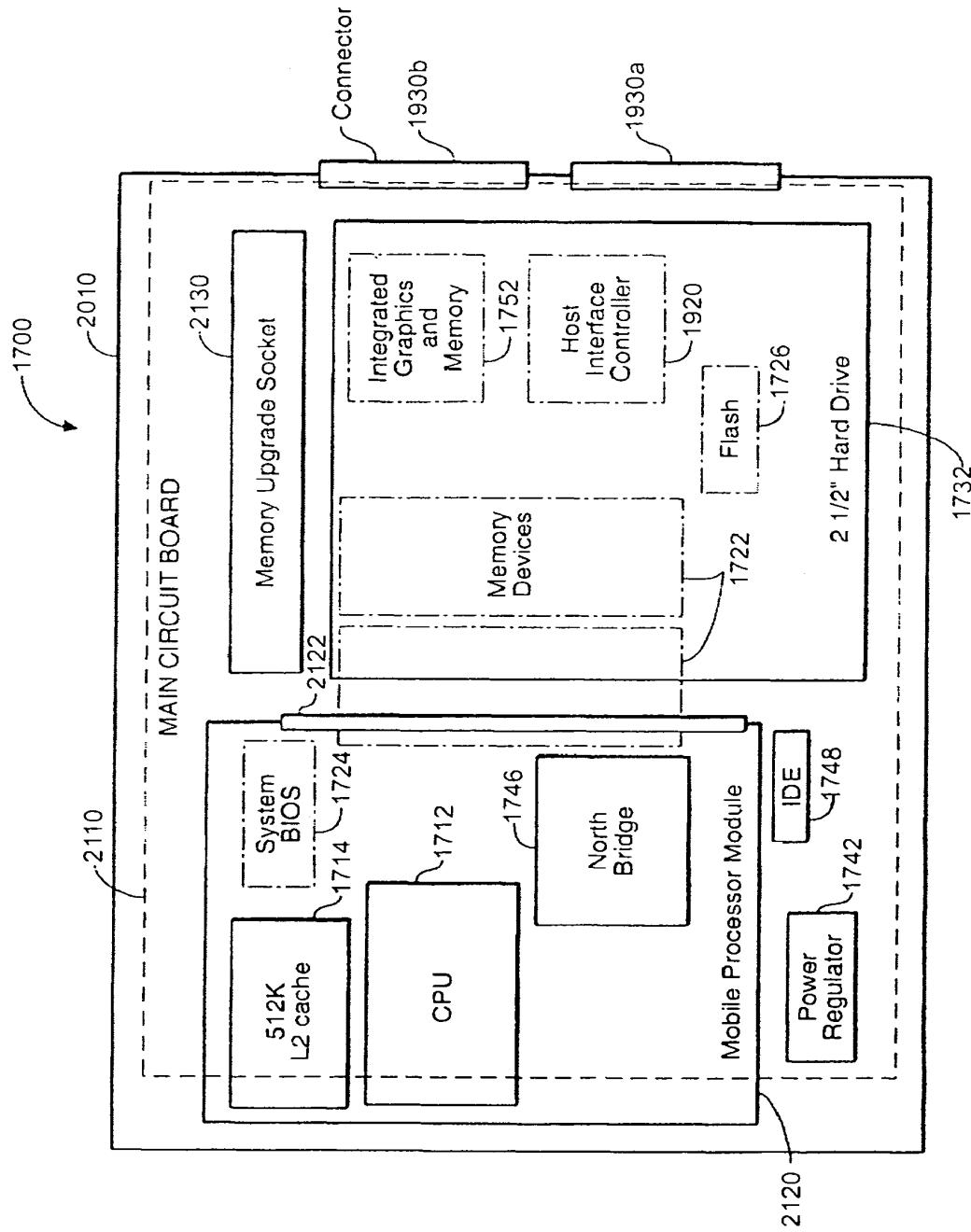


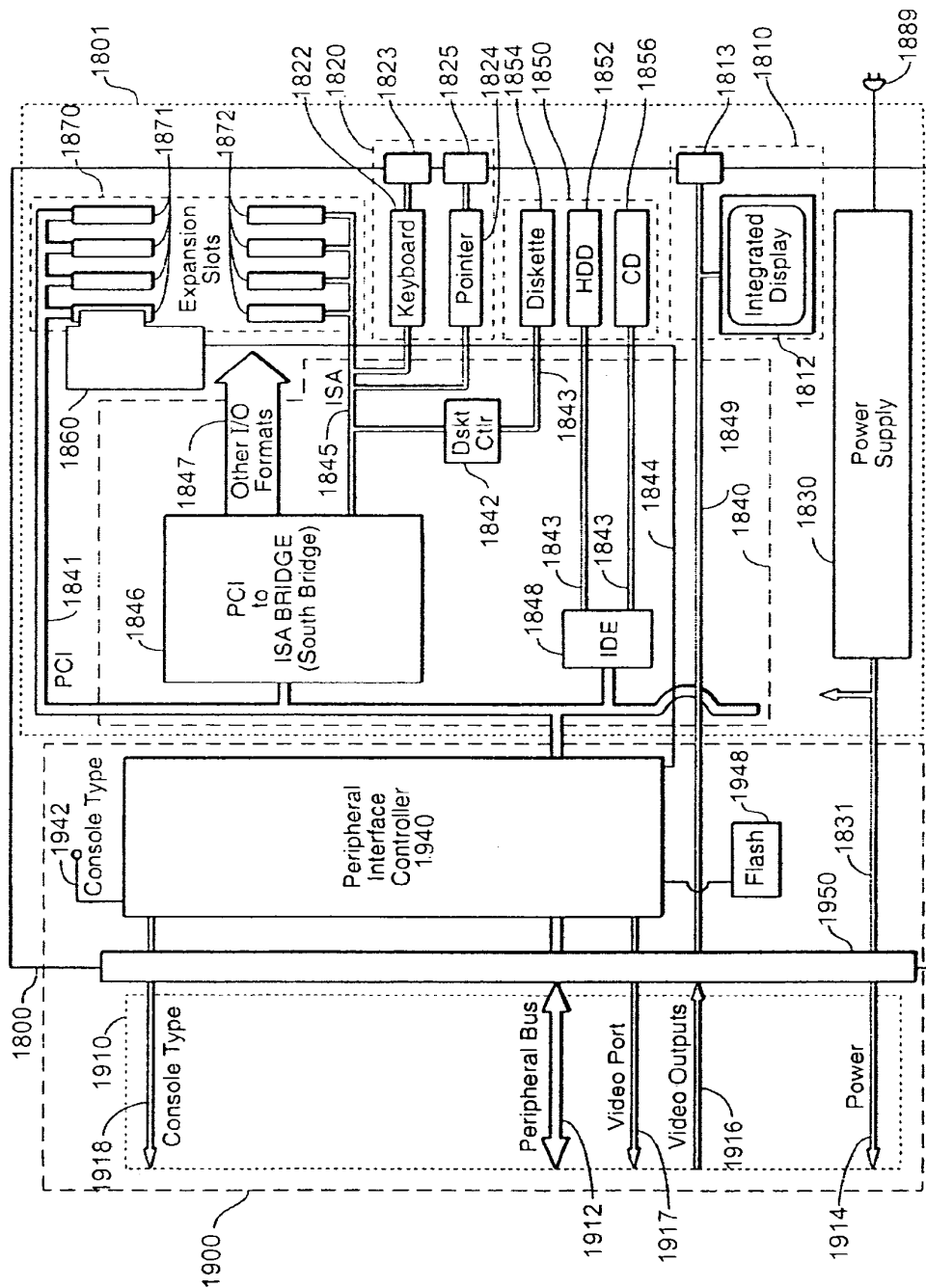
FIGURE 20

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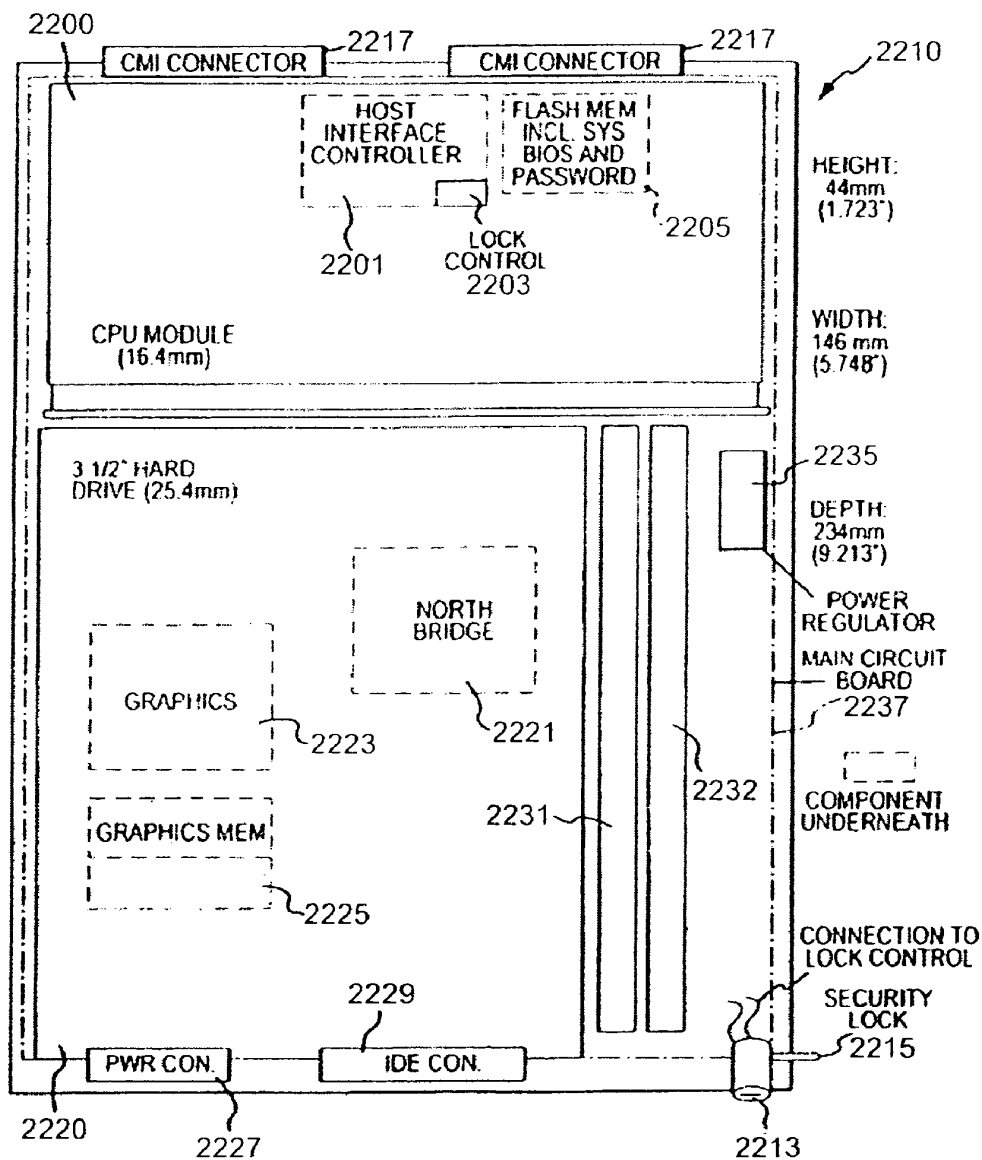


FIGURE 22

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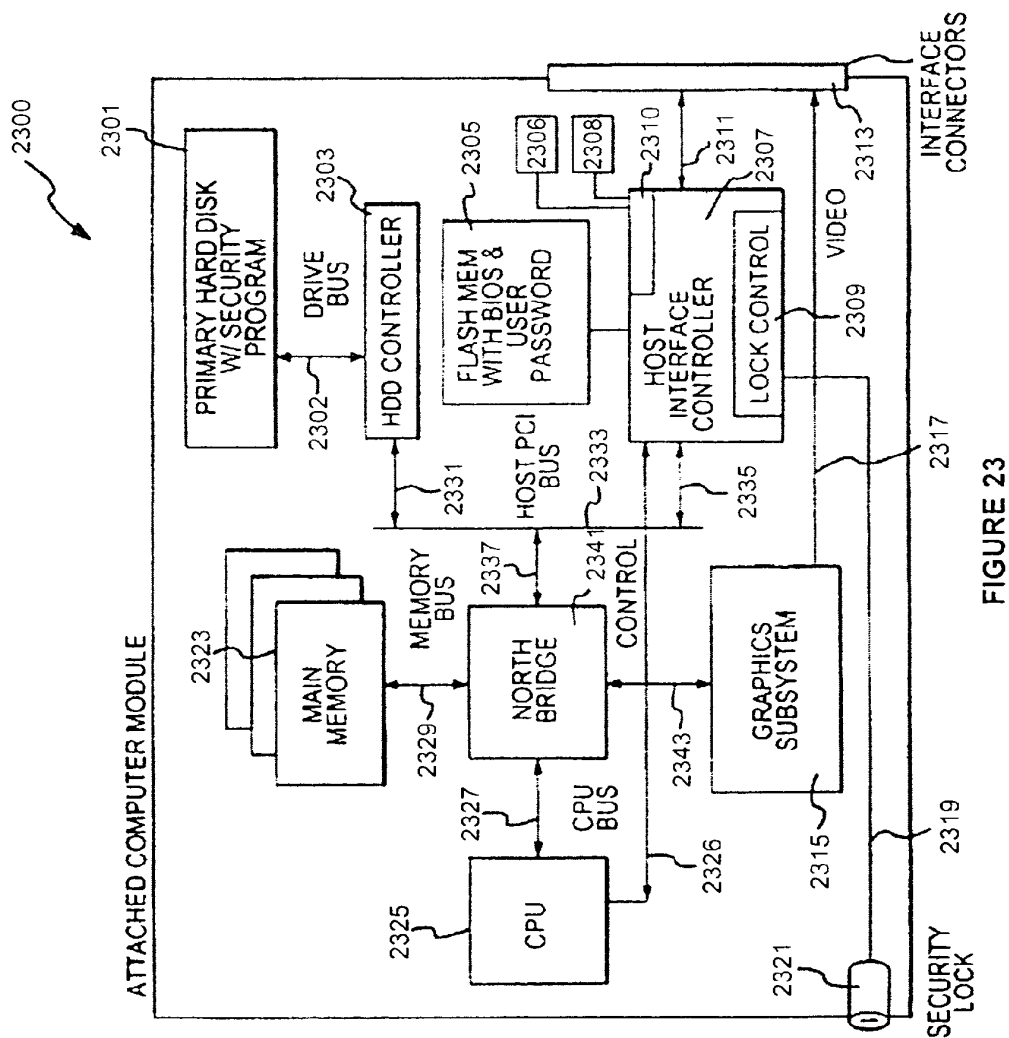


FIGURE 23



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**MULTIPLE MODULE COMPUTER SYSTEM  
AND METHOD USING DIFFERENTIAL  
SIGNAL CHANNEL INCLUDING  
UNIDIRECTIONAL, SERIAL BIT CHANNELS**

**CROSS REFERENCE TO RELATED  
APPLICATIONS**

The present application claims priority as a continuation of U.S. nonprovisional application Ser. No. 12/077,503 filed Mar. 18, 2008, which is a continuation of U.S. nonprovisional application Ser. No. 11/166,656, filed Jun. 24, 2005, which is a continuation of U.S. nonprovisional patent application Ser. No. 11/097,694, filed Mar. 31, 2005, which is a continuation of U.S. nonprovisional patent application Ser. No. 10/772,214, filed Feb. 3, 2004, which is a continuation of U.S. nonprovisional patent application Ser. No. 09/569,758, filed May 12, 2000 (Now U.S. Pat. No. 6,718,415), which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999, commonly assigned, and hereby incorporated by reference.

**BACKGROUND OF THE INVENTION**

The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like.

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Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals the are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use.

Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel's slot 1 architecture. For example, two Pentium II cartridges can be plugged into two "slot 1" card slots on a motherboard to form a Dual-processor system. The two CPU's share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.

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The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in FIG. 5. In FIG. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

An interface such as that shown in FIG. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W. Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel. The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

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Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

## BRIEF SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

In still further embodiments, the present invention provides methods of using multiple computer modules.

The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer

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interface bus, where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a pre-determined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a pre-determined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit

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channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identifica-



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tion code is designed to provide a permanent "finger print" on the attached computer module.

In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module ("ACM") into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., flat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

FIG. 3 is a simplified block diagram of a computer system according to a further alternative embodiment of the present invention; and

FIG. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

FIG. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

FIG. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

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FIG. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

FIG. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

FIG. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

FIG. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

FIG. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

FIG. 17 is a block diagram of one embodiment of a computer system employing the present invention.

FIG. 18 is a block diagram of an attached computing module (ACM).

FIG. 19 illustrates an external view of one embodiment of an ACM.

FIG. 19b illustrates one possible embodiment of a computer bay.

FIG. 20 illustrates the internal component layout for one embodiment of an ACM.

FIG. 21 is a block diagram of a peripheral console (PCON).

FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention; and

FIG. 23 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

FIG. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, each ACM 113 includes computer components, as will be described below, including a

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central processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) **121** is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998, commonly assigned, and hereby incorporated by reference for all purposes.

In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs' graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly, input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be used for the primary ACM if a high bandwidth peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

The shared peripheral console has a chassis and a motherboard that connects the following devices:

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- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. RGB monitor,
- 3) Add-on means, e.g. PCI add-on slots,
- 4) Two Computer Module Bays (CMB) with connectors to two ACMs,
- 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
- 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
- 7) Communication device, e.g. modem,
- 8) Power supply, and others.

The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of FIG. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM **203** is connected to PCI peripheral devices in the peripheral console through the PCI bus **225** that passes through the connection between primary ACM **203** and peripheral console **201**. As shown, ACM has a CPU module **207** coupled to the PCI bus through a North Bridge **211**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, peripheral controller **213** is coupled to BIOS/flash memory **217**. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module **215**. Among other elements, the ACM includes north bridge **215**, graphics subsystem **223** (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module **215** is the PCI bus. In a specific embodiment, North Bridge unit **211** often couples to a computer memory **209**, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **215** typically includes a computer operating system, application software

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program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **215** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection.

The ACM also has a network controller, which can be an Ethernet controller **219**, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub **233** in the console, which includes shared peripheral system **201**.

Also shown is the second ACM **205**. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM **219** accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g., CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port **235**, which connects to an external network.

The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g., Windows 98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

The Ethernet hub also couples to PCI bus **239**, which connects to PCI devices **241**, **243**, e.g., modem, SCSI controller. A flash memory **242** can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those implementations described in U.S. Ser. No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub **233** also couples to an I/O control **237**, which connects to keyboard/mouse switch **245**, which couples to keyboard/mouse **247**. Optionally, the keyboard/mouse switch also couples to a second keyboard/house **259** via PS2 or USB signal line **251**. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller **221** in each ACM via lines **253**, **255**. The I/O control **237** also

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couples to an RGB switch **257**, which allows video signals to pass to the first monitor **259**. Alternatively, the RGB switch couples to a second monitor **261**. The RGB switch includes analog video switches such as MAXIM's MAX4545.

The peripheral system **201** also has an independent power supply **231** for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 3 is a simplified block diagram **300** of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this FIG. as the previous FIGS. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous FIG. A primary ACM **203** is connected to PCI peripheral devices in the peripheral console through the PCI bus **225** that passes through the connection between primary ACM **203** and peripheral console **201**. As shown, ACM has a CPU module **207** coupled to the PCI bus through a North Bridge **211**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, peripheral controller **213** is coupled to BIOS/flash memory **217**. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module **215**. Among other elements, the ACM includes north bridge **215**, graphics subsystem **223** (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module **215** is the PCI bus. In a specific embodiment, North Bridge unit **211** often couples to a computer memory **209**, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.



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The hard drive module or mass storage unit **215** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **215** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection.

The ACM also has a network controller, which can be coupled to a serial port **302**, which is coupled to the PCI bus in the ACM. The serial port is coupled to the peripheral console through a serial controller **301** in the serial console. The serial controller is connected to PCI bus **239**. The serial controller is also coupled to a serial hub controller **303**, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board **310** is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection **307** to the peripheral board **300**. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

The Dual ACM system can support different usage models:

1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.

2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for

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four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting, firewall, etc.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step **401**) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step **403**. If so, the method in the originating module requests the other computer module to create (step **405**) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step **429**. The method then has the user try later **431**, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step **433**) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step **409**), the software in the originating ACM sets a timer to check (step **411**) for file modification via branches **423**, **427** through continue, step **425** process. If a file selected for backup has been modified (step **415**), then the file is automatically back up to the other ACM again, step **417**. Alternatively, the method returns to step **411** through branch **421**.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 6 is a block diagram of one embodiment of a computer system **600** using the interface of the present invention. Computer system **600** includes an attached computer module (ACM) **605** and a peripheral console **610**, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference. The ACM **605** and the peripheral console **610** are interfaced through an exchange interface system (XIS) bus **615**. The XIS bus **615** includes power bus **616**, video bus **617** and peripheral

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bus (XPBus) **618**, which is also herein referred to as an interface channel. The power bus **616** transmits power between ACM **605** and peripheral console **610**. In a preferred embodiment power bus **616** transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts Video bus **617** transmits video signals between the ACM **605** and the peripheral console **610**. In a preferred embodiment, the video bus **617** transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus **618** is coupled to host interface controller (HIC) **619** and to peripheral interface controller (PIC) **620**, which is also sometimes referred to as a bay interface controller.

In the embodiment shown in FIG. 6, HIC **619** is coupled to an integrated unit **621** that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 7, the CPU **705** and north bridge **710** are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 8, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit **805** includes an HIC and a north bridge, while integrated PIC and south bridge unit **810** includes a PIC and a south bridge.

FIG. 9 is a more detailed block diagram of one embodiment of an HIC **905** and a PIC **955** of the present invention. HIC **905** includes a peripheral component interconnect (PCI) bus controller **910**, an XPBus controller **915**, a phase lock loop (PLL) clock **920** and an input/output (IO) control **925**. Similarly, PIC **955** includes a PCI bus controller **960**, an XPBus controller **965**, a PLL clock **970** and an IO control **975**. PCI bus controllers **910** and **960** are coupled to the primary and secondary PCI buses **930** and **980**, respectively, and manage PCI transactions on the primary and secondary PCI buses **930** and **980**, respectively. Similarly, XPBus Controllers **915** and **965** are coupled to XPBus **990**. XPBus controller **915** drives the PCK line **991** and PD[0:3] and PCN lines **992** while XPBus controller **965** drives the PCKR lines **993**, the PDR [0:3] and PCNR lines **994** and the RESET# line **995**.

PCI bus controller **910** receives PCI clock signals from the primary PCI bus **930** and is synchronized to the PCI clock. However, as indicated in FIG. 9, the XPBus controller **915** is asynchronous with the PCI bus controller **910**. Instead, the XPBus controller receives a clock signal from the PLL clock **920** and is synchronized therewith. PLL clock **920** generates a clock signal independent of the PCI clock. The asynchronous operation of the PCI bus and the XPBus allows the PCI Bus to change in frequency, for example as in a power down situation, without directly affecting the XPBus clocking. In the embodiment shown in FIG. 9, the PLL clock **920** generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock **920** generates a clock signal having a frequency of 132 MHz.)

The XPBus **990** operates at the clock speed generated by the PLL clock **920**. Therefore, PCK, the clock signal from the XPBus controller **915** to XPBus controller **965** has the same frequency as the clock signal generated by PLL clock **920**. XPBus controller **965** receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock signal PCKR, the clock signal from the XPBus

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controller **965** to XPBus controller **915**. Accordingly, PCKR also has the same frequency as that generated by the PLL clock **920**. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XPBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

As indicated in FIG. 9, PLL clock **970** is asynchronous with the XPBus controller **965**. Instead, PLL clock **970** independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus **980**. The secondary PCI bus **980** operates at the same clock speed as the primary PCI bus **930**, namely at a frequency of 33 MHz.

FIG. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in FIG. 10, HIC **1000** comprises bus controller **1010**, translator **1020**, transmitter **1030**, receiver **1040**, a PLL **1050**, an address/data multiplexer (A/D MUX) **1060**, a read/write controller (RD/WR Cntl) **1070**, a video serial to parallel converter **1080** and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) **1090**.

HIC **1000** is coupled to an optional flash memory BIOS configuration unit **1001**. Flash memory unit **1001** stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX **1060** and RD/WR Control **1070**, which control the programming, read, and write of flash memory unit **1001**.

Bus controller **1010** is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller **1010** includes a slave (target) unit **1011** and a master unit **1016**. Both slave unit **1011** and master unit **1016** each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit **1016** as well as the two FIFOs in the slave unit **1011** are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit **1011** includes encoder **1022** and decoder **1023**, while master unit **1016** includes encoder **1027** and decoder **1028**. The FIFOs **1012**, **1013**, **1017** and **1018** manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs **1012** and **1017** before they are encoded by encoders **1022** and **1023**. Encoders **1022** and **1023** format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders **1023** and **1028** to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs **1013** and **1018** prior to being transferred to the host PCI bus. FIFOs **1012**, **1013**, **1017** and **1018**, allow bus controller **1010** to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller **1010** also comprises slave read/write control (RD/WR Cntl) **1014** and master read/write control (RD/WR Cntl) **1015**. RD/WR controls **1014** and **1015** are involved in the transfer of PCI control signals between bus controller **1010** and the host PCI bus.

Bus controller **1010** is coupled to translator **1020**. Translator **1020** comprises encoders **1022** and **1027**, decoders **1023**



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and **1028**, control decoder & separate data path unit **1024** and control encoder & merge data path unit **1025**. As discussed above encoders **1022** and **1027** are part of slave data unit **1011** and master data unit **1016**, respectively, receive PCI address and data information from FIFOs **1012** and **1017**, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders **1023** and **1028** are part of slave data unit **1011** and master data unit **1016**, respectively, and format address and data information from receiver **1040** into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit **1025** receives PCI control signals from the slave RD/WR control **1014** and master RD/WR control **1015**. Additionally, control encoder & merge data path unit **1025** receives control signals from CPU CNTL & GPIO latch/driver **1090**, which is coupled to the CPU and north bridge (not shown in FIG. 10). Control encoder & merge data path unit **1025** encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter **1030**, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit **1024** receives control bits from receiver **1040** which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit **1024** separates the control bits it receives from receiver **1040** into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

Transmitter **1030** receives multiplexed parallel address/data (A/D) bits and control bits from translator **1020** on the AD[31::0] out and the CNTL out lines, respectively. Transmitter **1030** also receives a clock signal from PLL **1050**. PLL **1050** takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

The multiplexed parallel A/D bits and some control bits input to transmitter **1030** are serialized by parallel to serial converters **1032** of transmitter **1030** into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter **1033** into 10 bit packets and send out on control line PCN of the XPBus.

A 10x multiplier **1031** receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters **1032** and **1033**. The parallel to serial converters **1032** and **1033** perform bit shifting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters **1032** and **1033** shift bits at 10 times the PCK rate, the bit rate for the serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XPBus is the same as the PCK rate, i.e. 106 MHz. As the PCI buses operate at a clock and bit rate of 33 MHz, the XPBus has a clock rate that

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is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

Receiver **1040** receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver **1040** also receives PCKR on the XPBus as well as the clock signal PCK from PLL **1050**. The synchronizer (SYNC) **1044** of receiver **1040** synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XPBus into PCK clock timing.

Serial to parallel converters **1042** convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders **1023** and **1028** and control decoder and separate data path unit **1024**, respectively. Serial to parallel converter **1043** receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path **1024**.

A 10x multiplier **1041** receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters **1042** and **1043**. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters **1042** and **1043** perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted that the rate at which bit packets are transmitted on the XPBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders **1023** and **1028** by way of the AD[3::0] in line and to control decoder & separate data path unit **1024** by way of CNTL in lines, respectively.

Reset control unit **1045** of HIC **1000** receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit **1045** then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit **1090**.

As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XPBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XPBus is able to interface such PCI buses without backup delays because the XPBus operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver **1090** is responsible for latching input signals from the CPU and north bridge and sending the signals to the translator. It also takes decoded signals from the control decoder & separate data path unit **1024** and drives the appropriate signals for the CPU and north bridge.

In the embodiment shown in FIG. 10, video serial to parallel converter **1080** is included in HIC **1000**. In another embodiment, video serial to parallel converter **1080** may be a separate unit from the HIC **1000**. Video serial to parallel converter **1080** receives serial video data on line VPD and a video clock signal VPCK from line VPCK of video bus **1081**. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in FIG. 10) on the video port data [0::15] and video port control lines, respectively.

HIC **1000** handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. HIC **1000** buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XPBus;

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2. HIC 1000 manages the signal locally; and
3. HIC 1000 receives control bits from XPBus, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

FIG. 11 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1100 is nearly identical to HIC 1000 in its function, except that HIC 1000 interfaces the host PCI bus to the XPBus while PIC 1100 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1100 serve the same function as their corresponding components in HIC 1000. Reference numbers for components in PIC 1100 have been selected such that a component in PIC 1100 and its corresponding component in HIC 1000 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1100 is referenced as bus controller 1110 while the bus controller in HIC 1000 is referenced as bus controller 1010. As many of the elements in PIC 1100 serve the same functions as those served by their corresponding elements in HIC 1000 and as the functions of the corresponding elements in HIC 1000 have been described in detail above, the function of elements of PIC 1100 having corresponding elements in HIC 1000 will not be further described herein. Reference may be made to the above description of FIG. 10 for an understanding of the functions of the elements of PIC 1100 having corresponding elements in HIC 1000.

As suggested above, there are also differences between HIC 1000 and PIC 1100. Some of the differences between HIC 1000 and PIC 1100 include the following. First, receiver 1140 in PIC 1100, unlike receiver 1040 in HIC 1000, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 1000 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1050. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1000. Another difference between PIC 1100 and HIC 1000 is the fact that PIC 1100 contains a video parallel to serial converter 1189 whereas HIC 1000 contains a video serial to parallel converter 1080. Video parallel to serial converter 1189 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0:15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1100, unlike HIC 1000, contains a clock doubler 1182 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1182 through buffer 1183 and is sent to serial to parallel converter 1080 through buffer 1184. Additionally, reset control unit 1135 in PIC 1100 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 1000 whereas reset control unit 1045 of HIC 1000 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1090 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1100 to the HIC 1000.

Like HIC 1000, PIC 1100 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. PIC 1100 buffers clocked control signals from the secondary PCI bus, encodes them and sends the encoded control bits to the XPBus;

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2. PIC 1100 manages the signal locally; and
3. PIC 1100 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

PIC 1100 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

FIG. 12 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

FIG. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In FIG. 13, A00 to A31 represent 32 bits of PCI address A[31:0], D00 to D31 represent 32 bits of PCI data D[31:0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBus, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information in each clock cycle. As shown in FIG. 13, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight A/D bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in FIG. 13 comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31:0] signals, 4 PCI C/BE# [3:0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

In the embodiment shown in FIG. 13, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address transfer, write data transfer, read data transfer, switch XPBus direction, last data transfer, wait, and other cycles.

Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBus between the HIC and the PIC.

FIG. 14 is a table showing the information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus. In this embodiment, the XPBus clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBus cycle. As can be seen in FIG. 14, there are no address or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

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In the embodiment shown in FIG. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XDBus clock cycles. The first bit transmitted on the control line in each XDBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example, BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicate that a PCI bus is used whereas a BS3 value of one may indicate that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

FIG. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 15, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 15 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XDBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XDBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

The XDBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XDBus lines may be IEEE 1394 lines.

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It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIG. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

FIG. 17 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 1710, system memory 1720, high performance devices 1750, primary mass storage 1730, and related interface and support circuitry 1740. The PCON includes primary display 1810, primary input 1820, secondary mass storage 1750, other devices 1860, expansion slots 1870, the primary power supply 1830, and related interface and support circuitry 1840. The interconnection apparatus 1900 includes circuitry to convey power and operational signals between the ACM and PCON.

Within the ACM 1700, the CPU 1710 executes instructions and manipulates data stored in the system memory. The CPU 1710 and system memory 1720 represent the user's core computing power. The core computing power may also include high performance devices 1750 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 1730 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 1740 primarily includes interface chips and signal busses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

Within the PCON 1800, the primary display component 1810 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the



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computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

The primary input component **1820** of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

The PCON may contain secondary mass storage **1850** to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

The PCON may be enhanced with additional capability through the use of integrated "Other Devices" **1860** or add-on cards inserted into the PCON's expansion slots **1870**. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry **1840** primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

Importantly, the PCON houses the primary power supply **1830**. The primary power supply has sufficient capacity to power both the PCON and the ACM **1700** for normal operation. Note that the ACM may include a secondary "power supply" in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

FIG. **18** is a block diagram of an attached computing module (ACM) **1700**. The physical ACM package **1700** contains the ACM functional components **1701** and the ACM side of the ACM-to-PCON Interconnection **1900**. The ACM **1701** comprises a CPU component **1710**, a system memory component **1720**, a primary mass storage component **1730**, a high performance devices components **1750**, and an interface and support component **1740**.

The ACM side of the ACM-to-PCON Interconnection **1900** comprises a Host Interface Controller (HIC) component **1920** and an ACM connector component **1930**. The HIC **1920** and connector **1930** components couple the ACM functional components **1700** with the signals of an ACM-to-PCON interface bus **1910** used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus **1910** comprises conveyance for electrical power **1914** and signals for a peripheral bus **1912**, video **1916**, video port **1917**, and console type **1918**. The preferred ACM-to-PCON Interconnection **1900** is described in detail in a companion U.S. patent application Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," by the same inventor, filed on the same day herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection **1900** includes circuitry to transmit and receive parallel bus information from

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multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection **1900**. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

The CPU component **1710** of the ACM functional circuitry **1701** of the presently described embodiment comprises a microprocessor **1712**, which is the chief component of the personal computer system, power supply connection point **1713**, and cache memory **1714** tightly coupled to the microprocessor **1712** by the CPU-to-cache bus **1714** comprising signal paths for address, data, and control information. The microprocessor **1712** of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor **1712** receives electrical power from power bus **1768** via connection point **1713**. Microprocessor **1712** couples to the Host Interface Controller (HIC) **1920** via CPU-to-HIC bus **1763** comprising signal paths to exchange control information such as an interrupt request. Microprocessor **1712** also couples to CPU Bridge **1746** via CPU main bus **1764** comprising signal paths for address, data, and control information.

The CPU Bridge component **1746** of the interface and support circuitry **1740** operates to couple the high speed CPU main bus **1764** to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge **1746** such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

The system memory component **1720** of the ACM functional circuitry **1701** in the present embodiment comprises main system memory (RAM) **1722**, BIOS memory **1724**, and flash memory **1726**. The system memory **1720** is used to contain data and instructions that are directly addressable by the CPU. The RAM **1722** comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion of total system memory **1720** capacity. The BIOS memory **1724** comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating conditions. The BIOS memory **1724** stores, for example, start-up instructions for the microprocessor **1712** and sets of instructions for rudimentary input/output tasks. The flash memory **1726** comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory **1726** are easily changed under normal operating conditions. The flash memory **1726** may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor **1712**. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

The main system memory (RAM) **1722** is coupled to memory controller circuitry resident within the CPU Bridge **1746** via direct memory bus **1765**. The BIOS **1724** and flash memory **1726** are coupled to HIC **1920** via switched memory bus **1766**. This permits the BIOS **1724** and flash **1726** memories to be accessed by circuitry in the HIC **1920** or other

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circuitry connected thereto. The direct memory bus **1765** and the switch memory bus **1766** each comprises conductors to convey signals for data, address, and control information.

The primary mass storage component **1730** of the ACM functional circuitry **1701** in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) **1732** has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD **1732** in the present embodiment serves as the “boot” device for the personal computer from which the operating system is loaded into RAM **1722** by the start-up program stored in the BIOS **1724**.

The present HDD **1732** has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk **1732** stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user’s identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user’s favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device **1730**.

The HDD **1732** is coupled to IDE controller circuitry **1748** via IDE bus **1772**. The IDE controller circuitry **1748** is coupled to the CPU Bridge **1746** via the Host PCI bus **1767**. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive **1732** to the microprocessor **1712**.

The high performance devices component **1750** of the ACM functional circuitry **1701** in the present embodiment comprises an Advanced Graphics Processor (AGP) **1752**. The Model 740 Graphics Device from Intel Corporation may be used in the present embodiment as the AGP.

Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP **1752** is located in the ACM **1700**, where it is in close proximity to the microprocessor **1712**. The AGP **1752** is coupled to the microprocessor **1712** via the advanced graphics port bus **1773** of the CPU Bridge **1746**. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus **1770**. Video information from a source external to the ACM and appearing as video port signals **1917** may be conveyed to the AGP **1752** via video port signal path **1771**.

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Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today’s CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user’s core computing power and environment in a portable package. This represents a further advantage of the invention.

The interface and support component **1740** of the ACM functional circuitry **1701** in the present embodiment comprises circuitry for power regulation **1742**, clocking **1744**, CPU Bridge **1746**, IDE controller **1748**, and signal conveyance paths **1761-1774**. The CPU Bridge **1746** couples the CPU component **1710** of the ACM **1700** with the other components of the ACM **1720-1750** and the CPU-to-PCON Interconnection **1900**. The CPU Bridge **1746** and IDE controller **1748** have already been discussed. Power regulation circuitry **1742** receives electrical power via the electrical power conduction path **1914** of the CPU-to-PCON Interconnection **1900**, conditions and distributes it to the other circuitry in the ACM using power distribution bus **1768**. Such regulation and distribution is well known and understood in the art.

Clocking circuitry **1744** generates clock signals for distribution to other components within the ACM **1700** that require a timing and synchronization clock source. The CPU **1710** is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM **1700** includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path **1762**, in response to a signal received from the host interface controller (HIC) **1920** via signal path **1761**. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) **1920** of the presently described embodiment adjusts the frequency control signal sent via signal path **1761** to the clocking circuitry **1744**, based on the “console type” information signal **1918** conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection **1900**. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the user’s core computing power and environment to different work settings, which is a further advantage of the present invention.

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FIG. 19 illustrates an external view of one embodiment of an ACM. The case 2010 of the ACM 1700 is generally rectangular in shape, preferably constructed of a strong, lightweight, rigid material that will protect the internal components from mechanical and environmental exposure. The case 2010 may readily be used to construct the case 2010. The case 2010 completely surrounds the internal components, being generally an 8-sided box. FIG. 19 shows the top 2012, right 2014, and rear 2016 surfaces of the ACM case 2010. Rear edges 2018 of the case joining the rear surface 2016 with its adjoining surfaces may be beveled or rounded to facilitate insertion of the ACM 1700 into the computer bay of the PCON. Notches 2040 may be formed by projecting small surfaces inward from otherwise generally flat surfaces of the ACM case 2010. The notches 2040 may be used to engage with mechanical devices mounted in and about a computer bay. Such mechanical devices can be employed to secure the ACM into position within a computer bay for reliability and security. Openings 2017 are formed into the rear surface 2016 of the ACM case 2010 through which to project connectors 1930a and 1930b. In one embodiment the case 2010 is approximately 5.75 inches wide by 6.5 inches deep by 1.6 inches high.

Connectors 1930a and 1930b are part of the ACM-to-PCON Interconnection as described earlier in reference to FIGS. 3 and 4. When the ACM 1700 is inserted into the computer bay of a peripheral console (PCON), connectors 1930a and 1930b mate with corresponding connectors located at the rear of the computer bay to electrically couple the ACM with the PCON containing the computer bay. Details concerning the ACM-to-PCON Interconnection can be found in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference. The connectors 1930a and 1930b used in one embodiment are connectors complying with the Device Bay industry standard as documented in "Device Bay Interface Specification," revision 0.85, Feb. 6, 1998. Such connectors have specifically been designed to stand up to the rigors of repeated insertion and withdrawal.

Cooling plate 2030 forms part of the top surface 2012 of ACM 1700. The cooling plate 2030 may be mounted to, or project through an opening formed in, case 2010. Similarly, electromagnetic interference (EMI)/electrostatic discharge (ESD) grounding plate 2032 forms part of the right surface 2014 of ACM 1700. The grounding plate 2032 may be mounted to, or project through an opening formed in, case 2010. Cooling plate 2030 and grounding plate 2032 compressively mate with counterparts when the ACM is fully inserted into the computer bay. The counterparts located along the boundaries of the computer bay conduct dangerous heat and electrical charges away from the ACM. Inside the ACM, cooling plate 2030 thermally couples to heat-sensitive components such as CPU 1710 by methods well known in the art. Similarly, grounding plate 2032 electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art.

LCD display 2050 forms part of the right surface 2014 of ACM 1700. The LCD display may be mounted to, or project through an opening formed in, case 2010. The LCD display may contain indicators about the status of the ACM. Such indicators may display, for example, the time-of-day from a time-of-day clock contained within the ACM, or the amount of charge remaining in an ACM-resident battery, or certain configuration options recorded in flash memory. The LCD display 2050 provides display capability for a limited amount

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of information, most useful when the ACM is separated from a PCON (and is thus separated from a full-capability, primary display device).

FIG. 19b illustrates one possible embodiment of a computer bay. A computer bay 1890 acts as a receptacle for lodging an ACM (such as the one shown in FIG. 20) within a desktop PCON. The illustrated computer bay 1890 provides an ACM with housing and with signal flow, electrical grounding, heat transfer, and mechanical connections. While many physical arrangements between the ACM and PCON are possible, the use of an enclosed computer bay as the one illustrated in FIG. 20b offers many advantages. For example, the illustrated computer bay 1890 provides physical protection for the ACM. The computer bay may also be easily incorporated into industry standard form factors used in the manufacture of desktop personal computers (e.g., the ACM and associated computer bay could be designed to fit within the volume occupied by a standard-size disk drive).

The computer bay 1890 appearing in FIG. 20b is shown mounted within the confines of PCON case 1802. The computer bay 1890 comprises frame 1891 and signal flow, grounding, cooling, and locking components as described below. Mounting flanges 1898 of frame 1891 may be used to attach the computer bay 1890 to the PCON structure. The computer bay 1890 is prominently defined by frame 1891 generally forming a cavity in which to lodge an ACM. As such, the interior cavity formed by frame 1891 closely approximates the exterior dimensions of a compatible ACM. The top 1893, right 1894, and rear 1895 sides of the computer bay frame 1891 are visible. The computer bay frame 1891 also includes substantial bottom and left sides which are not shown. The front side of the frame 1891 (not shown) is open to allow the insertion of the ACM. Frame 1891 is constructed of metal for strength and to facilitate the conductance of heat and undesired electrical currents away from the ACM.

In the presently described embodiment, the weight of an inserted ACM is largely borne by the bottom side (not shown) of computer bay frame 1891. Alternative embodiments are possible where, for example, the weight of the ACM is borne by rails running longitudinally down the right and left sides of the computer bay cavity that engage corresponding grooves running longitudinally down the right and left sides of an ACM.

FIG. 20 illustrates the internal component layout for one embodiment of an ACM. All components are contained within the confines of the ACM case 510, except for connectors 1930a and 1930b which extend from the rear of the ACM 1700 to engage mating connectors (not shown) that will couple the ACM circuitry with the PCON circuitry. Main circuit board 2110 provides electrical connections for circuitry within the ACM and mounting for many of its components 1724, 1722, 1721, 1752, 1742, 1748, 1920, and 1930. The fabrication and use of such circuit boards is well known and understood in the art. Connector 2122 is also mounted on main circuit board 2110 and mates with mobile processor module 2120. Mobile processor module 2120 represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module 2120 is a self-contained unit that includes a microprocessor 1712, CPU cache 1714, and CPU bridge 1746 operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.



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The mobile processor module **2120** blocks the view, from the top, of the system BIOS **1724**. Similarly, hard disk drive **1732** hides RAM memory **1722**, the high performance graphics processor **1752**, the host interface controller **1920**, and flash memory **1726**. Memory upgrade socket **2130** remains exposed to facilitate installation of additional RAM memory **1722**. Power regulator **1742**, like the memory upgrade socket, enjoys a generous amount of overhead clearance to accommodate its vertical size. The area including IDE controller **1748** also enjoys overhead clearance to facilitate a cable connection with the hard disk drive **1732**.

The functional interconnection and operation of components contained within the ACM and depicted in FIG. **20** has already been described in relation to FIG. **18** for like numbered items appearing therein.

FIG. **21** is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package **200** contains the PCON functional components **1801** and the PCON side of the ACM-to-PCON Interconnection **1900**. The PCON functional components **1801** comprise primary display **1810**, a primary input **1820**, a primary power supply **1830**, interface and support **1840**, secondary mass storage **1850**, other devices **1860**, and expansion slots **1870**.

The PCON side of the ACM-to-PCON Interconnection **1900** comprises a Peripheral Interface Controller (PIC) component **1940**, a PCON connector component **1950**, console-type component **1942**, and flash memory device **1948**. The PIC **1940** and connector **1950** components couple the PCON functional components **1801** with the signals of an ACM-to-PCON interface bus **1910** used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus **1910** comprises conveyance for electrical power **1914** and signals for a peripheral bus **1912**, video **1916**, video port **1917**, and console-type **1918**. The preferred ACM-to-PCON Interconnection **1900** is described in detail in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference.

Connector component **1950** may be selected to mate directly with the connector component **1930** of an ACM (shown in FIG. **18**). Alternatively, connector component **1950** may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment, such as cable **1964** shown in FIG. **19B**. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

Flash memory device **1948** provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory **1948** may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

The primary display component **1810** of the PCON functional circuitry **1801** of the presently described embodiment comprises integrated display panel **1812** and video connector **1813**. Integrated display panel **1812** is a color LCD display panel having a resolution of 640 horizontal by 480 vertical pixels. 640-by-480 resolution is popularly considered to be the minimum screen size to make practical use of the appli-

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cation software in widespread use today. One skilled in the art recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (**1710** of FIG. **17**) of an ACM presently coupled to PCON **1800**.

Integrated display panel **1812** is coupled to video signal bus **1849** and displays a screen image in response to video signals presented on bus **1849**. Certain pins of connector **1950** receive video output signals **1916** of the ACM-to-PCON interface bus **1910** from a mated connector that is coupled to an ACM. These certain pins of connector **1950** couple to video signal bus **1849** which conveys the video output signals **316** throughout the PCON **1800** as needed. Video connector **1813** is exposed at the exterior of PCON **1800** and couples to video signal bus **1849**. Connector **1813** permits easy attachment of an external display device that is compatible with the signals carried by bus **1849**, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel **1812**.

The isolation of the relatively heavy and sizable primary display **1810** from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

The primary input component **1820** of the PCON functional circuitry **1801** of the presently described embodiment comprises keyboard interface circuitry **1822**, keyboard connector **1823**, pointer interface circuitry **1824**, and pointer connector **1825**. Keyboard interface circuitry **1822** and pointer interface circuitry **1824** connect to ISA bus **1845** and are thereby coupled to the CPU component (**1710** of FIG. **17**) of any ACM attached to PCON **1800**. Keyboard interface circuitry **1822** interfaces a standard computer keyboard (not shown), attached at connector **1823**, to ISA bus **1845**. Pointer interface circuitry **1822** interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector **1825**, to ISA bus **1845**. Computer keyboards, pointing devices, connectors **1823**, **1825**, keyboard interface circuitry **1822**, and pointer interface circuitry **1824** are well known in the art. The isolation of the relatively heavy and sizable primary input devices **1820** from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

The primary power supply component **1830** of the PCON functional circuitry **1801** of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON **1800** and any ACM coupled to connector **1950**. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source **1889**, such as a wall outlet. Power supply **1830** reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply **1830** are applied to power bus **1831**. Power bus **1831** distributes the power supply outputs to the other circuitry within the PCON **1800**. Bus **1831** also connects to certain pins of connector **1950** to provide the electrical power **1914** for an ACM conveyed by ACM-to-PCON interconnection **1900**. The isolation of the usually heavy power supply **1830** from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.

The interface and support component **1840** of the PCON functional circuitry **1801** of the presently described embodi-



ment comprises peripheral bridge **1846**, diskette controller **1842**, IDE controller **1848**, and signal conveyance paths **1841**, **1843**, **1844**, **1845**, **1847** and **1849**. Peripheral bridge **1846** couples PCI peripheral bus **1841** with peripheral busses of other formats such as ISA peripheral bus **1845** and others **1847**. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses **1847** may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console **1800** may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection **1900**, such as PCI bus **1841**, this embodiment includes peripheral bridge **1846** to establish additional busses **1845**, **1847**. The additional busses **1845**, **1847** permit the use of the many low-cost and readily available components compatible with these bus specifications.

Diskette controller **1842** interfaces a floppy disk drive **1854** with the CPU component **1710** of an attached ACM (shown in FIG. **18**) so that the CPU may control and use the diskette drive **1854** hardware to store and retrieve data. Diskette controller **1842** couples to the CPU via a connection to ISA bus **1845**. Diskette controller **1842** connects to the diskette drive **1854** via one of device cables **1843**.

Similarly, IDE controller **1848** interfaces a hard disk drive **1852** and a CDROM drive **1856** with the CPU component **1710** of an attached ACM (shown in FIG. **18**) so that the CPU may control and use the hard disk drive **1852** and CDROM **1856** hardware to store and retrieve data. IDE controller **1848** couples to the CPU via connection to PCI peripheral bus **1841**. IDE controller **1848** connects to each of hard disk drive **1852** and CD-ROM drive **1856** via one of device cables **1843**. Some embodiments of PCON **1800** may take advantage of VLSI integrated circuits such as an 82371 SB (PIIX4) integrated circuit from Intel Corporation. An 82371 SB integrated circuit includes circuitry for both the peripheral bridge **1846** and the IDE controller **1848** in a single package.

The secondary mass storage component **1850** of the PCON functional circuitry **1801** of the presently described embodiment comprises diskette drive **1854**, hard disk drive **1852**, and CD-ROM drive **1856**. Secondary mass storage **1850** generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage **1850** are not part of a computer user's core computing power and environment. Secondary mass storage **1850** may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console **1800**, or archival copies of data files that are maintained in primary mass storage **1750** of an ACM (shown in FIG. **18**). Storage capacities for secondary mass storage **1850** devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive **1854**, to more than 10 gigabytes for a large format (5-inch) hard disk drive **1852**. Hard disk drive **1852** employs fixed recording media, while diskette drive **1854** and CD-ROM drive **1856** employ removable media. Diskette drive **1854** and hard disk drive **1852** support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive **1856** supports only read operations.

The other devices component **1860** of the PCON functional circuitry **1801** of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog signal for processing by the computer. Video capture cards at present are considered a specialty, i.e., not ubiquitous, com-

ponent of personal computer systems. Digitized picture information from video capture card **1860** is carried via signal conveyance path **1844** to the peripheral interface controller **1940** which transforms it to the video port signals **1917** of the ACM-to-PCON interconnection **1900** for coupling to the advanced graphics processor **1752** in an attached ACM (shown in FIG. **18**).

Video capture card **1860** is merely representative of the many types of "other" devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card **1860** is shown installed in one of expansion slots **1870** for coupling to the interface and control circuitry **1840** of the PCON. Any of other devices **1860** could be coupled to the interface and control circuitry **1840** of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry **1840**; e.g., a motherboard.

The expansion slots component **1870** of the PCON functional circuitry **1801** of the presently described embodiment comprises PCI connectors **1871** and ISA connectors **1872**. A circuit card may be inserted into one of the connectors **1871**, **1872** in order to be operatively coupled with the CPU **1710** of an attached ACM (shown in FIG. **18**). Each of connectors **1871** electrically connects to PCI bus **1841**, and may receive and hold a printed circuit card which it electrically couples to PCI bus **1841**. Each of connectors **1872** electrically connects to ISA bus **1845**, and may receive and hold a printed circuit card which it electrically couples to ISA bus **1845**. The PCI **1841** and ISA **1845** busses couple to the CPU **1710** of an attached ACM (shown in FIG. **18**) by circuitry already described.

An embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises, an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary input circuitry when said interconnection circuitry is disconnected from a peripheral console.

An alternative embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary output circuitry when said interconnection circuitry is disconnected from a peripheral console.

Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. (A limited number of modifications have already been described in the preceding discussion.) For example, a particular embodiment may insert another layer of bus bridging between the CPU bridge and the Peripheral bridge. This may be desirable if, for example, a vendor wants to implement a proprietary, general-purpose bus having intermediate performance characteristics that fall between those of the high-performance general purpose bus originating at the CPU, and the slower general purpose PCI bus. Thus, the foregoing description is not intended to limit the invention as set forth.

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In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 22, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 2200, and a second portion, which includes a hard drive module 2220. A common printed circuit board 2237 houses these modules and the like. Among other features, the ACM includes the central processing unit module 2200 with a cache memory 2205, which is coupled to a north bridge unit 2221, and a host interface controller 2201. The host interface controller includes a lock control 2203. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 2217. Here, the CPU module is spatially located near connector 2217.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 2201 is coupled to BIOS/flash memory 2205. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 2203 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 2220. Among other elements, the hard drive module includes north bridge 2221, graphics accelerator 2223, graphics memory 2225, a power controller 2227, an IDE controller 2229, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal

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computer interface ("PCI") bus 2231, 2232. A power regulator 435 is disposed near the PCI bus.

In a specific embodiment, north bridge unit 2221 often couples to a computer memory, to the graphics accelerator 2223, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 2223 typically couples to a graphics memory 2223, and other elements. IDE controller 2229 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit 2220 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 2220 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 2240 may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

FIG. 23 is a simplified block diagram 2300 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 2300 has a variety of features such as those noted above, as well as others. In the present reference numerals are used to show the operation of the present system.

The block diagram is an attached computer module 2300. The module 2300 has a central processing unit, which communicates to a north bridge 2341, by way of a CPU bus 2327. The north bridge couples to main memory 2323 via memory

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bus **2329**. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem **2315** via bus **2342**. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2½ inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **2302** and **2331**. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus **2337** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **2305** with a BIOS. The flash memory device **2305** also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller **2307** communicates to the north bridge via bus **2335** and host PCI bus. The host interface controller also has a lock control **2309**, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller **2307** communicates to the console using bus **2311**, which couples to connection **2313**.

In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device **505**. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

In a specific embodiment, the present invention also includes a real-time clock **510** in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz **508** that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source **506** such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety

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of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.



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The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

1. A computer system comprising:

- a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector, the console being an enclosure housing the coupling sites, an Ethernet controller coupled to an external network, and
- a low voltage differential signal channel (LVDS) comprises two sets of unidirectional, serial bit channels which transmit encoded PCI bus transaction data in opposite directions;
- a computer module coupled to one of the coupling sites through the connector, comprising
  - a processing unit,
  - a flash memory storage device coupled to the processing unit, and
  - a serial communication controller coupled to the connector of the coupling site for communication to the console; and

wherein the computer module comprises a computing environment for a personal user.

2. The computer system of claim 1 wherein each of the unidirectional, serial bit channels comprises a plurality of pairs of low voltage differential signal lines.

3. The computer system of claim 1 wherein the computer module communicates to the console through USB (Universal Serial Bus).

4. The computer system of claim 1 wherein the flash memory storage device includes code to provide password protection for controlling access to the computer module.

5. The computer system of claim 1 wherein the console further comprises a power supply that supplies power to the computer module.

6. A computer system comprising:

- a console comprising a power supply, a first coupling site and a second coupling site, each coupling site comprising a connector, the console being a first enclosure housing the coupling sites, the power supply and a low voltage differential signal channel (LVDS) comprises two sets of unidirectional, serial bit channels which transmit encoded PCI bus transaction data in opposite directions;
- a computer module coupled to one of the coupling sites through the connector, comprising
  - a second enclosure,
  - a processing unit,
  - a serial communication controller coupled to the connector of the coupling site for communication to the console, and
  - a flash memory storage device coupled to the processing unit;

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wherein the power supply supplies power to the computer module.

7. The computer system of claim 6 wherein the computer module communicates to the console through USB (Universal Serial Bus).

8. The computer system of claim 6 wherein each of the unidirectional, serial bit channels comprises a plurality of pairs of low voltage differential signal lines.

9. The computer system of claim 6 wherein the flash memory storage device is configurable to store a password for controlling access to the computer module.

10. The computer system of claim 6 wherein the computer module further comprises a computing environment for a personal user.

11. A computer system comprising:

- a console comprising an integrated LCD display, a first coupling site and a second coupling site, each coupling site comprising a connector, the console being a first enclosure housing the coupling sites, and a low voltage differential signal channel (LVDS) comprises two sets of unidirectional, serial bit channels which transmit encoded PCI bus transaction data in opposite directions;
- a computer module coupled to one of the coupling sites through the connector, comprising
  - a second enclosure,
  - a processing unit,
  - a serial communication controller coupled to the connector of the coupling site for communication to the console, and
  - a mass storage device coupled to the processing unit;

wherein the computer module communicates to the console through USB (Universal Serial Bus), and wherein each of the unidirectional, serial bit channels comprises a plurality of pairs of low voltage differential signal lines.

12. The computer system of claim 11 wherein the mass storage device comprises a flash memory.

13. The computer system of claim 11 wherein the mass storage device is configurable to store a password for controlling access to the computer module.

14. The computer system of claim 11 wherein the computer module further comprises a computing environment for a personal user.

15. The computer system of claim 11 wherein the mass storage device comprises a hard disk drive.

16. A computer system comprising:

- a console comprising a DVD drive, a first coupling site, and a second coupling site, each coupling site comprising a connector, the console being a first enclosure housing each coupling site, and
  - an interface controller coupled to a differential signal channel which comprises two sets of unidirectional low voltage serial bit channels which transmit encoded PCI bus transaction data in opposite directions; and
  - a computer module coupled to one of the coupling sites through the connector, comprising
    - a second enclosure,
    - a processing unit,
    - a serial communication controller coupled to the connector of the coupling site for communication to the console, and
    - a mass storage device coupled to the processing unit;
- wherein the computer module communicates to the console through USB (Universal Serial Bus) and wherein each of the unidirectional serial bit channels comprises a plurality of pairs of low voltage differential signal lines.

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17. The computer system of claim 16 wherein the mass storage device comprises a flash memory.

18. The computer system of claim 16 wherein the mass storage device is configurable to store a password for controlling access to the computer module.

19. The computer system of claim 16 wherein the computer module further comprises a computing environment for a personal user.

20. The computer system of claim 16 wherein the mass storage device comprises a hard disk drive.

21. A computer system comprising:

a console comprising a first coupling site and a second coupling site; each coupling site comprising a connector, the console being an enclosure housing each coupling site, a shared storage subsystem, and a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector, each computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a serial communication controller coupled to the console through the connector of the coupling site, and

two unidirectional serial, low voltage differential signal (LVDS) channels which transmit encoded PCI bus transaction data in opposite directions, and wherein each of the computer modules operates independent of each other, and the shared storage subsystem is shared by the computer modules.

22. The computer system of claim 21 wherein the shared storage subsystem is a hard disk drive.

23. The computer system of claim 21 wherein the shared storage subsystem is a DVD drive.

24. The computer system of claim 21 wherein each of the unidirectional serial channels comprises a plurality of pairs of low voltage differential signal lines.

25. The computer system of claim 21 wherein the console further comprises a serial communication hub controller that couples to the serial communication controller in each of the computer modules through the connector of the coupling site to support communication to an external network.

26. A computer system comprising:

a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector, the console being an enclosure housing each coupling site, a hard disk drive and

a low voltage differential signal (LVDS) channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions; and

a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, comprising

a processing unit,

a main memory coupled to the processing unit, and

an Ethernet controller coupled to the connector of the coupling site for communication to an external network through the console; and

wherein each of the computer modules is similar in design to each other and operates fully independent of each other.

27. The computer system of claim 26 wherein the data transmitted by the LVDS channel comprises encoded Peripheral Component Interconnect (PCI) bus transaction.

28. The computer system of claim 26 wherein the console further comprises an Ethernet hub controller that couples to the Ethernet controller in each of the computer modules through the connector of the coupling site to support the communication to the external network.

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29. The computer system of claim 26 wherein the hard disk drive is shared by the computer modules.

30. The computer system of claim 25 wherein each of the unidirectional serial channels comprises a plurality of pairs of low voltage differential signal lines.

31. A computer system comprising:

a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector, the console being an enclosure housing each coupling site, a shared storage subsystem and

a low voltage differential signal (LVDS) channel comprises two sets of a plurality of unidirectional serial bit channels which transmit data in opposite directions; and a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, comprising

a processing unit,

a main memory coupled to the processing unit, and

a serial communication controller coupled to the connector of the coupling site for communication to an external network through the console; and

wherein each of the computer modules is similar in design to each other and operates fully independent of each other, and the shared storage subsystem is shared by the computer modules.

32. The computer system of claim 31 wherein the data transmitted by the LVDS channel comprises encoded Peripheral Component Interconnect (PCI) bus transaction.

33. The computer system of claim 31 wherein the console further comprises a serial communication hub controller that couples to the serial communication controller in each of the computer modules through the connector of the coupling site to support the communication to the external network.

34. The computer system of claim 31 wherein the shared storage subsystem is a hard disk drive.

35. The computer system of claim 31 wherein one of the computer modules comprises a core computing power and environment for a computer user.

36. A computer system comprising:

a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector; the console being an enclosure housing each coupling site, and

a low voltage differential signal (LVDS) channel comprises two sets of unidirectional multiple serial bit channels which can transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions;

a plurality of computer modules, each computer module coupled to one of the coupling sites through the connector, and comprising

a processing unit, and

a main memory coupled to the processing unit,

wherein each of the computer modules can operate fully independent of each other, and wherein one of the computer modules couples to the LVDS channel for data communication.

37. The computer system of claim 36 wherein each computer module further comprises an Ethernet controller coupled to the console through the connector of the coupling site for communication to an external network.

38. The computer system of claim 36 wherein the console further comprises a hard disk drive coupled to the computer modules.

39. A computer system comprising:

a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector

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and a slot, the console comprises a serial communication hub controller and an enclosure housing each coupling site, the serial communication hub controller, a low voltage differential signal (LVDS) channel comprises two sets of unidirectional multiple serial bit channels which transmit data in opposite directions, and a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector and the slot and each computer module comprising a processing unit, a main memory coupled to the processing unit, and an Ethernet controller coupled to the console for communication to an external network; wherein each of the computer modules can operate fully independent of each other.

40. The computer system of claim 39 wherein the console further comprises a shared hard disk drive that couples to the computer modules.

41. The computer system of claim 39 wherein the LVDS channel in the console communicates an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction data.

42. A computer system comprising:

a console comprising a first coupling site and a second coupling site; each coupling site comprising a connector, the console being an enclosure housing an integrated LCD display, each coupling site, two unidirectional multiple serial, low voltage differential signal (LVDS) channels which transmit data in opposite directions, and a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector, each computer module comprising a processing unit, a main memory coupled to the processing unit, a serial communication controller coupled to the connector of the coupling site for communication to an external network, and a flash memory storage device coupled to the processing unit; and wherein each of the computer modules can operate independent of each other.

43. The computer system of claim 42 wherein the console further comprises a hard disk drive that couples to one of the computer modules.

44. The computer system of claim 42 wherein the data transmitted by the LVDS channels comprises encoded Peripheral Component Interconnect (PCI) bus transaction data.

45. A computer system comprising:

a console comprising a first coupling site, and a second coupling site, each coupling site comprising a connector and a slot, the console being an enclosure housing each coupling site, a low voltage differential signal (LVDS) channel comprises two sets of unidirectional serial bit channels in opposite directions which can transmit an encoded data of Peripheral Component Interconnect (PCI) bus transaction; and a plurality of computer modules; each computer module coupled to one of the coupling sites through the connector and the slot and each computer module comprising a processing unit,

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a main memory coupled to the processing unit, and an Ethernet controller coupled to the connector of the coupling site for communication to an external network; and

wherein one of the computer modules couples to the LVDS channel through the connector of the coupling site.

46. The computer system of claim 45 wherein the console further comprises a hard disk drive that couples to one of the computer modules.

47. The computer system of claim 45 wherein the console further houses an add-on board that communicates Peripheral Component Interconnect (PCI) bus transaction data through the LVDS channel in the console to one of the computer modules.

48. A computer system comprising:

a console comprising a first coupling site and a second coupling site, each coupling site comprising a connector, the console being an enclosure housing the coupling sites,

a low voltage differential signal (LVDS) channel comprises two sets of unidirectional serial bit channels in opposite directions which transmit an encoded data of Peripheral Component Interconnect (PCI) bus transaction; and

a computer module coupled to one of the coupling sites through the connector, comprising a processing unit, a main memory coupled to the processing unit, and an interface controller that couples to the low voltage differential signal (LVDS) channel in the console through the connector of the coupling site.

49. The computer system of claim 48 wherein the console further houses an add-on board that communicates Peripheral Component Interconnect (PCI) bus transaction data through the low voltage differential signal (LVDS) channel in the console to the computer module.

50. A computer system comprising:

a console comprising a first coupling site and a second coupling site, the console being an enclosure housing each coupling site and an integrated LCD display;

a plurality of computer modules, each computer module coupled to one of the coupling sites, and comprising a processing unit, a main memory coupled to the processing unit, a low voltage differential signal (LVDS) channel comprises two sets of unidirectional serial bit channels which transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions, and

an interface controller coupled to a connector of the coupling site through the LVDS channel.

51. The computer system of claim 50 wherein the console further comprises a serial communication hub controller to support communication between the computer modules.

52. The computer system of claim 50 wherein each computer module further comprises a flash memory storage device.

53. A computer system comprising:

a console comprising a power supply, a plurality of coupling sites, and an Ethernet hub controller configured to couple to an external network, each of the coupling sites comprising a connector and a slot, the coupling sites comprising a first coupling site and a second coupling site, the console being an enclosure comprising internal power and data connections to each of the coupling sites, the enclosure housing the power supply, the coupling sites, and the Ethernet hub controller; and

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a plurality of computer modules configured to couple to  
 respective ones of the coupling sites, each of the com-  
 puter modules being an assembly comprising a main  
 circuit board and a connector that is distinct from the  
 main circuit board and that is configured to couple to a  
 respective one of the connectors of the coupling sites for  
 power and data communication, each of the computer  
 modules comprising  
 a processing unit,  
 a main memory coupled to the processing unit, and  
 an Ethernet controller configured to couple to the Eth-  
 ernet hub controller through a respective one of the  
 connectors of the coupling sites for data communica-  
 5 tion between the computer modules and to the exter-  
 nal network,  
 wherein the computer modules comprise a first computer  
 module, configured to couple to the first coupling site,  
 and a second computer module, configured to couple to  
 the second coupling site, the slot of the first coupling site  
 configured to receive the first computer module and to  
 guide the first computer module to the connector of the  
 first coupling site, the slot of the second coupling site  
 configured to receive the second computer module and

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to guide the second computer module to the connector of  
 the second coupling site, and  
 wherein each of the computer modules is configured to  
 operate fully independent of each other.

54. The computer system of claim 53 wherein the Ethernet  
 hub controller is configured to establish data communication  
 between the computer modules and to the external network  
 through point-to-point Ethernet links.

55. The computer system of claim 53 wherein the console  
 10 further comprises a storage subsystem configured as a shared  
 storage for the computer modules.

56. The computer system of claim 53 wherein the console  
 further comprises a low voltage differential signal channel  
 that comprises two sets of unidirectional, serial bit channels  
 15 which transmit data in opposite directions.

57. The computer system of claim 56 wherein each of the  
 computer modules is configured to couple to the low voltage  
 differential signal channel through a respective one of the  
 connectors of the coupling sites.

20 58. The computer system of claim 57 wherein each of the  
 unidirectional, serial bit channels comprises a plurality of  
 pairs of low voltage differential signal lines.

\* \* \* \* \*





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(12) **United States Patent**  
**Chu**

(10) **Patent No.:** **US 8,041,873 B2**

(45) **Date of Patent:** **\*Oct. 18, 2011**

(54) **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA**

(52) **U.S. Cl. ....** 710/313; 710/301; 710/315; 709/227

(58) **Field of Classification Search ....** 710/300-317, 710/62-64, 72-74; 709/214-219, 226-227; 714/43-44, 11, 13

See application file for complete search history.

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(57) **ABSTRACT**

A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

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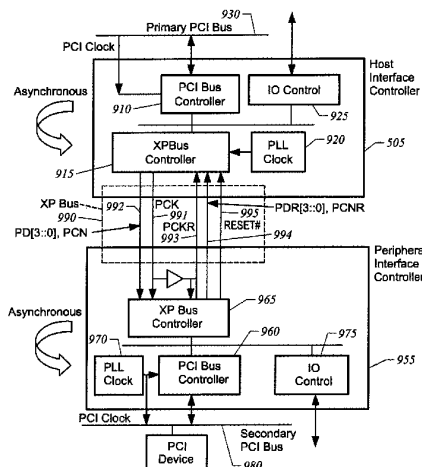
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(51) **Int. Cl.**  
**G06F 13/20**

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**103 Claims, 24 Drawing Sheets**



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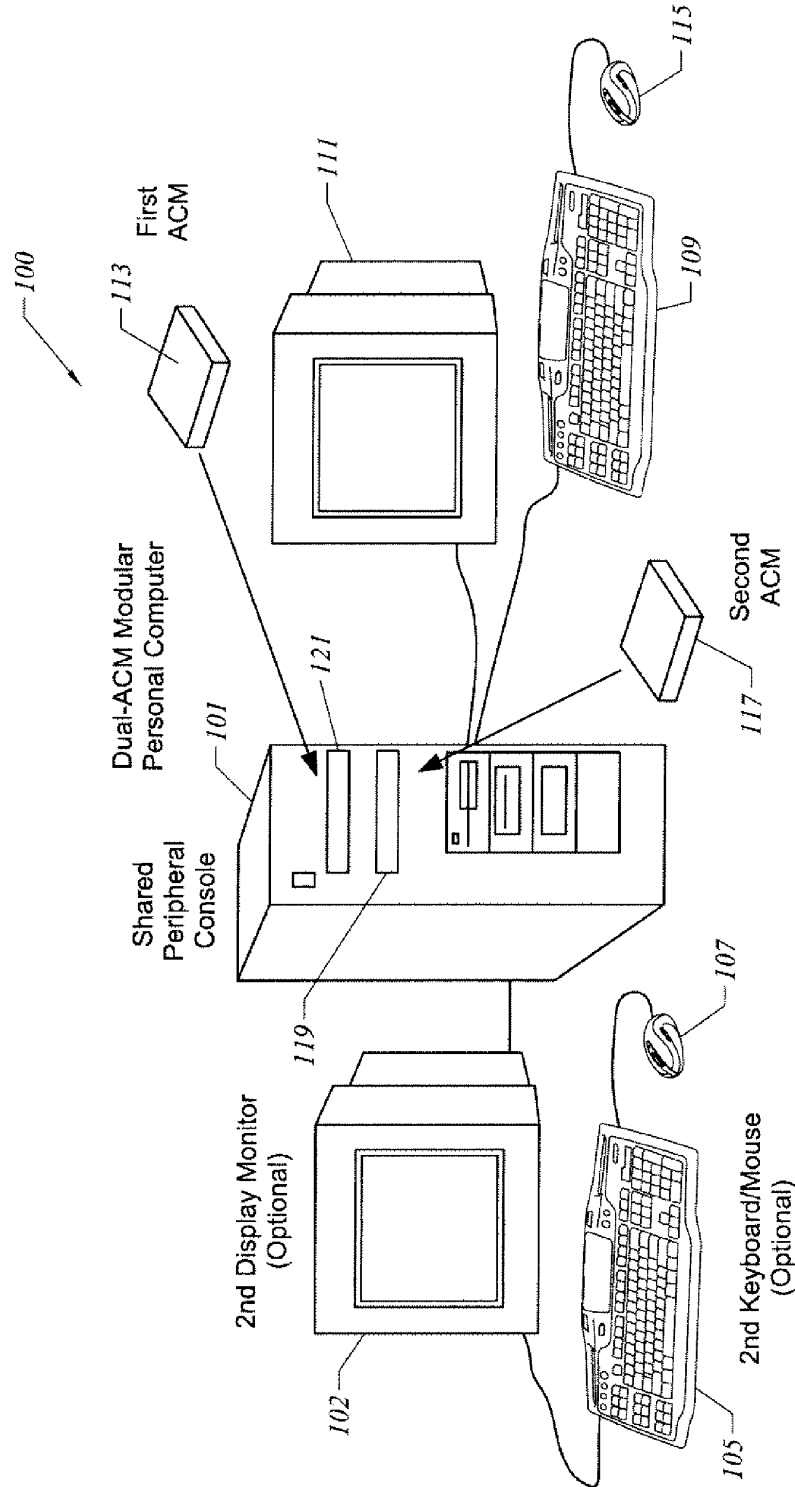


FIGURE 1



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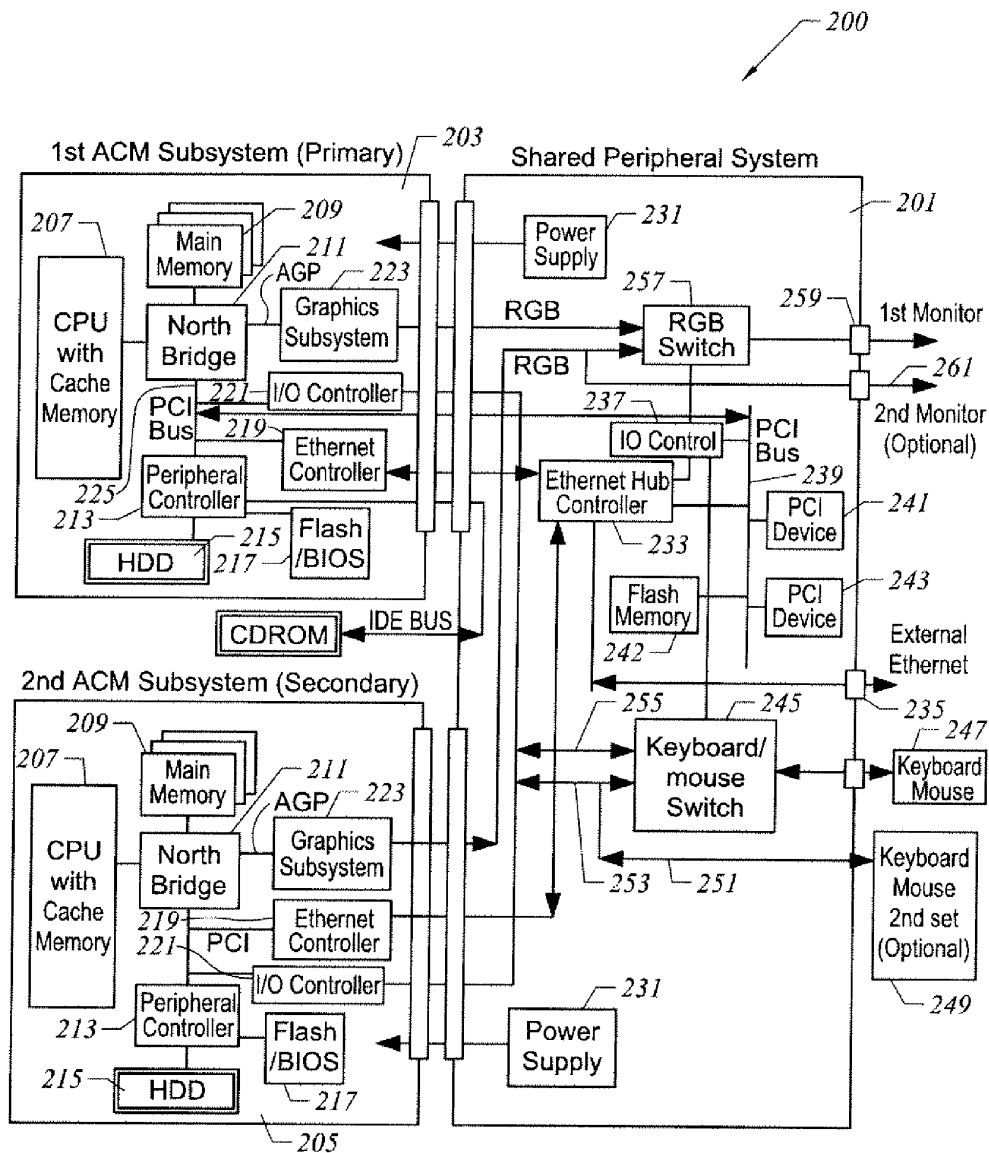


FIGURE 2

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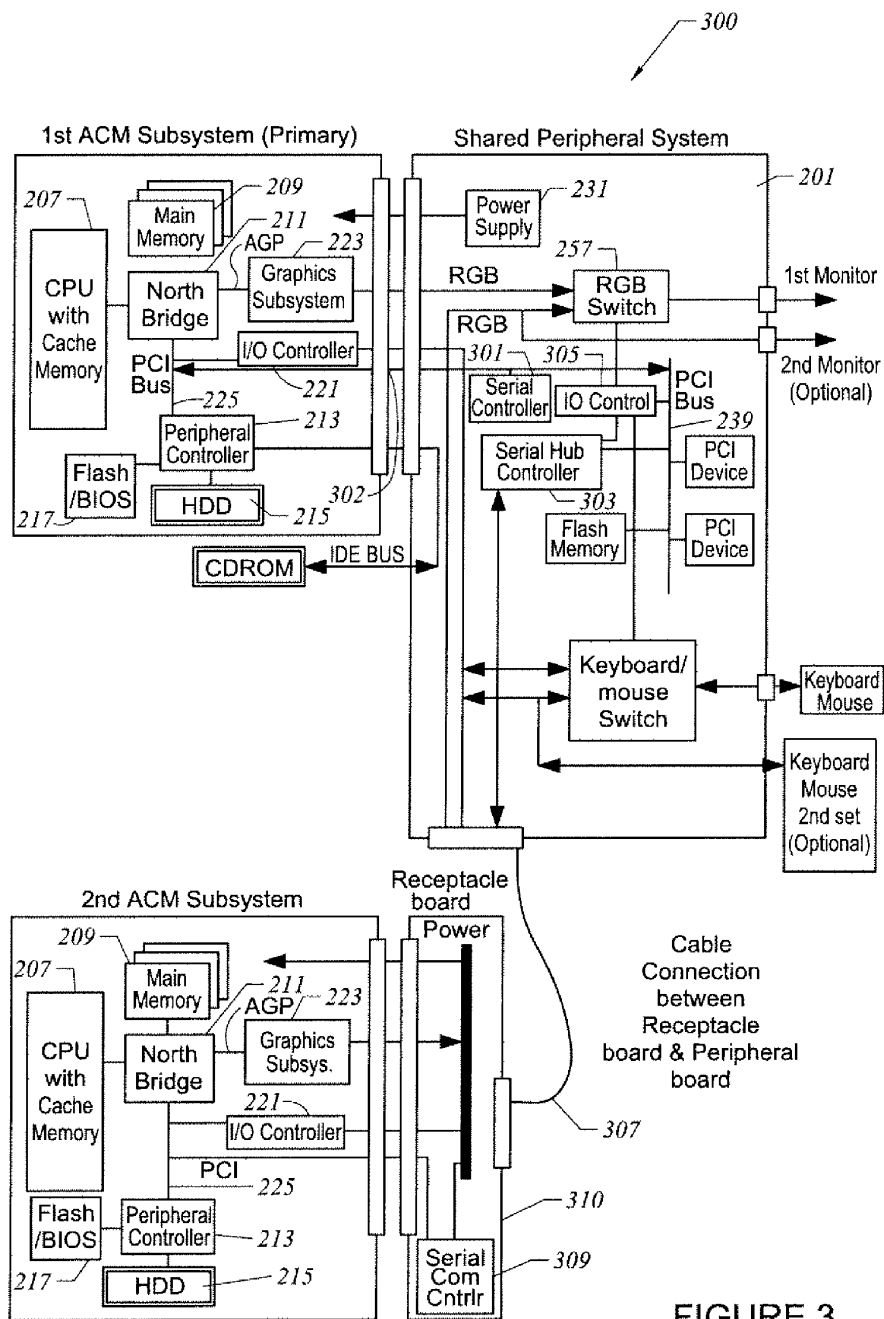


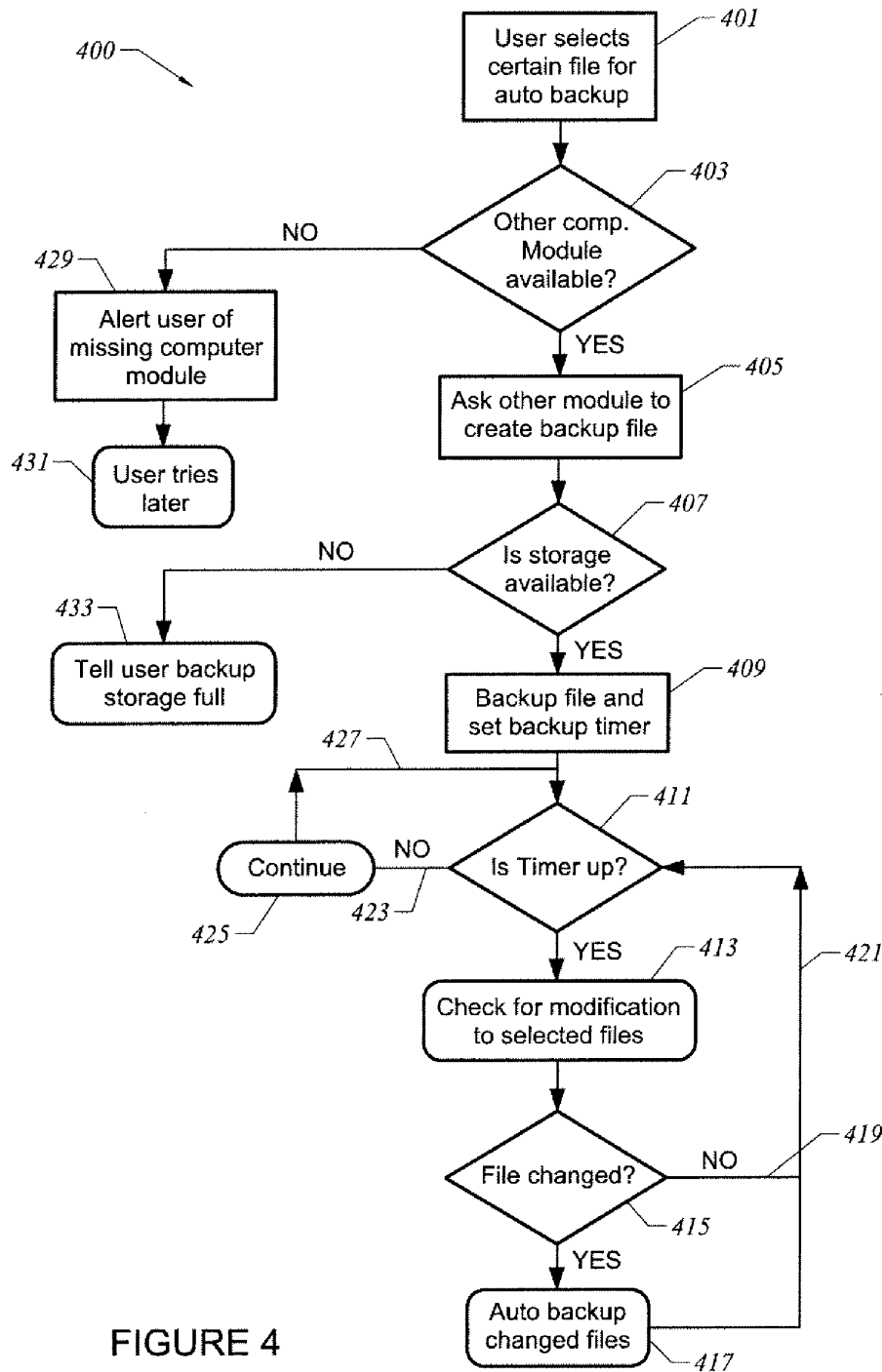
FIGURE 3

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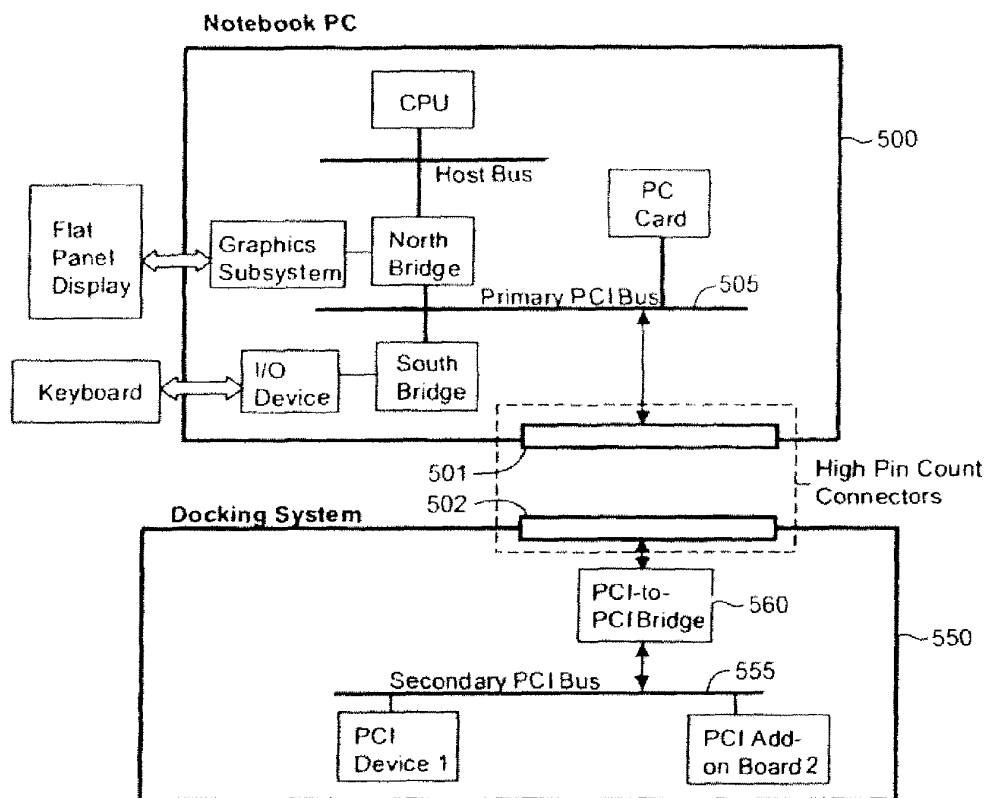


FIGURE 5

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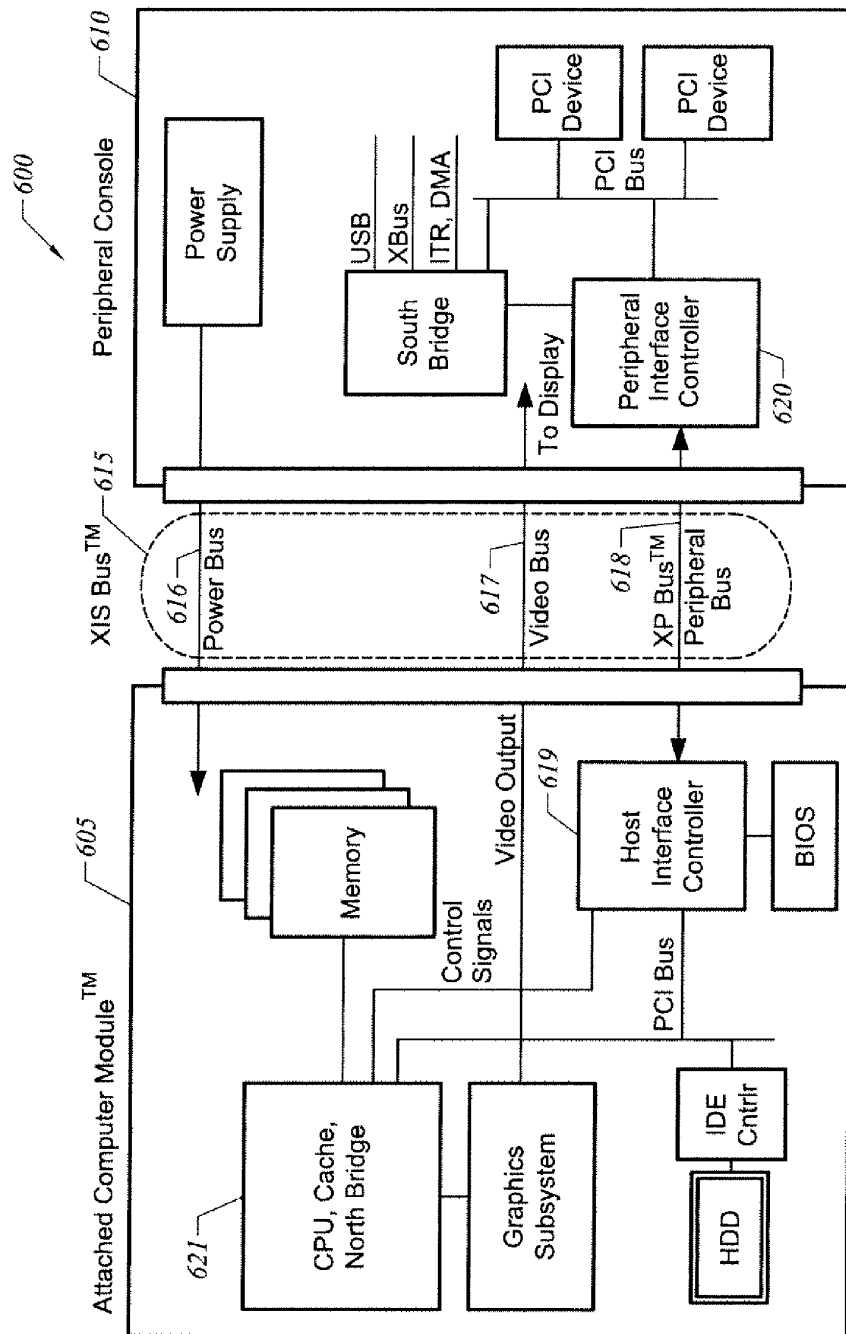


FIGURE 6

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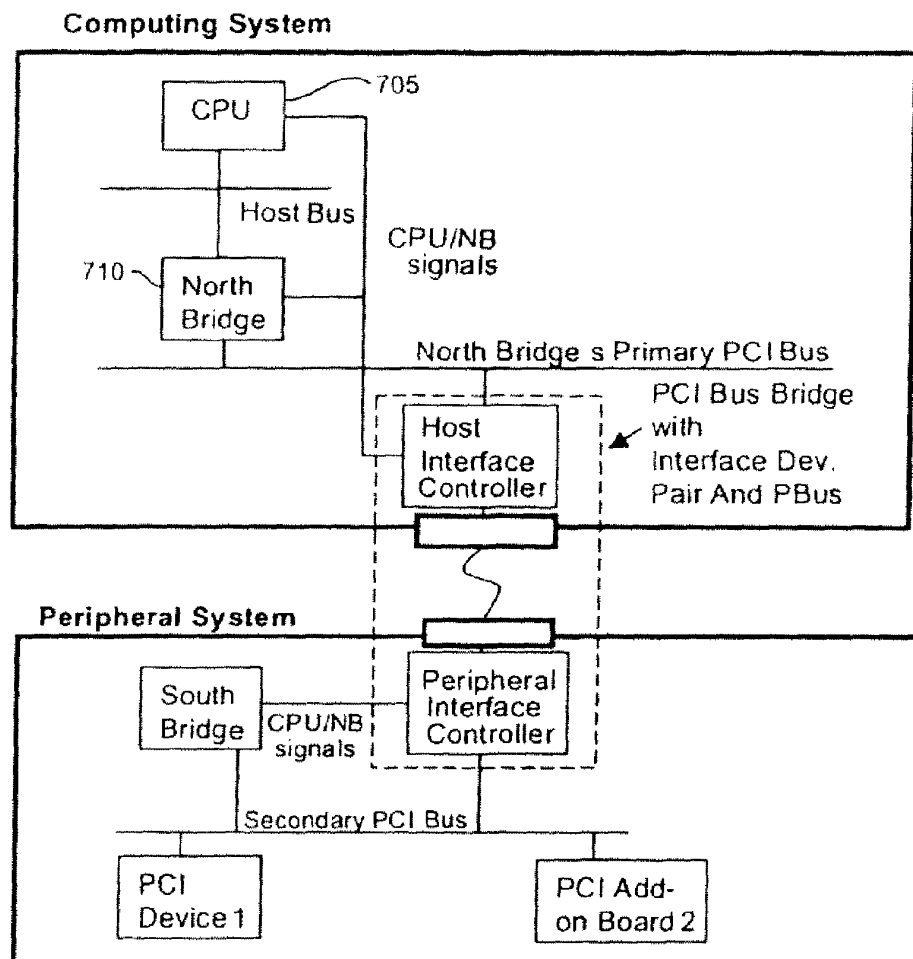


FIGURE 7

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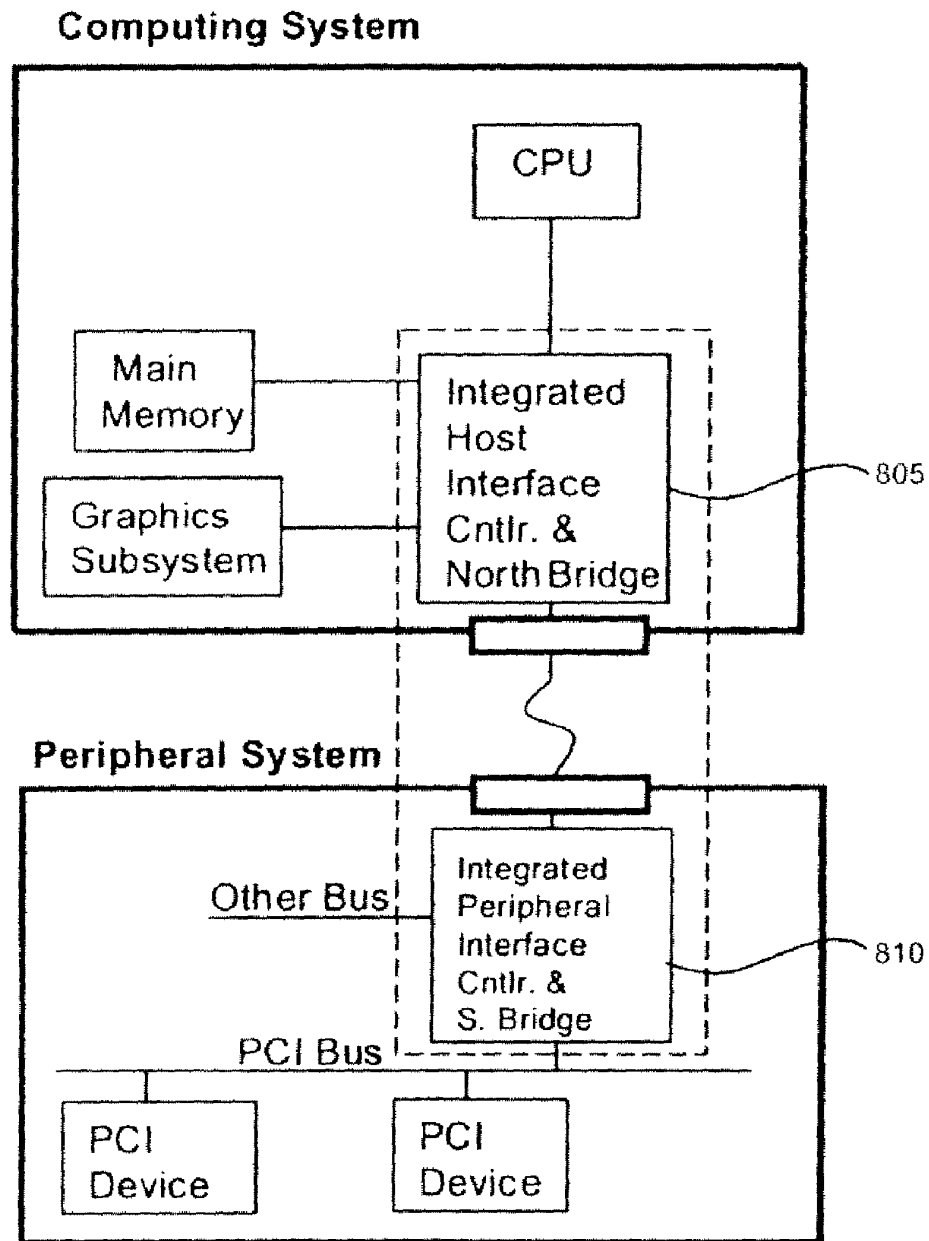


FIGURE 8



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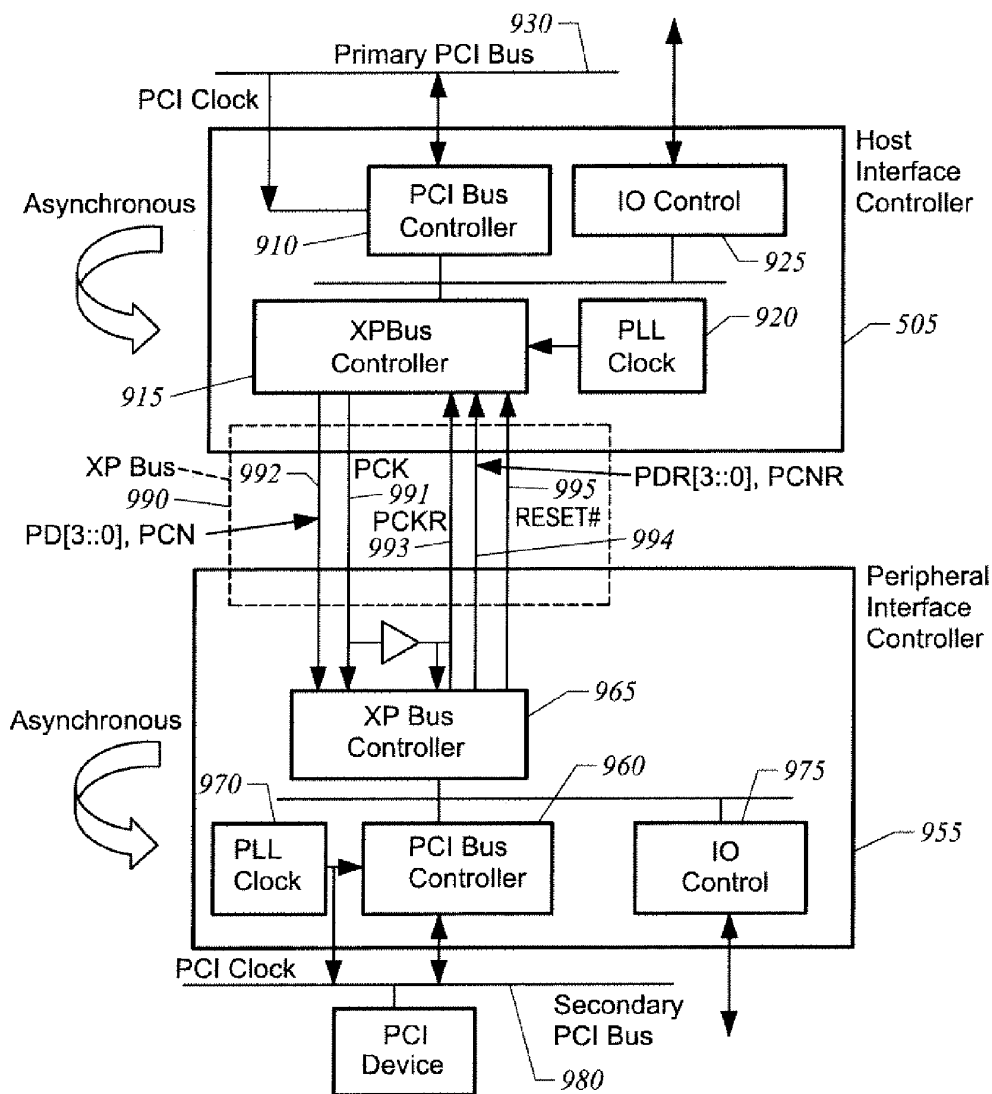


FIGURE 9

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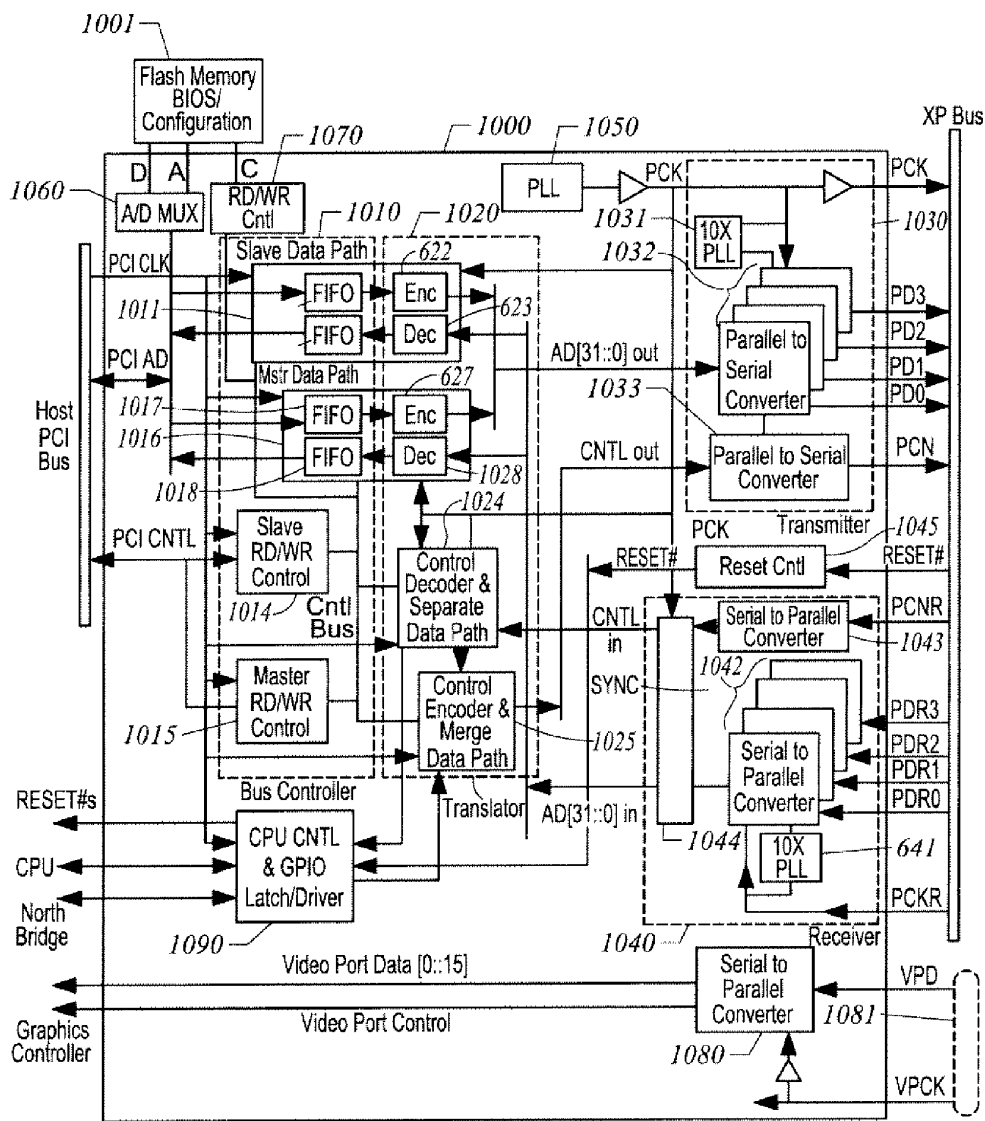


FIGURE 10

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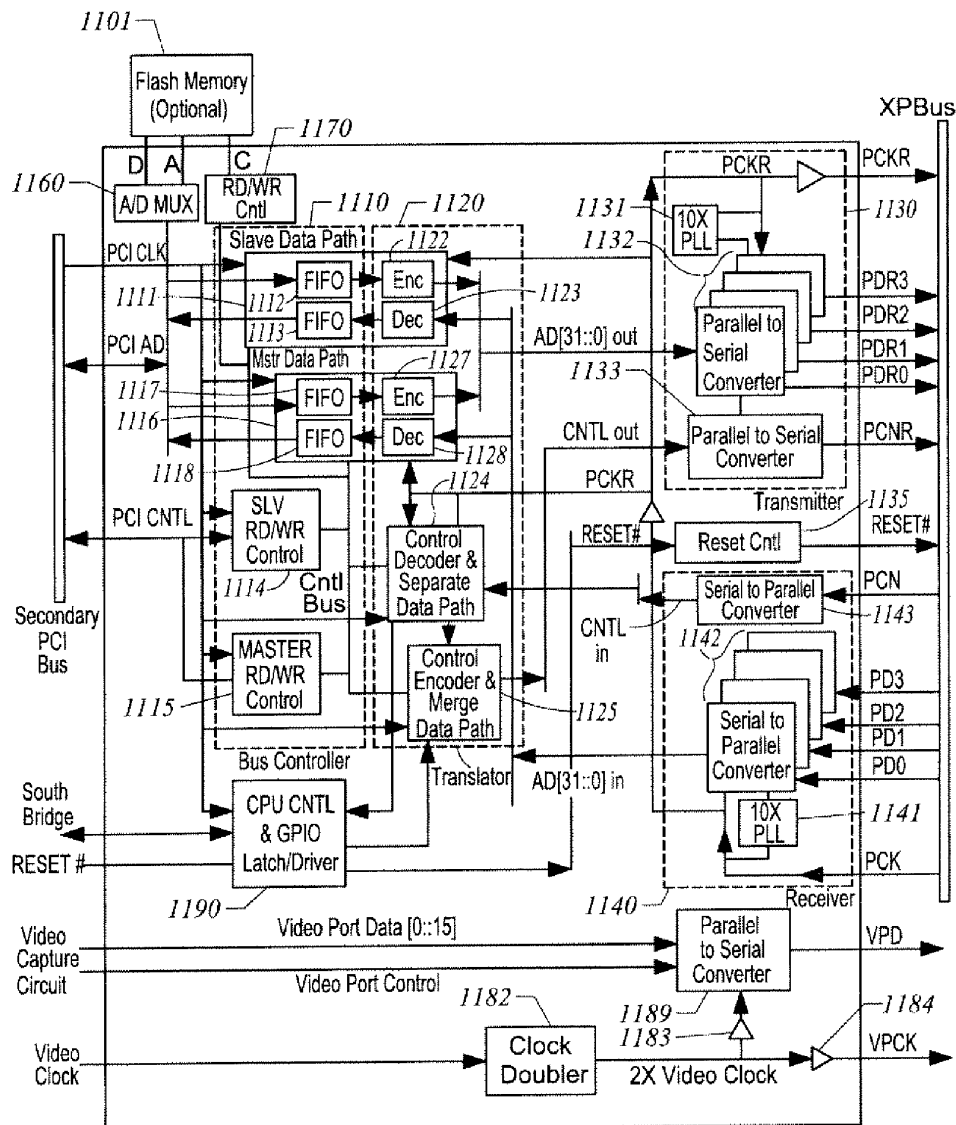


FIGURE 11

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	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0+
3	PD0-			Computer to Peripheral LVDS Data 0-
4	PD1 RTN			GND
5	PD1+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1+
6	PD1-			Computer to Peripheral LVDS Data 1-
7	PD2 RTN			GND
8	PD2+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2+
9	PD2-			Computer to Peripheral LVDS Data 2-
10	PD3 RTN			GND
11	PD3+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3+
12	PD3-			Computer to Peripheral LVDS Data 3-
13	PCK RTN			GND
14	PCK+	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK-			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN+	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN-			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0+
21	PDR0-			Peripheral to Computer LVDS Data 0-
22	PDR1 RTN			GND
23	PDR1+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1+
24	PDR1-			Peripheral to Computer LVDS Data 1-
25	PDR2 RTN			GND
26	PDR2+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2+
27	PDR2-			Peripheral to Computer LVDS Data 2-
28	PDR3 RTN			GND
29	PDR3+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3+
30	PDR3-			Peripheral to Computer LVDS Data 3-
31	PCKR RTN			GND
32	PCKR+	Reverse Dir Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR-			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR+	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Control +
36	PCNR-			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIGURE 12

FIGURE 13

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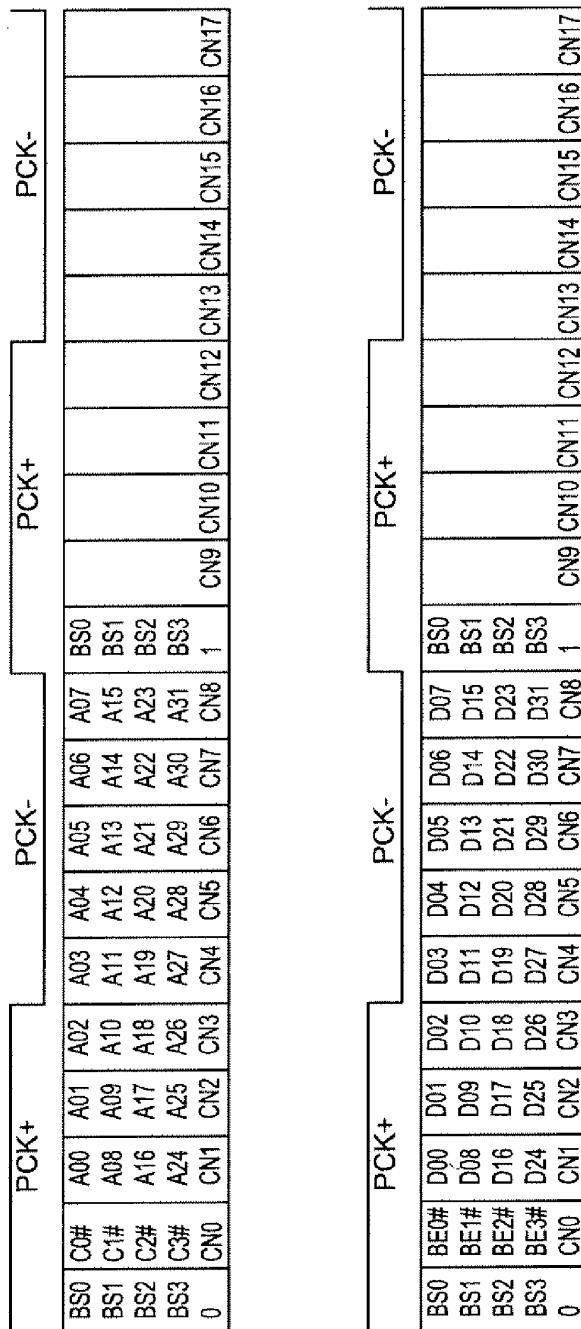


FIGURE 14

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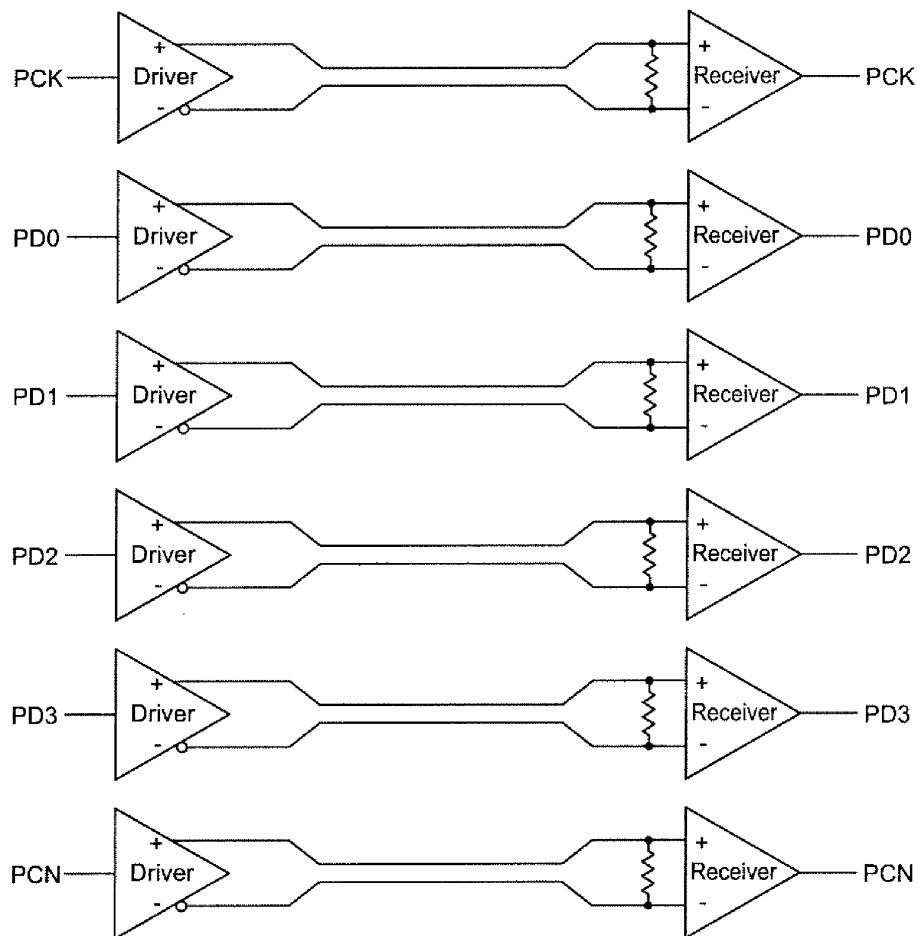


FIGURE 15



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Name	Type	Pins	Description
AD[31:0]	TS	32	Multiplexed Address/Data. AD is driven to a valid state when GNT# is asserted.
C/BE[3:0]#	TS	4	Multiplexed Command/Byte Enables. For a two-address transaction, 1st address phase carries the command, and the 2nd address phase carries the transaction type C/BE is driven to a valid state when GNT# is asserted.
FRAME#	STS	1	Indicates beginning and duration of a PCI transaction. When the bus is idle, FRAME# is driven to High for 1 cycle. A pull-up resistor sustains STS signal.
IRDY#	STS	1	Initiator Ready. IRDY# is driven High for 1 cycle if bus is idle, and the state is sustained by a pull-up resistor.
TRDY#	STS	1	Target Ready. When bus is idle, TRDY# is driven High for 1 cycle if bus is idle. An external pull-up resistor sustains STS signal.
DEVSEL#	STS	1	Device Select. DEVSEL# is asserted by target to indicate it is ready to accept the transaction. HIC decodes address of a transaction to decide the need to assert DEVSEL#. As an initiator, HIC waits for 5 cycles to detect assertion of DEVSEL# by the target; otherwise HIC terminates with a master abort. DEVSEL# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
STOP#	STS	1	Target request to stop transaction. There are 3 cases: STOP#, TRDY# & DEVSEL# asserted: disconnect with data transfer Only STOP# & DEVSEL# asserted: request initiator to retry later Only STOP# asserted: target abort STOP# is driven High for 1 cycle when bus is idle, and the state is sustained by a pull-up resistor.
PAR	TS	1	Even parity for 36 bits of AD & C/BE#. PAR is sent one cycle after address or data is valid. In write transaction, initiator sends PAR one cycle after write data is valid. In read transaction, target sends PAR one cycle after read data is valid.
LOCK#	Input	1	Initiator request lock on target downstream. LOCK# is asserted 1 clock cycle after address phase by an initiator wanting to perform an atomic operation that take more than one transaction to complete. HIC passes the LOCK# request to the secondary PCI bus. HIC does not drive LOCK# or propagate LOCK# upstream.
IDSEL#	Input	1	Chip Select for Type 0 configuration access. During a Type 0 configuration transaction, the initiator asserts IDSEL# during the address phase to select HIC. HIC responds by asserting DEVSEL#.
PERR#	STS	1	Data Parity Error on all transactions except Special Cycle. PERR# is driven one clock cycle after PAR. PERR# is asserted by target during write transactions, and by initiator during read transactions.
SERR#	OD	1	System Error. HIC asserts SERR# under the following conditions: Address parity error. Secondary bus SERR# asserted. Posted write transaction: data parity error on target bus. Posted write transaction discarded. Master abort. Target abort Delayed read or write transaction discarded, and Delayed transaction master timeout.
REQ#	TS	1	Request for bus. If a target retry or disconnect is received in response to initiating a transaction, HIC deasserts REQ# for at least 2 cycles before asserting it again.
GNT#	Input	1	Bus is granted to HIC. HIC can initiate transaction if GNT# is asserted and the bus is idle. When HIC is not requesting bus and GNT# is asserted, HIC must drive AD, C/BE, and PAR to valid logic levels.
CLKRUN#	I/OD	1	Input indicating clock status. HIC can request the central clock resource to start, speed up or maintain the PCI clock. There are 3 clocking states: Clock running, Clock about to stop/slow down, and Clock stopped/slowed.
PCICK	Input	1	PCI Clock. All inputs are sampled on the rising edge of PCICK. Frequency

FIGURE 16

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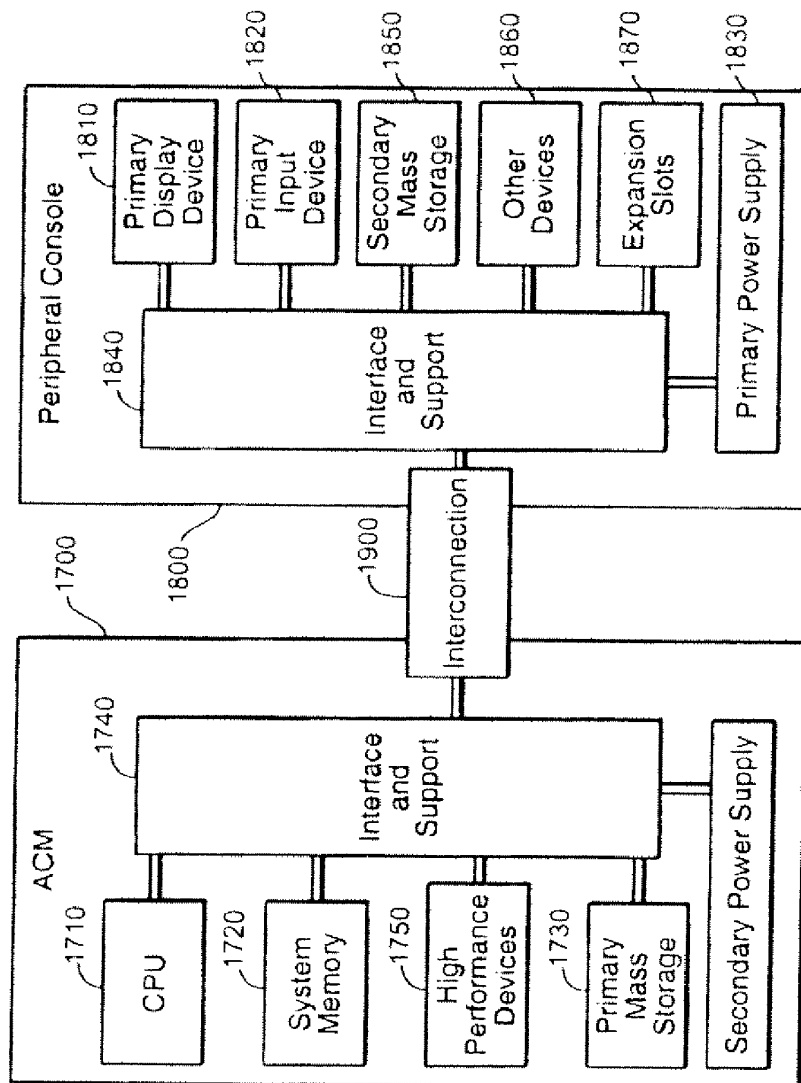


FIGURE 17

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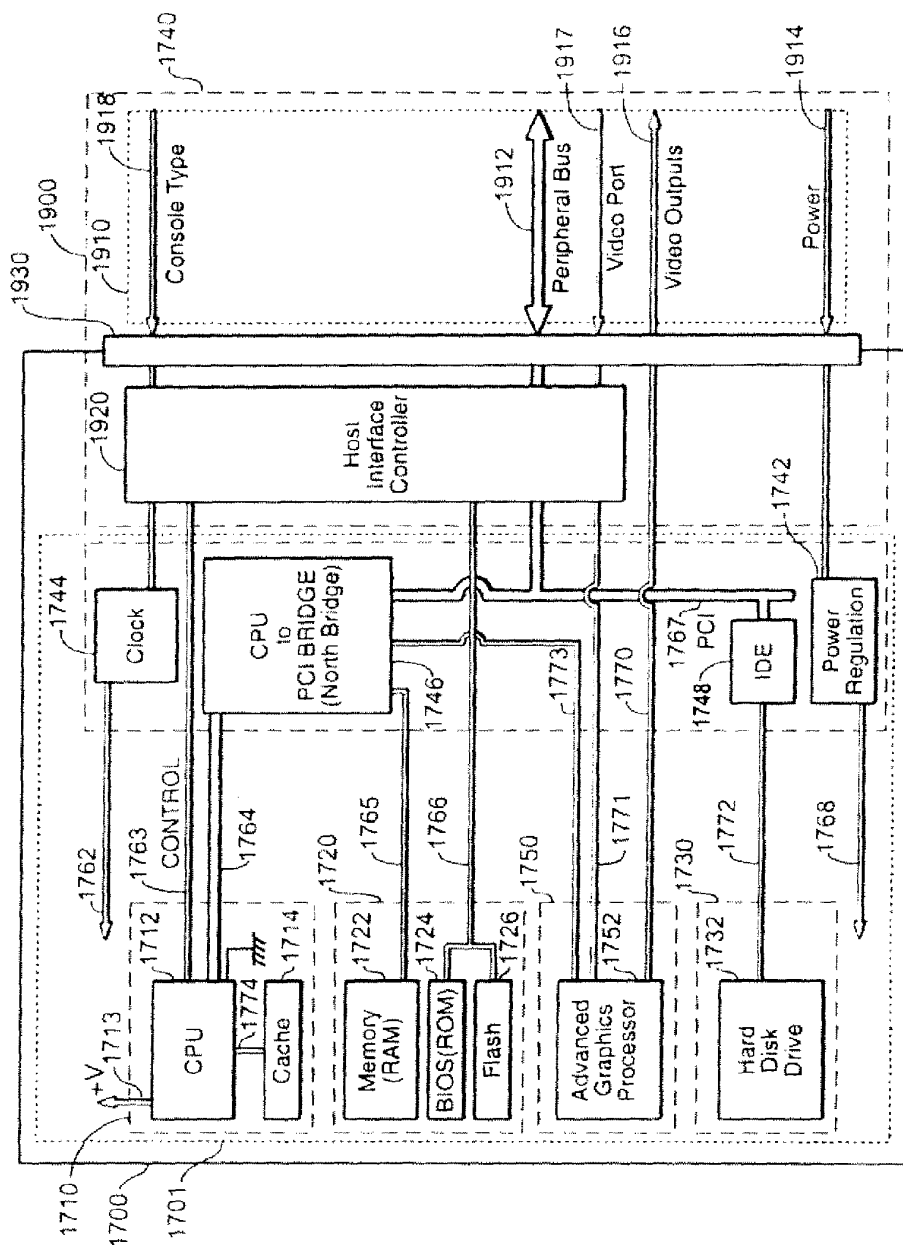


FIGURE 18

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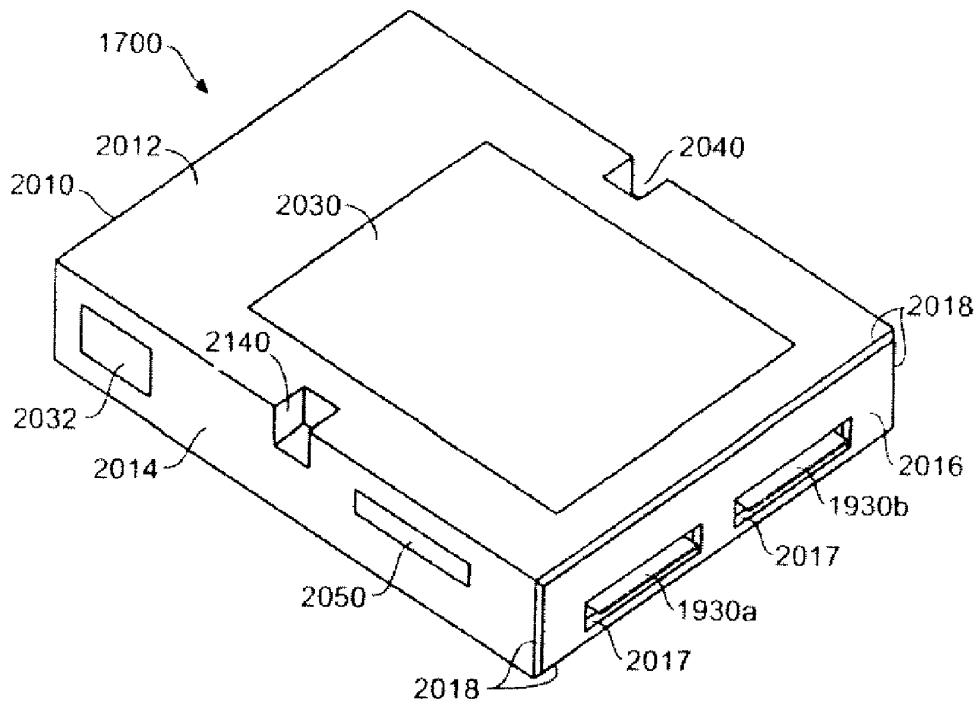


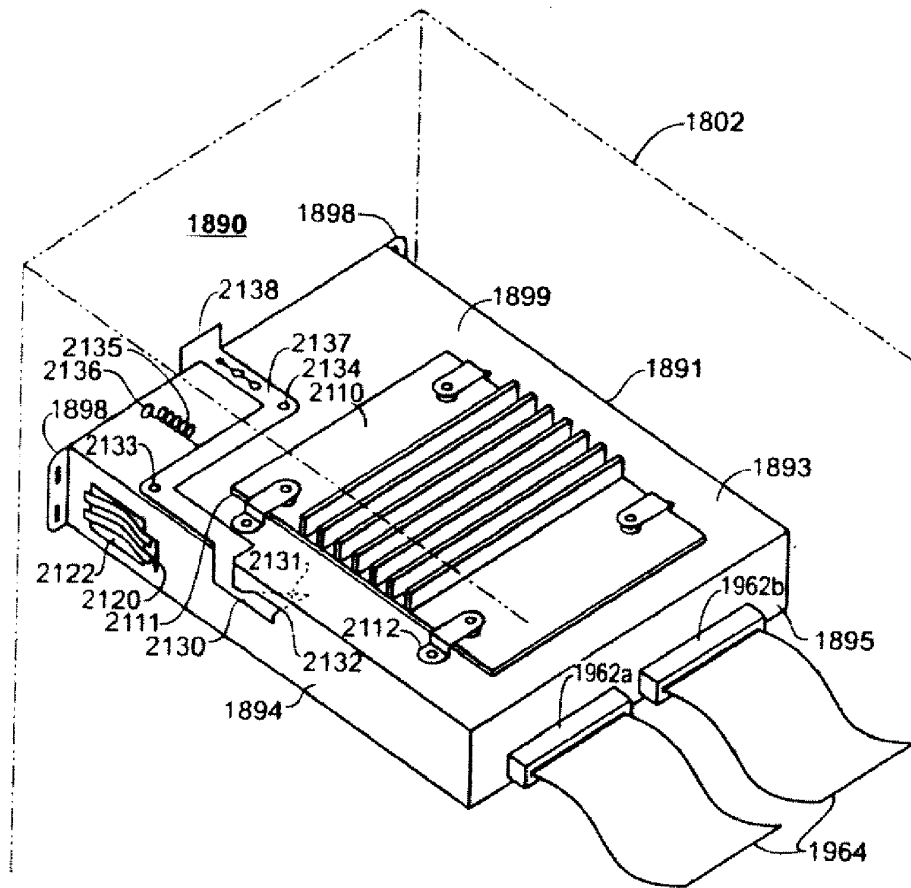
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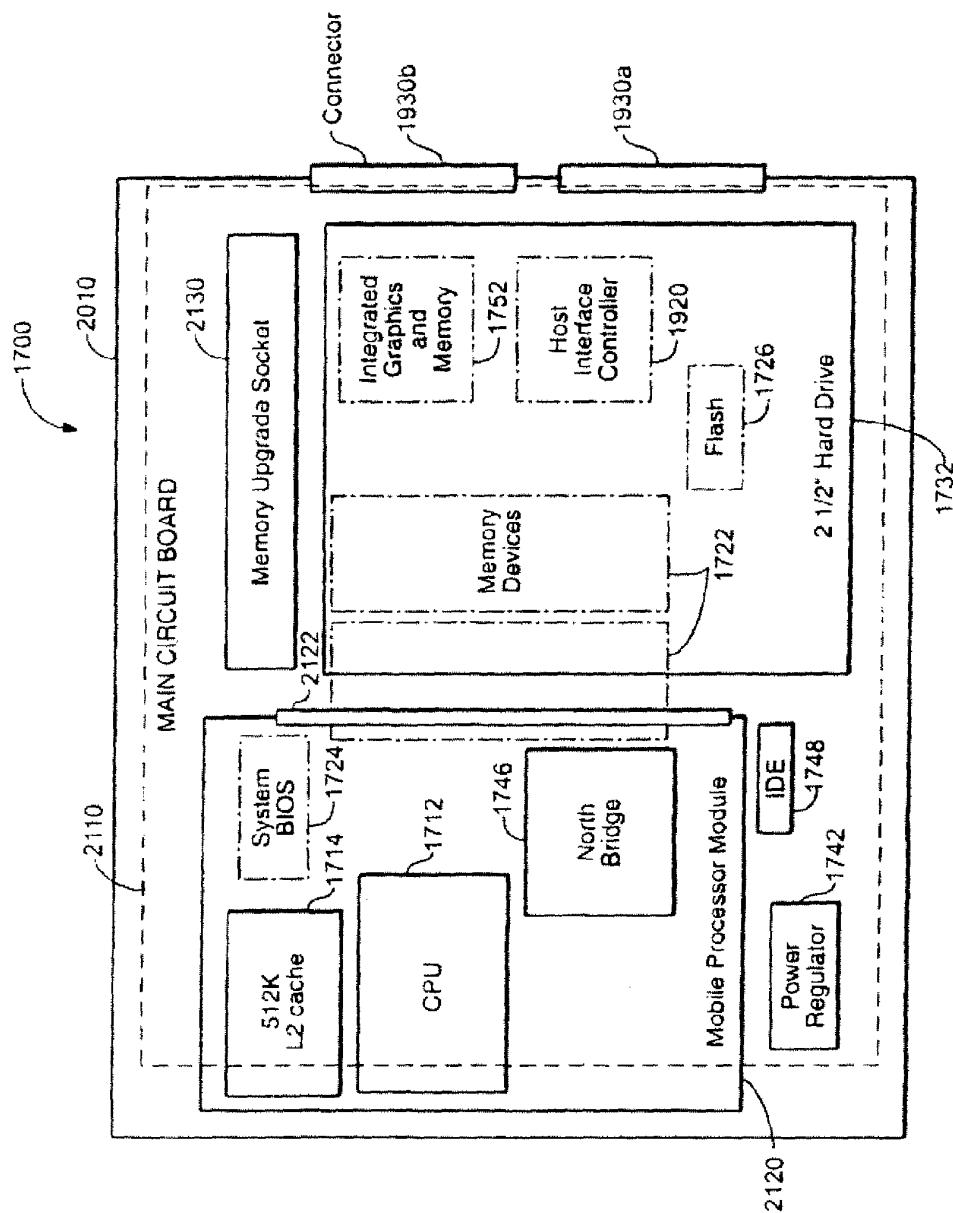


FIGURE 20

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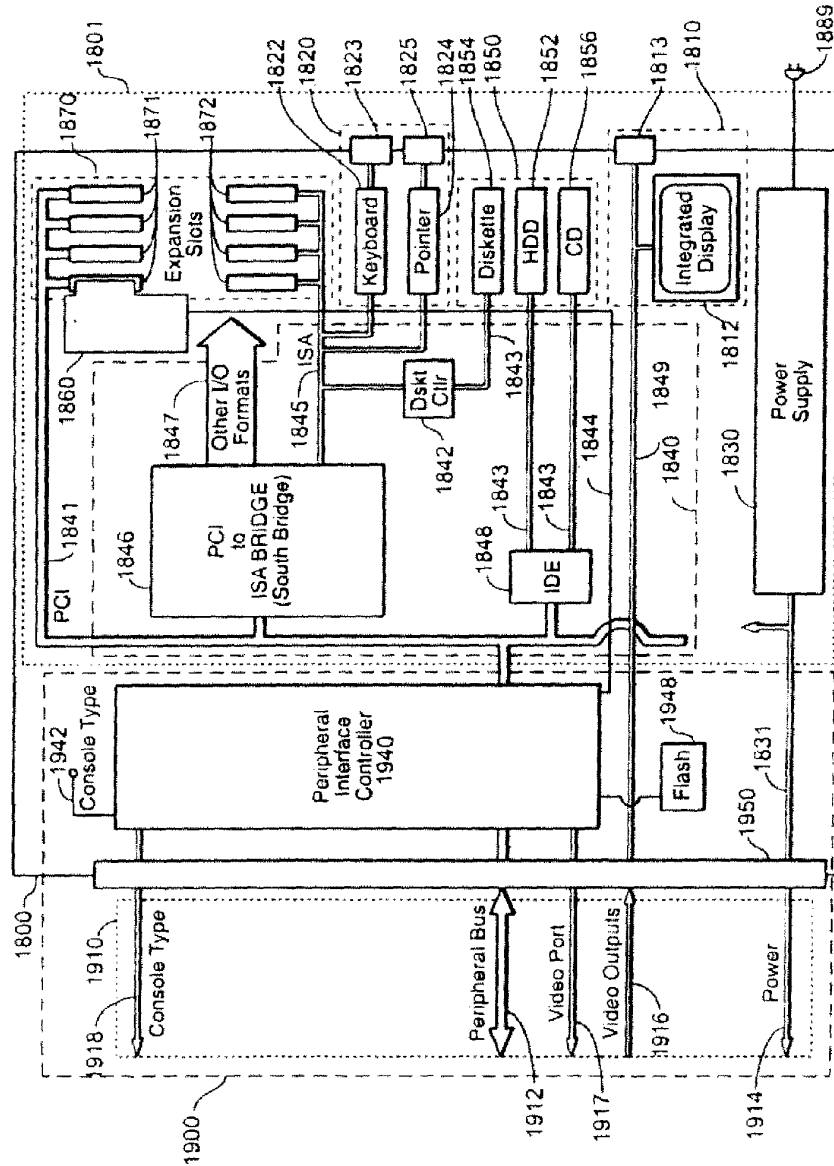


FIGURE 21

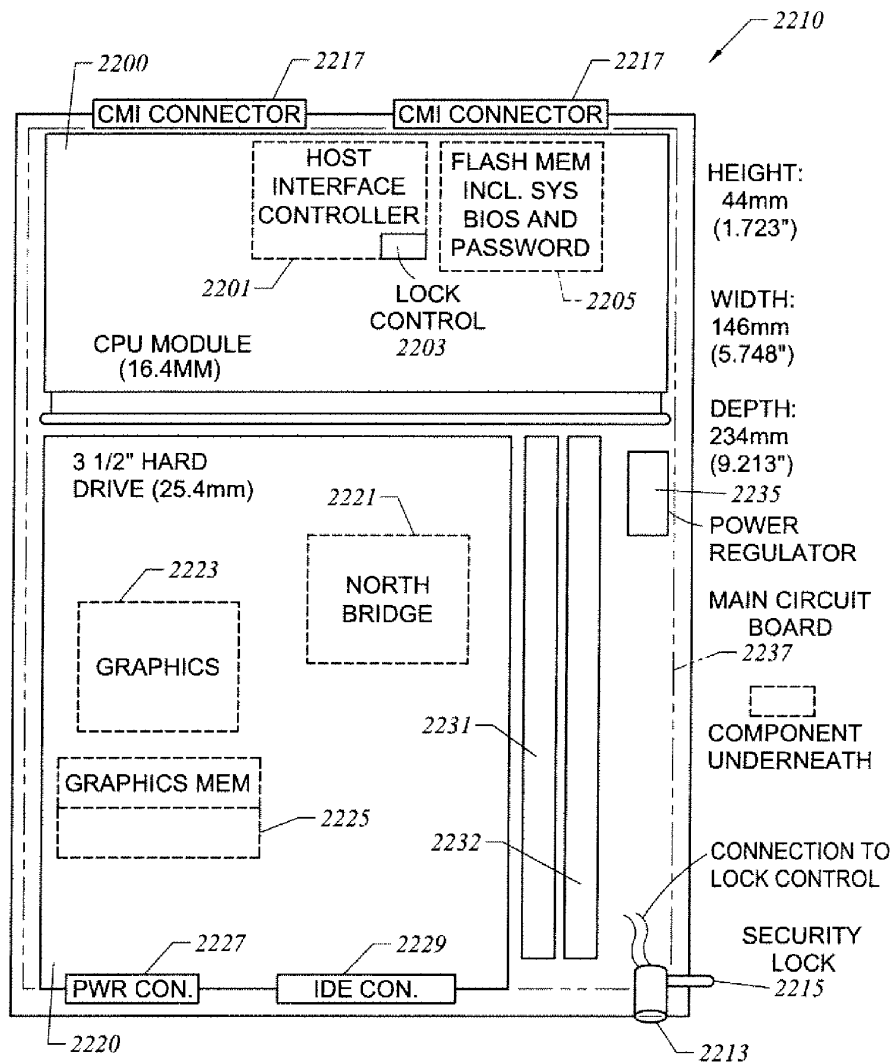


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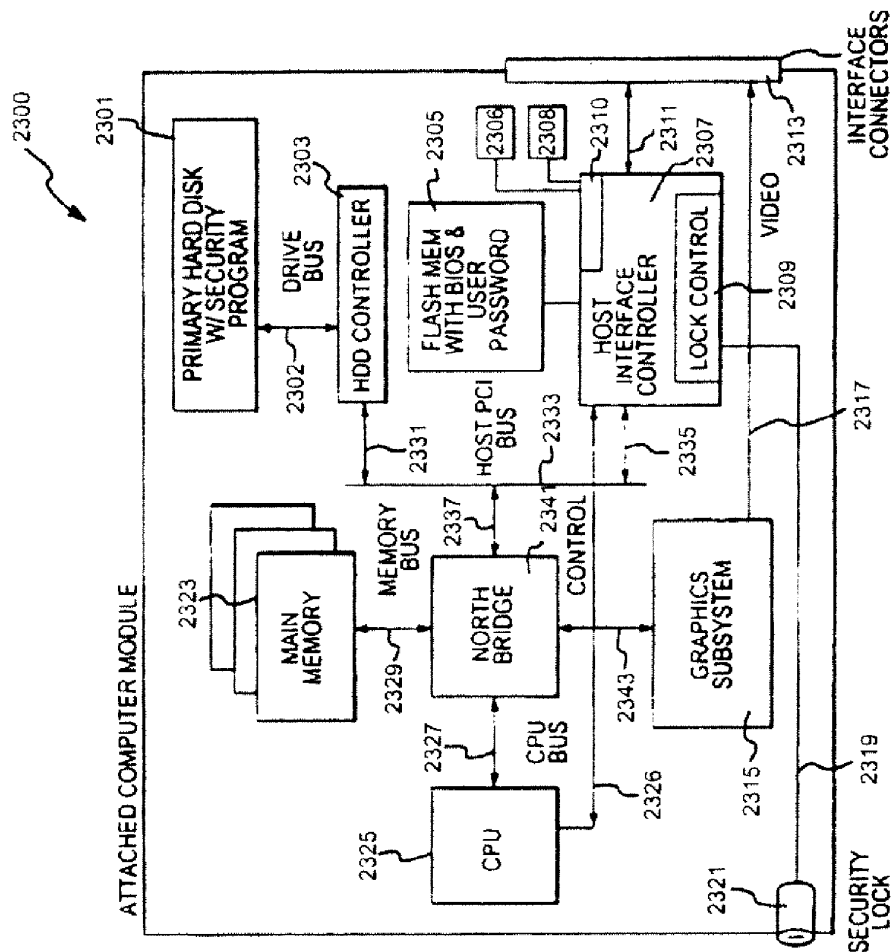


FIGURE 23

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**MULTIPLE MODULE COMPUTER SYSTEM  
AND METHOD INCLUDING DIFFERENTIAL  
SIGNAL CHANNEL COMPRISING  
UNIDIRECTIONAL SERIAL BIT CHANNELS  
TO TRANSMIT ENCODED PERIPHERAL  
COMPONENT INTERCONNECT BUS  
TRANSACTION DATA**

**CROSS REFERENCE TO RELATED  
APPLICATIONS**

This application is a continuation of U.S. application Ser. No. 12/077,503 filed Mar. 18, 2008 now U.S. Pat. No. 7,676,624, which is a continuation of U.S. nonprovisional application Ser. No. 11/166,656, filed Jun. 24, 2005 (Now U.S. Pat. No. 7,376,779), which is a continuation of U.S. nonprovisional application Ser. No. 11/097,694, filed Mar. 31, 2005 (Now U.S. Pat. No. 7,363,415), which is a continuation of U.S. nonprovisional application Ser. No. 10/772,214, filed Feb. 3, 2004 (Now U.S. Pat. No. 7,099,981), which is a continuation of U.S. nonprovisional application Ser. No. 09/569,758, filed May 12, 2000 (Now U.S. Pat. No. 6,718,415), and which claimed priority to U.S. Provisional Application No. 60/134,122 filed May 14, 1999. These applications are hereby incorporated by reference in their entirety.

**BACKGROUND OF THE INVENTION**

The present invention relates to computing devices. More particularly, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the

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computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as “laptop” computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have “total” computing power, where the desktop serves as a “regular” computer and the laptop serves as a “portable” computer. Purchasing both computers is often costly and runs “thousands” of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to “zip” up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for “on the road” use and a docking station that houses the portable computer for office use.

Similar to separate desktop and portable computers, there is no commonality between two desktop computers. To date, most personal computers are constructed with a single motherboard that provides connection for CPU and other components in the computer. Dual CPU systems have been available through Intel’s slot 1 architecture. For example, two Pentium II cartridges can be plugged into two “slot 1” card slots on a motherboard to form a Dual-processor system. The two CPU’s share a common host bus that connects to the rest of the system, e.g. main memory, hard disk drive, graphics subsystem, and others. Dual CPU systems have the advantage of increased CPU performance for the whole system. Adding a CPU cartridge requires no change in operating systems and application software. However, dual CPU systems may suffer limited performance improvement if memory or disk drive bandwidth becomes the limiting factor. Also, dual CPU systems have to time-share the processing unit in running multiple applications. CPU performance improvement efficiency

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also depends on software coding structure. Dual CPU systems provide no hardware redundancy to help fault tolerance. In running multiple applications, memory and disk drive data throughput will become the limiting factor in improving performance with multi-processor systems.

The present invention generally relates to computer interfaces. More specifically, the present invention relates to an interface channel that interfaces two computer interface buses that operate under protocols that are different from that used by the interface channel.

Interfaces coupling two independent computer buses are well known in the art. A block diagram of a computer system utilizing such a prior art interface is shown in FIG. 5. In FIG. 5, a primary peripheral component interconnect (PCI) bus 505 of a notebook PC 500 is coupled to a secondary PCI bus 555 in a docking system 550 (also referred to as docking station 550) through high pin count connectors 501 and 502, which are normally mating connectors. The high pin count connectors 501 and 502 contain a sufficiently large number of pins so as to carry PCI bus signals between the two PCI buses without any translation. The main purpose for interfacing the two independent PCI buses is to allow transactions to occur between a master on one PCI bus and a target on the other PCI bus. The interface between these two independent PCI buses additionally includes an optional PCI to PCI bridge 560, located in the docking station 550, to expand the add on capability in docking station 550. The bridge 560 creates a new bus number for devices behind the bridge 560 so that they are not on the same bus number as other devices in the system thus increasing the add on capability in the docking station 550.

An interface such as that shown in FIG. 5 provides an adequate interface between the primary and secondary PCI buses. However, the interface is limited in a number of ways. The interface transfers signals between the primary and secondary PCI buses using the protocols of a PCI bus. Consequently, the interface is subject to the limitations under which PCI buses operate. One such limitation is the fact that PCI buses are not cable friendly. The cable friendliness of the interface was not a major concern in the prior art. However, in the context of the computer system of the present invention, which is described in the present inventor's (William W. Y. Chu's) application for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998 and incorporated herein by reference, a cable friendly interface is desired for interfacing an attached computer module (ACM) and a peripheral console of the present invention. Furthermore, as a result of operating by PCI protocols, the prior art interface includes a very large number of signal channels with a corresponding large number of conductive lines (and a similarly large number of pins in the connectors of the interface) that are commensurate in number with the number of signal lines in the PCI buses which it interfaces. One disadvantage of an interface having a relatively large number of conductive lines and pins is that it costs more than one that uses a fewer number of conductive lines and pins. Additionally, an interface having a large number of conductive lines is bulkier and more cumbersome to handle. Finally, a relatively large number of signal channels in the interface renders the option of using differential voltage signals less viable because a differential voltage signal method would require duplicating a large number of signal lines. It is desirable to use a low voltage differential signal (LVDS) channel in the computer system of the present invention because an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise, including electromagnetic interferences (EMI), than a PCI channel.

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The term LVDS is herein used to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.

Thus, what is needed are computer systems that can have multiple computer modules. Each computer module has dedicated memory and disk drive, and can operate independently.

## BRIEF SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

In a specific embodiment, the present invention provides a computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site, e.g., computer module bay. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.

In an alternative specific embodiment, the present invention provides a multi-processing computer system. The system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to one of the connectors. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, a mass storage device coupled to the processing unit, and a video output coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system. A video switch circuit is coupled to each of the computer modules through the video output. The video switch is configured to switch a video signal from any one of the computer modules to a display.

Numerous benefits are achieved using the present invention over previously existing techniques. In one embodiment, the invention provides improved processing and maintenance features. The invention can also provide increased CPU performance for the whole system. The invention also can be implemented without changes in operating system and application software. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner.

In another embodiment, the invention provides at least two users to share the same modular desktop system. Each user operates on a different computer module. The other peripheral devices, i.e. CDROM, printer, DSL connection, etc. can be shared. This provides lower system cost, less desktop space and more efficiency. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

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In still further embodiments, the present invention provides methods of using multiple computer modules.

The present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock line and a plurality of bit lines for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

The present invention overcomes the aforementioned disadvantages of the prior art by interfacing two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed

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address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further



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embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent “finger print” on the attached computer module.

In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module (“ACM”) into a bay of a modular computer system. The ACM has a microprocessor unit (e.g. microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., flat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached Figs.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified block diagram of a computer system according to an alternative embodiment of the present invention;

FIG. 3 is a simplified block diagram of a computer system according to a further alternative embodiment of the present invention, and

FIG. 4 is a simplified flow diagram of a method according to an embodiment of the present invention.

FIG. 5 is a block diagram of a computer system using a prior art interface between a primary and a secondary PCI bus.

FIG. 6 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 7 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 8 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

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FIG. 9 is a block diagram of one embodiment of the host interface controller and the peripheral interface controller of the present invention.

FIG. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

FIG. 11 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 12 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

FIG. 13 is a table showing the information transmitted on the XPBus during two clock cycles of the XPBus in one embodiment of the present invention where 10 data bits transmitted in each clock cycle of the XPBus.

FIG. 14 is a table showing information transmitted on the XPBus during four clock cycles of the XPBus in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBus.

FIG. 15 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals.

FIG. 17 is a block diagram of one embodiment of a computer system employing the present invention.

FIG. 18 is a block diagram of an attached computing module (ACM).

FIG. 19 illustrates an external view of one embodiment of an ACM.

FIG. 19b illustrates one possible embodiment of a computer bay.

FIG. 20 illustrates the internal component layout for one embodiment of an ACM.

FIG. 21 is a block diagram of a peripheral console (PCON).

FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention; and

FIG. 23 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

According to the present invention, a technique including a method and device for multi-module computing is provided. In an exemplary embodiment, the present invention provides a system including a plurality of computer modules that can independently operate to provide backup capability, dual processing, and the like.

FIG. 1 is a simplified diagram of a computer system 100 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 100 includes an attached computer module (i.e., ACM) 113, a desktop console 101, among other elements. The computer system also has another ACM module 117. Each ACM module has a respective slot 121, 119, which mechanically houses and electrically couples each ACM to the computer console. Also shown is a display 111, which connects to the console. Additionally, keyboard 109 and mouse 115 are also shown. A second display 102, keyboard 105, and mouse 107 can be coupled to the console in some optional embodiments to allow more than one user to operate the computer system. The computer system is modular and has a variety of components that are removable. Some

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of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, each ACM **113** includes computer components, as will be described below, including a central processing unit (“CPU”). IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) **121** is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to the ACM. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998, commonly assigned, and hereby incorporated by reference for all purposes.

In a specific embodiment, the present multiple computer module system has a peripheral console that has two or more computer bays that can receive a removable computer module or ACM. Multiple computer module system can function as a personal computer with only one ACM and the peripheral console. The second and additional ACM can be added later to increase overall system performance and reliability. The ACM operates independently as self-contained computer, communicates with each other through a high-speed serial communication and share most peripheral devices within the peripheral console. Each ACM controls its independent graphics subsystem and drives separate video output signals. A practical implementation is a dual ACM system. In a dual ACM system, two monitors can be used to display the two ACMs’ graphics outputs at the same time. For a single monitor, a RGB switch is used to switch between the video outputs of the two ACMs and can be controlled by a command from the user. Similarly, input devices (i.e. keyboard and mouse) are switched between the two computer systems with a command from the user. Command from the user can be in the form of either a dedicated key on the keyboard or a special icon on the screen that the mouse can click on.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive (“HDD”) that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present system are described in more detail below. In a dual ACM system, the primary ACM can connect directly to the peripheral board in the peripheral console. The second ACM can connect either directly or indirectly to the peripheral board. For indirect connection, a receptacle board is added to allow a cable connection to the peripheral board. This is to facilitate the mechanical positioning of the second ACM inside the computer chassis. The receptacle board approach can even be

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used for the primary ACM if a high bandwidth peripheral bus, e.g. PCI Bus, is not connected from the primary ACM to the peripheral board.

The shared peripheral console has a chassis and a motherboard that connects the following devices:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. RGB monitor,
- 3) Add-on means, e.g. PCI add-on slots,
- 4) Two Computer Module Bays (CMB) with connectors to two ACMs,
- 5) A serial communication Hub controller that interfaces to serial communication controller of both ACMs,
- 6) Shared storage subsystem, e.g. Floppy drive, CDROM drive, DVD drive, or 2nd Hard Drive,
- 7) Communication device, e.g. modem,
- 8) Power supply, and others.

The computer bay is an opening in the peripheral console that receives an ACM. CMB provides mechanical protection to ACM, mechanical alignment for connector mating, mechanical locking system to prevent theft and accidental removal, and connectors at the end of the opening for connecting to ACM. The interface bus between ACM and the peripheral console has a video bus, peripheral connections, serial communication connection, control signals and power connection. Video bus includes video output of graphics devices, i.e. analog RGB and control signals for monitor. Power connection supplies the power for ACM.

An implementation of peripheral sharing is the use of Ethernet controllers to bridge the communication between the two ACMs. Some of the peripheral devices residing in the peripheral console are shown in the simplified diagram of FIG. 2. As shown, the diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, alternatives, and modifications. As shown, a primary ACM **203** is connected to PCI peripheral devices in the peripheral console through the PCI bus **225** that passes through the connection between primary ACM **203** and peripheral console **201**. As shown, ACM has a CPU module **207** coupled to the PCI bus through a North Bridge **211**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, peripheral controller **213** is coupled to BIOS/flash memory **217**. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module **215**. Among other elements, the ACM includes north bridge **215**, graphics subsystem **223** (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module **215** is the PCI bus. In a specific embodiment, North Bridge unit **211** often couples to a computer memory **209**, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as part of a P114XE controller from Intel, for



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example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **215** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **215** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection.

The ACM also has a network controller, which can be an Ethernet controller **219**, which is coupled to the North Bridge through the PCI bus. The North Bridge is coupled to the CPU. The Ethernet controller can be a 10/100 Base, such as Intel's 82559 or the like. Other types of network connection devices can also be used. For example, the invention can use Gbit Ethernet 1394, and USB 2.0. The network controller couples to a hub **233** in the console, which includes shared peripheral system **201**.

Also shown is the second ACM **205**. The second ACM has the same or similar components as the first ACM. Here, like reference numerals have been used for easy cross-referencing, but is not intended to be limiting. In some embodiments, the secondary ACM is not connected to the PCI bus in the peripheral console directly. The secondary ACM **219** accesses peripheral devices controlled by the primary ACM through the Ethernet connection to the primary ACM, e.g. CD-ROM, or PCI modem. The implementation is not restricted to Ethernet serial communication and can use other high-speed serial communication such as USB 2.0, and 1394. The Ethernet hub is coupled to an external output port **235**, which connects to an external network.

The primary hard disk drive in each ACM can be accessed by the other ACM as sharable hard drive through the Ethernet connection. This allows the easy sharing of files between the two independent computer modules. The Ethernet Hub Controller provides the high-speed communication function between the two computer modules. Ethernet data bandwidth of 100 Mbit/sec allows fast data communication between the two computer modules. The secondary ACM access peripheral devices of the primary ACM through the network connection provided by Ethernet link. The operating system, e.g. Windows98, provides the sharing of resources between the two ACMs. In some embodiments, critical data in one ACM can be backup into the other ACM.

The Ethernet hub also couples to PCI bus **239**, which connects to PCI devices **241**, **243**, e.g., modem, SCSI controller. A flash memory **242** can also be coupled to the PCI bus. The flash memory can store passwords and security information, such as those implementations described in U.S. Ser. No. 09/183,493, which is commonly owned, and hereby incorporated by reference. The hub **233** also couples to an I/O control **237**, which connects to keyboard/mouse switch **245**, which couples to keyboard/mouse **247**. Optionally, the keyboard/mouse switch also couples to a second keyboard/house

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**259** via PS2 or USB signal line **251**. The keyboard/mouse switch has at least a first state and a second state, which allow operation of respectively multiple keyboards or a single keyboard. The switch also couples to each I/O controller **221** in each ACM via lines **253**, **255**. The I/O control **237** also couples to an RGB switch **257**, which allows video signals to pass to the first monitor **259**. Alternatively, the RGB switch couples to a second monitor **261**. The RGB switch includes analog video switches such as MAXIM's MAX4545.

The peripheral system **201** also has an independent power supply **231** for each ACM. Each power supply provides power to each ACM. As merely an example, the power supply is a MICRO ATX 150W made by ENLIGHT, but can be others. The power supply is connected or coupled to each ACM through a separate line, for example. The independent power supply allows for independent operation of each ACM in some embodiments.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 3 is a simplified block diagram **300** of a computer system according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. Like reference numerals are used in this Fig. as the previous Figs. for easy referencing, but are not intended to be limiting. As shown, each ACM includes common elements as the previous Fig. A primary ACM **203** is connected to PCI peripheral devices in the peripheral console through the PCI bus **225** that passes through the connection between primary ACM **203** and peripheral console **201**. As shown, ACM has a CPU module **207** coupled to the PCI bus through a North Bridge **211**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, peripheral controller **213** is coupled to BIOS/flash memory **217**. Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The ACM has the hard drive module **215**. Among other elements, the ACM includes north bridge **215**, graphics subsystem **223** (e.g., graphics accelerator, graphics memory), an IDE controller, and other components. Adjacent to and in parallel alignment with the hard drive module **215** is the PCI bus. In a specific embodiment, North Bridge unit **211** often couples to a computer memory **209**, to the graphics subsystem, and to the peripheral controller via the PCI bus. Graphics subsystem typically couples to a graphics memory, and other elements. IDE controller generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is

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embodied as part of a P114XE controller from Intel, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **215** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **215** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

Among other features, the computer system includes an ACM with security protection.

The ACM also has a network controller, which can be coupled to a serial port **302**, which is coupled to the PCI bus in the ACM. The serial port is coupled to the peripheral console through a serial controller **301** in the serial console. The serial controller is connected to PCI bus **239**. The serial controller is also coupled to a serial hub controller **303**, which is coupled to the PCI bus and a second ACM. In a specific embodiment, a receptacle board **310** is added to connect to the second ACM. The purpose of the receptacle board is to allow a cable connection **307** to the peripheral board **300**. The cable connection is possible because the signals needed to connect to the peripheral board can be limited to video, I/O, serial communication, and power. The serial communication controller can be placed on the receptacle board and not in the ACM. As shown, the serial bus controller couples to the PCI bus. The receptacle board also couples to power, graphics subsystem, I/O controller, and other elements, which may be on a common bus. The overall operation of the present configuration is similar to the previous one except it operates in serial communication mode.

The Dual ACM system can support different usage models:

1. One user using both ACMs concurrently with 1 or 2 monitors, and a common keyboard/mouse.
2. Two users using the two separate ACMs at the same time with separate monitors and keyboard/mouse. The 2 users share peripherals, e.g., printer, CDROM, and others. The two users share external networking.

To support 1 monitor for both ACMs, a video switch in the peripheral console is used to switch between the video outputs of the two ACMs. The system can be set to support either 1 monitor or 2-monitor mode. The user presses a special key on the keyboard or a special icon on the screen to switch the screen display from one ACM to the other. This same action causes the keyboard and mouse connections to switch from one ACM to the other ACM.

A dual ACM system can save space, wiring, and cost for a 2-person PC setup, with the added benefit that both PC systems can be accessed from one user site for increased system performance if the other user is not using the system. Files can be copied between the primary drive of both system and provides protection against a single ACM failure. Software needs to be developed to manage the concurrent use of two PC subsystems, the automatic sharing of selected files between the two systems, and fault tolerance.

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The design with more than two computer modules can be implemented with the use of multi-port, serial communication hub controller and multi-port I/O switches. In one embodiment, a peripheral console has four computer bays for four separate computer modules. The computer modules communicate through a four port Ethernet hub. The video, keyboard, and mouse switch will cycle through the connection from each computer module to the external monitor, keyboard, and mouse with a push button sequentially. This embodiment is useful for a server that performs different functions concurrently, e.g. email, application hosting, web hosting, firewall, etc.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 4 is a simplified diagram of a method according to an embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The present diagram illustrates an automatic file backup procedure from one computer module to the other. As shown, a user selects (step **401**) a certain file in one of the computer module for automatic backup. Next, the method determines if another module is available, step **403**. If so, the method in the originating module requests the other computer module to create (step **405**) backup file. Alternatively, the method alerts the user of the missing or malfunctioning module, step **429**. The method then has the user try later **431**, once the missing or malfunctioning module has been replaced or repaired. Next, the method determines if there is sufficient storage available in the other computer module for the backup files. If so, the method goes to the next step. (Alternatively, the method prompts (step **433**) a message to the user indicating that the storage is full.) In the next step, the method stores the backup file in memory of the other module. After the backup file has been successfully created (step **409**), the software in the originating ACM sets a timer to check (step **411**) for file modification via branches **423**, **427** through continue, step **425** process. If a file selected for backup has been modified (step **415**), then the file is automatically back up to the other ACM again, step **417**. Alternatively, the method returns to step **411** through branch **421**.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

FIG. 6 is a block diagram of one embodiment of a computer system **600** using the interface of the present invention. Computer system **600** includes an attached computer module (ACM) **605** and a peripheral console **610**, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application

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on Sep. 8, 1998 and incorporated herein by reference. The ACM 605 and the peripheral console 610 are interfaced through an exchange interface system (XIS) bus 615. The XIS bus 615 includes power bus 616, video bus 617 and peripheral bus (XPBus) 618, which is also herein referred to as an interface channel. The power bus 616 transmits power between ACM 605 and peripheral console 610. In a preferred embodiment power bus 616 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 617 transmits video signals between the ACM 605 and the peripheral console 610. In a preferred embodiment, the video bus 617 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 618 is coupled to host interface controller (HIC) 619 and to peripheral interface controller (PIC) 620, which is also sometimes referred to as a bay interface controller.

In the embodiment shown in FIG. 6, HIC 619 is coupled to an integrated unit 621 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 7, the CPU 705 and north bridge 710 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 8, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 810 includes a PIC and a south bridge.

FIG. 9 is a more detailed block diagram of one embodiment of an HIC 905 and a PIC 955 of the present invention. HIC 905 includes a peripheral component interconnect (PCI) bus controller 910, an XPBus controller 915, a phase lock loop (PLL) clock 920 and an input/output (IO) control 925. Similarly, PIC 955 includes a PCI bus controller 960, an XPBus controller 965, a PLL clock 970 and an IO control 975. PCI bus controllers 910 and 960 are coupled to the primary and secondary PCI buses 930 and 980, respectively, and manage PCI transactions on the primary and secondary PCI buses 930 and 980, respectively. Similarly, XPBus Controllers 915 and 965 are coupled to XPBus 990. XPBus controller 915 drives the PCK line 991 and PD[0:3] and PCN lines 992 while XPBus controller 965 drives the PCKR lines 993, the PDR [0:3] and PCNR lines 994 and the RESET# line 995.

PCI bus controller 910 receives PCI clock signals from the primary PCI bus 930 and is synchronized to the PCI clock. However, as indicated in FIG. 9, the XPBus controller 915 is asynchronous with the PCI bus controller 910. Instead, the XPBus controller receives a clock signal from the PLL clock 920 and is synchronized therewith. PLL clock 920 generates a clock signal independent of the PCI clock. The asynchronous operation of the PCI bus and the XPBus allows the PCI Bus to change in frequency, for example as in a power down situation, without directly affecting the XPBus clocking. In the embodiment shown in FIG. 9, the PLL clock 920 generates a clock signal having a frequency of 66 MHz, which is twice as large as the 33 MHz frequency of the PCI clock. (The clock signal generated by the PLL clock may have a clock speed different from, including lower than, 66 MHz. For example, in another embodiment, which is discussed in greater detail below, the PLL clock 920 generates a clock signal having a frequency of 132 MHz.)

The XPBus 990 operates at the clock speed generated by the PLL clock 920. Therefore, PCK, the clock signal from the XPBus controller 915 to XPBus controller 965 has the same frequency as the clock signal generated by PLL clock 920.

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XPBus controller 965 receives the PCK signal after it has been buffered and operates at the clock speed of PCK. The buffered version of the clock signal PCK is used to generate the clock signal PCKR, the clock signal from the XPBus controller 965 to XPBus controller 915. Accordingly, PCKR also has the same frequency as that generated by the PLL clock 920. The synchronous operation of PCK and PCKR provides for improved reliability in the system. In another embodiment, PCKR may be generated independently of PCK and may have a frequency different from that of PCK. It is to be noted that even when PCKR is generated from PCK, the slew between PCK and PCKR cannot be guaranteed because of the unknown cable length used for the XPBus. For a cable that is several feet long, the cable propagation delay alone can be several nano seconds.

As indicated in FIG. 9, PLL clock 970 is asynchronous with the XPBus controller 965. Instead, PLL clock 970 independently generates a clock signal that is used as a PCI clock signal on the secondary PCI bus 980. The secondary PCI bus 980 operates at the same clock speed as the primary PCI bus 930, namely at a frequency of 33 MHz.

FIG. 10 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in FIG. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.

HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.

Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder 1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 10 operate at 33 MHz and 106 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/



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WR Cntl) **1015**. RD/WR controls **1014** and **1015** are involved in the transfer of PCI control signals between bus controller **1010** and the host PCI bus.

Bus controller **1010** is coupled to translator **1020**. Translator **1020** comprises encoders **1022** and **1027**, decoders **1023** and **1028**, control decoder & separate data path unit **1024** and control encoder & merge data path unit **1025**. As discussed above encoders **1022** and **1027** are part of slave data unit **1011** and master data unit **1016**, respectively, receive PCI address and data information from FIFOs **1012** and **1017**, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders **1023** and **1028** are part of slave data unit **1011** and master data unit **1016**, respectively, and format address and data information from receiver **1040** into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit **1025** receives PCI control signals from the slave RD/WR control **1014** and master RD/WR control **1015**. Additionally, control encoder & merge data path unit **1025** receives control signals from CPU CNTL & GPIO latch/driver **1090**, which is coupled to the CPU and north bridge (not shown in FIG. 10). Control encoder & merge data path unit **1025** encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter **1030**, which then transmits the control bits on the data lines PDR0 to PD3 and control line PCNR of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit **1024** receives control bits from receiver **1040** which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit **1024** separates the control bits it receives from receiver **1040** into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

Transmitter **1030** receives multiplexed parallel address/data (AID) bits and control bits from translator **1020** on the AD[31:0] out and the CNTL out lines, respectively. Transmitter **1030** also receives a clock signal from PLL **1050**. PLL **1050** takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 106 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 106 MHz rather than 33 MHz or having 104 rather than 32 multiplexed address/data lines.

The multiplexed parallel A/D bits and some control bits input to transmitter **1030** are serialized by parallel to serial converters **1032** of transmitter **1030** into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter **1033** into 10 bit packets and send out on control line PCN of the XPBus.

A 10x multiplier **1031** receives PCK, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCK into the parallel to serial converters **1032** and **1033**. The parallel to serial converters **1032** and **1033** perform bit shifting at 10 times the PCK rate to serialize the parallel bits into 10 bit packets. As the parallel to serial converters **1032** and **1033** shift bits at 10 times the PCK rate, the bit rate for the

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serial bits output by the parallel to serial converters is 10 times higher than PCK rate, i.e., 1060 MHz. However, the rate at which data packets are transmitted on the XPBus is the same as the PCK rate, i.e., 106 MHz. As the PCI buses operate at a clock and bit rate of 33 MHz, the XPBus has a clock rate that is twice as large and a bit rate per bit line (channel) that is 100 times as large as that of the PCI buses which it interfaces.

Receiver **1040** receives serial bit packets on data lines PDR0 to PDR3 and control line PCNR. Receiver **1040** also receives PCKR on the XPBus as well as the clock signal PCK from PLL **1050**. The synchronizer (SYNC) **1044** of receiver **1040** synchronizes the clock signal PCKR to the locally generated clock signal, PCK, in order to capture the bits received from the XPBus into PCK clock timing.

Serial to parallel converters **1042** convert the serial bit packets received on lines PDR0 to PDR3 into parallel address/data and control bits that are sent to decoders **1023** and **1028** and control decoder and separate data path unit **1024**, respectively. Serial to parallel converter **1043** receives control bit packets from control line PCNR, converts them to parallel control bits and sends the parallel control bits to control decoder & separate data path **1024**.

A 10x multiplier **1041** receives PCKR, multiplies it by a factor of 10 and feeds a clock signal 10 times greater than PCKR into the serial to parallel converters **1042** and **1043**. Because the bits on PDR0 to PDR3 and PCNR are transmitted at a bit rate of 10 times the PCKR rate, the serial to parallel converters **1042** and **1043** perform bit shifting at 10 times the PCKR rate to convert the 10 bit packets into parallel bits. It is to be noted that the rate at which bit packets are transmitted on the XPBus is the same as the PCKR rate, i.e., 106 MHz. The parallel data and control bits are thereafter sent to decoders **1023** and **1028** by way of the AD[3:0] in line and to control decoder & separate data path unit **1024** by way of CNTL in lines, respectively.

Reset control unit **1045** of HIC **1000** receives the signal RESET#, which is an independent system reset signal, on the reset line RESET#. Reset control unit **1045** then transmits the reset signal to the CPU CNTL & GPIO latch/driver unit **1090**.

As may be noted from the above, the 32 line host and secondary PCI buses are interfaced by 10 XPBus lines (PD0, PD1, PD2, PD3, PCN, PDR0, PDR1, PDR2, PDR3, PCNR). Therefore, the interface channel, XPBus, of the present invention uses fewer lines than are contained in either of the buses which it interfaces, namely the PCI buses. XPBus is able to interface such PCI buses without backup delays because the XPBus operates at a clock rate and a per line (channel) bit rate that are higher than those of the PCI buses.

In addition to receiving a reset signal, the CPU CNTL & GPIO latch/driver **1090** is responsible for latching input signals from the CPU and north bridge and sending the signals to the translator. It also takes decoded signals from the control decoder & separate data path unit **1024** and drives the appropriate signals for the CPU and north bridge.

In the embodiment shown in FIG. 10, video serial to parallel converter **1080** is included in HIC **1000**. In another embodiment, video serial to parallel converter **1080** may be a separate unit from the HIC **1000**. Video serial to parallel converter **1080** receives serial video data on line VPD and a video clock signal VPCK from line VPCK of video bus **1081**. It then converts the serial video data into 16 bit parallel video port data and the appropriate video port control signals, which it transmits to the graphics controller (not shown in FIG. 10) on the video port data [0:15] and video port control lines, respectively.

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HIC 1000 handles the PCI bus control signals and control bits from the XPBUS representing PCI control signals in the following ways:

1. HIC 1000 buffers clocked control signals from the host PCI bus, encodes them into control bits and sends the encoded control bits to the XPBUS;
2. HIC 1000 manages the signal locally; and
3. HIC 1000 receives control bits from XPBUS, translates the control bits into PCI control signals and sends the PCI control signals to the host PCI bus.

FIG. 11 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1100 is nearly identical to HIC 1000 in its function, except that HIC 1000 interfaces the host PCI bus to the XPBUS while PIC 1100 interfaces the secondary PCI bus to the XPBUS. Similarly, the components in PIC 1100 serve the same function as their corresponding components in HIC 1000. Reference numbers for components in PIC 1100 have been selected such that a component in PIC 1100 and its corresponding component in HIC 1000 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1100 is referenced as bus controller 1110 while the bus controller in HIC 1000 is referenced as bus controller 1010. As many of the elements in PIC 1100 serve the same functions as those served by their corresponding elements in HIC 1000 and as the functions of the corresponding elements in HIC 1000 have been described in detail above, the function of elements of PIC 1100 having corresponding elements in HIC 1000 will not be further described herein. Reference may be made to the above description of FIG. 10 for an understanding of the functions of the elements of PIC 1100 having corresponding elements in HIC 1000.

As suggested above, there are also differences between HIC 1000 and PIC 1100. Some of the differences between HIC 1000 and PIC 1100 include the following. First, receiver 1140 in PIC 1100, unlike receiver 1040 in HIC 1000, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 1000 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1050. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1000. Another difference between PIC 1100 and HIC 1000 is the fact that PIC 1100 contains a video parallel to serial converter 1189 whereas HIC 1000 contains a video serial to parallel converter 1080. Video parallel to serial converter 1189 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0:15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1100, unlike HIC 1000, contains a clock doubler 1182 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1182 through buffer 1183 and is sent to serial to parallel converter 1080 through buffer 1184. Additionally, reset control unit 1135 in PIC 1100 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 1000 whereas reset control unit 1045 of HIC 1000 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1090 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1100 to the HIC 1000.

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Like HIC 1000, PIC 1100 handles the PCI bus control signals and control bits from the XPBUS representing PCI control signals in the following ways:

1. PIC 1100 buffers clocked control signals from the secondary PCI bus, encodes them and sends the encoded control bits to the XPBUS;
2. PIC 1100 manages the signal locally; and
3. PIC 1100 receives control bits from XPBUS, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

PIC 1100 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

FIG. 12 is a table showing the symbols, signals, data rate and description of signals on the XPBUS, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

FIG. 13 is a table showing the information transmitted on the XPBUS during two clock cycles of the XPBUS in one embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBUS. In FIG. 13, A00 to A31 represent 32 bits of PCI address A[31:0], D00 to D31 represent 32 bits of PCI data D[31:0], BS0 to BS3 represent 4 bits of bus status data indicating the status of the XPBUS, CM0# to CM3# represent 4 bits of PCI command information, BE0# to BE3# represent 4 bits of PCI byte enable information, and CN0 to CN9 represent 10 bits of control information sent in each clock cycle. As shown in FIG. 13, for each of lines PD0 to PD3, the 10 bit data packets contain one BS bit, one CM/BE bit, and eight AID bits. For the PCN line, the 10 bit data packet contains 10 CN bits. The first clock cycle shown in FIG. 13 comprises an address cycle in which 4 BS bits, 4 CM bits, 32 A bits and 10 CN bits are sent. The second clock cycle comprises a data cycle in which 4 BS bits, 4 BE bits, 32 D bits and 10 CN bits are sent. The bits transmitted on lines PD0 to PD3 represent 32 PCI AD[31:0] signals, 4 PCI C/BE# [3:0] signals, and part of the function of PCI control signals, such as FRAME#, IRDY#, and TRDY#.

In the embodiment shown in FIG. 13, BS0 to BS3 are sent at the beginning of each clock cycle. The bus status bits indicate the following bus cycle transactions: idle, address transfer, write data transfer, read data transfer, switch XPBUS direction, last data transfer, wait, and other cycles.

Bits representing signals transmitted between the CPU and South Bridge may also be sent on the lines interconnecting the HIC and PIC, such as lines PCN and PCNR. For example, CPU interface signals such as CPU interrupt (INTR), Address 20 Mask (A20M#), Non-Maskable Interrupt (NMI), System Management Interrupt (SMI#), and Stop Clock (STPCLK#), may be translated into bit information and transmitted on the XPBUS between the HIC and the PIC.

FIG. 14 is a table showing the information transmitted on the XPBUS during four clock cycles of the XPBUS in another embodiment of the present invention where 10 data bits are transmitted in each clock cycle of the XPBUS. In this embodiment, the XPBUS clock rate is twice as large as the PCI clock rate. This allows sending data and address bits every other XPBUS cycle. As can be seen in FIG. 14, there are no address

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or data bits transmitted during the second or fourth XPBus clock cycle. The fact that the XPBus clock rate is higher than the PCI clock rate allows for compatibility of the XPBus with possible future expansions in the performance of PCI bus to higher data transfer and clock rates.

In the embodiment shown in FIG. 14, there are 18 control bits, CN0 to CN17, transmitted in every two XPBus clock cycles. The first bit transmitted on the control line in each XPBus clock cycle indicates whether control bits CN0 to CN8 or control bits CN9 to CN17 will be transmitted in that cycle. A zero sent at the beginning of a cycle on the control line indicates that CN0 to CN8 will be transmitted during that cycle, whereas a one sent at the beginning of a cycle on the control line indicates that CN9 to CN17 will be transmitted during that cycle. These bits also indicate the presence or absence of data and address bits during that cycle. A zero indicates that address or data bits will be transmitted during that cycle whereas a one indicates that no address or data bits will be transmitted during that cycle.

In one embodiment, BS0 and BS1 are used to encode the PCI signals FRAME# and IRDY#, respectively. Additionally, in one embodiment, BS2 and BS3 are used to indicate the clock speed of the computer bus interface and the type of computer bus interface, respectively. For example, BS2 value of zero may indicate that a 33 MHz PCI bus of 32 bits is used whereas a BS2 value of one may indicate that a 66 MHz PCI bus of 32 bits is used. Similarly, a BS3 value of zero may indicate that a PCI bus is used whereas a BS3 value of one may indicate that another computer interface bus, such as an Institute of Electronics & Electrical Engineers (IEEE) 1394 bus, is used.

FIG. 15 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits such as those shown in FIGS. 13 and 14 from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 15, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 15 transmit data. In other words they transmit information from the NC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

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The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 23, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIG. 16 is a table showing the names, types, number of pins dedicated to, and the description of the primary bus PCI signals. The pins represent those between the host PCI bus and the HIC.

FIG. 17 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 1710, system memory 1720, high performance devices 1750, primary mass storage 1730, and related interface and support circuitry 1740. The PCON includes primary display 1810, primary input 1820, secondary mass storage 1750, other devices 1860, expansion slots 1870, the primary power supply 1830, and related interface and support circuitry 1840. The interconnection apparatus 1900 includes circuitry to convey power and operational signals between the ACM and PCON.

Within the ACM 1700, the CPU 1710 executes instructions and manipulates data stored in the system memory. The CPU 1710 and system memory 1720 represent the user's core computing power. The core computing power may also include high performance devices 1750 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 1730 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 1740 primarily includes interface chips and signal busses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

Within the PCON 1800, the primary display component 1810 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display



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screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

The primary input component **1820** of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

The PCON may contain secondary mass storage **1850** to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

The PCON may be enhanced with additional capability through the use of integrated "Other Devices" **1860** or add-on cards inserted into the PCON's expansion slots **1870**. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry **1840** primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

Importantly, the PCON houses the primary power supply **1830**. The primary power supply has sufficient capacity to power both the PCON and the ACM **1700** for normal operation. Note that the ACM may include a secondary "power supply" in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

FIG. **18** is a block diagram of an attached computing module (ACM) **1700**. The physical ACM package **1700** contains the ACM functional components **1701** and the ACM side of the ACM-to-PCON Interconnection **1900**. The ACM **1701** comprises a CPU component **1710**, a system memory component **1720**, a primary mass storage component **1730**, a high performance devices components **1750**, and an interface and support component **1740**.

The ACM side of the ACM-to-PCON Interconnection **1900** comprises a Host Interface Controller (HIC) component **1920** and an ACM connector component **1930**. The HIC **1920** and connector **1930** components couple the ACM functional components **1700** with the signals of an ACM-to-PCON interface bus **1910** used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus **1910** comprises conveyance for electrical power **1914** and signals for a peripheral bus **1912**, video **1916**, video port **1917**, and console type **1918**. The preferred ACM-to-PCON Interconnection **1900** is described in detail in a companion U.S. patent application Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," by the same inventor, filed on the same day

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herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection **1900** includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection **1900**. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

The CPU component **1710** of the ACM functional circuitry **1701** of the presently described embodiment comprises a microprocessor **1712**, which is the chief component of the personal computer system, power supply connection point **1713**, and cache memory **1714** tightly coupled to the microprocessor **1712** by the CPU-to-cache bus **1714** comprising signal paths for address, data, and control information. The microprocessor **1712** of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor **1712** receives electrical power from power bus **1768** via connection point **1713**. Microprocessor **1712** couples to the Host Interface Controller (HIC) **1920** via CPU-to-HIC bus **1763** comprising signal paths to exchange control information such as an interrupt request. Microprocessor **1712** also couples to CPU Bridge **1746** via CPU main bus **1764** comprising signal paths for address, data, and control information.

The CPU Bridge component **1746** of the interface and support circuitry **1740** operates to couple the high speed CPU main bus **1764** to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge **1746** such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

The system memory component **1720** of the ACM functional circuitry **1701** in the present embodiment comprises main system memory (RAM) **1722**, BIOS memory **1724**, and flash memory **1726**. The system memory **1720** is used to contain data and instructions that are directly addressable by the CPU. The RAM **1722** comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion of total system memory **1720** capacity. The BIOS memory **1724** comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating conditions. The BIOS memory **1724** stores, for example, start-up instructions for the microprocessor **1712** and sets of instructions for rudimentary input/output tasks. The flash memory **1726** comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory **1726** are easily changed under normal operating conditions. The flash memory **1726** may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor **1712**. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

The main system memory (RAM) **1722** is coupled to memory controller circuitry resident within the CPU Bridge **1746** via direct memory bus **1765**. The BIOS **1724** and flash



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memory 1726 are coupled to HIC 1920 via switched memory bus 1766. This permits the BIOS 1724 and flash 1726 memories to be accessed by circuitry in the HIC 1920 or other circuitry connected thereto. The direct memory bus 1765 and the switch memory bus 1766 each comprises conductors to convey signals for data, address, and control information.

The primary mass storage component 1730 of the ACM functional circuitry 1701 in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) 1732 has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD 1732 in the present embodiment serves as the “boot” device for the personal computer from which the operating system is loaded into RAM 1722 by the start-up program stored in the BIOS 1724.

The present HDD 1732 has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk 1732 stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user’s identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user’s favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device 1730.

The HDD 1732 is coupled to IDE controller circuitry 1748 via IDE bus 1772. The IDE controller circuitry 1748 is coupled to the CPU Bridge 1746 via the Host PCI bus 1767. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive 1732 to the microprocessor 1712.

The high performance devices component 1750 of the ACM functional circuitry 1701 in the present embodiment comprises an Advanced Graphics Processor (AGP) 1752. The Model 740 Graphics Device from Intel Corporation may be used in the present embodiment as the AGP.

Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP 1752 is located in the ACM 1700, where it is in close proximity to the microprocessor 1712. The AGP 1752 is coupled to the microprocessor 1712 via the advanced graphics port bus 1773 of the CPU Bridge 1746. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus 1770. Video information from a

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source external to the ACM and appearing as video port signals 1917 may be conveyed to the AGP 1752 via video port signal path 1771.

Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today’s CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user’s core computing power and environment in a portable package. This represents a further advantage of the invention.

The interface and support component 1740 of the ACM functional circuitry 1701 in the present embodiment comprises circuitry for power regulation 1742, clocking 1744, CPU Bridge 1746, IDE controller 1748, and signal conveyance paths 1761-1774. The CPU Bridge 1746 couples the CPU component 1710 of the ACM 1700 with the other components of the ACM 1720-1750 and the CPU-to-PCON Interconnection 1900. The CPU Bridge 1746 and IDE controller 1748 have already been discussed. Power regulation circuitry 1742 receives electrical power via the electrical power conduction path 1914 of the CPU-to-PCON Interconnection 1900, conditions and distributes it to the other circuitry in the ACM using power distribution bus 1768. Such regulation and distribution is well known and understood in the art.

Clocking circuitry 1744 generates clock signals for distribution to other components within the ACM 1700 that require a timing and synchronization clock source. The CPU 1710 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1700 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path 1762, in response to a signal received from the host interface controller (HIC) 1920 via signal path 1761. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1920 of the presently described embodiment adjusts the frequency control signal sent via signal path 1761 to the clocking circuitry 1744, based on the “console type” information signal 1918 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1900. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the

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user's core computing power and environment to different work settings, which is a further advantage of the present invention.

FIG. 19 illustrates an external view of one embodiment of an ACM. The case **2010** of the ACM **1700** is generally rectangular in shape, preferably constructed of a strong, lightweight, rigid material that will protect the internal components from mechanical and environmental exposure. Plastics may readily be used to construct the case **2010**. The case **2010** completely surrounds the internal components, being generally an 8-sided box. FIG. 19 shows the top **2012**, right **2014**, and rear **2016** surfaces of the ACM case **2010**. Rear edges **2018** of the case joining the rear surface **2016** with its adjoining surfaces may be beveled or rounded to facilitate insertion of the ACM **1700** into the computer bay of the PCON. Notches **2040** may be formed by projecting small surfaces inward from otherwise generally flat surfaces of the ACM case **2010**. The notches **2040** may be used to engage with mechanical devices mounted in and about a computer bay. Such mechanical devices can be employed to secure the ACM into position within a computer bay for reliability and security. Openings **2017** are formed into the rear surface **2016** of the ACM case **2010** through which to project connectors **1930a** and **1930b**. In one embodiment the case **2010** is approximately 5.75 inches wide by 6.5 inches deep by 1.6 inches high.

Connectors **1930a** and **1930b** are part of the ACM-to-PCON Interconnection as described earlier in reference to FIGS. 3 and 4. When the ACM **1700** is inserted into the computer bay of a peripheral console (PCON), connectors **1930a** and **1930b** mate with corresponding connectors located at the rear of the computer bay to electrically couple the ACM with the PCON containing the computer bay. Details concerning the ACM-to-PCON Interconnection can be found in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference. The connectors **1930a** and **1930b** used in one embodiment are connectors complying with the Device Bay industry standard as documented in "Device Bay Interface Specification," revision 0.85, Feb. 6, 1998. Such connectors have specifically been designed to stand up to the rigors of repeated insertion and withdrawal.

Cooling plate **2030** forms part of the top surface **2012** of ACM **1700**. The cooling plate **2030** may be mounted to, or project through an opening formed in, case **2010**. Similarly, electromagnetic interference (EMI)/electrostatic discharge (ESD) rounding plate **2032** forms part of the right surface **2014** of ACM **1700**. The grounding plate **2032** may be mounted to, or project through an opening formed in, case **2010**. Cooling plate **2030** and grounding plate **2032** compressively mate with counterparts when the ACM is fully inserted into the computer bay. The counterparts located along the boundaries of the computer bay conduct dangerous heat and electrical charges away from the ACM. Inside the ACM, cooling plate **2030** thermally couples to heat-sensitive components such as CPU **1710** by methods well known in the art. Similarly, grounding plate **2032** electrically couples to EMI/ESD-sensitive components, such as a microprocessor, by methods well known in the art.

LCD display **2050** forms part of the right surface **2014** of ACM **1700**. The LCD display may be mounted to, or project through an opening formed in, case **2010**. The LCD display may contain indicators about the status of the ACM. Such indicators may display, for example, the time-of-day from a time-of-day clock contained within the ACM, or the amount of charge remaining in an ACM-resident battery, or certain

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configuration options recorded in flash memory. The LCD display **2050** provides display capability for a limited amount of information, most useful when the ACM is separated from a PCON (and is thus separated from a full-capability, primary display device).

FIG. 19b illustrates one possible embodiment of a computer bay. A computer bay **1890** acts as a receptacle for lodging an ACM (such as the one shown in FIG. 20) within a desktop PCON. The illustrated computer bay **1890** provides an ACM with housing and with signal flow, electrical grounding, heat transfer, and mechanical connections. While many physical arrangements between the ACM and PCON are possible, the use of an enclosed computer bay as the one illustrated in FIG. 20b offers many advantages. For example, the illustrated computer bay **1890** provides physical protection for the ACM. The computer bay may also be easily incorporated into industry standard form factors used in the manufacture of desktop personal computers (e.g., the ACM and associated computer bay could be designed to fit within the volume occupied by a standard-size disk drive).

The computer bay **1890** appearing in FIG. 20b is shown mounted within the confines of PCON case **1802**. The computer bay **1890** comprises frame **1891** and signal flow, grounding, cooling, and locking components as described below. Mounting flanges **1898** of frame **1891** may be used to attach the computer bay **1890** to the PCON structure. The computer bay **1890** is prominently defined by frame **1891** generally forming a cavity in which to lodge an ACM. As such, the interior cavity formed by frame **1891** closely approximates the exterior dimensions of a compatible ACM. The top **1893**, right **1894**, and rear **1895** sides of the computer bay frame **1891** are visible. The computer bay frame **1891** also includes substantial bottom and left sides which are not shown. The front side of the frame **1891** (not shown) is open to allow the insertion of the ACM. Frame **1891** is constructed of metal for strength and to facilitate the conductance of heat and undesired electrical currents away from the ACM.

In the presently described embodiment, the weight of an inserted ACM is largely borne by the bottom side (not shown) of computer bay frame **1891**. Alternative embodiments are possible where, for example, the weight of the ACM is borne by rails running longitudinally down the right and left sides of the computer bay cavity that engage corresponding grooves running longitudinally down the right and left sides of an ACM.

FIG. 20 illustrates the internal component layout for one embodiment of an ACM. All components are contained within the confines of the ACM case **510**, except for connectors **1930a** and **1930b** which extend from the rear of the ACM **1700** to engage mating connectors (not shown) that will couple the ACM circuitry with the PCON circuitry. Main circuit board **2110** provides electrical connections for circuitry within the ACM and mounting for many of its components **1724**, **1722**, **17221**, **1752**, **1742**, **1748**, **1920**, and **1930**. The fabrication and use of such circuit boards is well known and understood in the art. Connector **2122** is also mounted on main circuit board **2110** and mates with mobile processor module **2120**. Mobile processor module **2120** represents a form of packaging for a microprocessor and related components. The illustrated mobile processor module **2120** is a self-contained unit that includes a microprocessor **1712**, CPU cache **1714**, and CPU bridge **1746** operatively interconnected by the manufacturer. An example of one such module is the Pentium Processor with MMX Technology Mobile Module from Intel Corporation (order number 24 3515-001, September 1997). One skilled in the art recognizes that discrete

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microprocessor, cache, and bridge could have been employed and mounted directly to the main circuit board.

The mobile processor module **2120** blocks the view, from the top, of the system BIOS **1724**. Similarly, hard disk drive **1732** hides RAM memory **1722**, the high performance graphics processor **1752**, the host interface controller **1920**, and flash memory **1726**. Memory upgrade socket **2130** remains exposed to facilitate installation of additional RAM memory **1722**. Power regulator **1742**, like the memory upgrade socket, enjoys a generous amount of overhead clearance to accommodate its vertical size. The area including IDE controller **1748** also enjoys overhead clearance to facilitate a cable connection with the hard disk drive **1732**.

The functional interconnection and operation of components contained within the ACM and depicted in FIG. **20** has already been described in relation to FIG. **18** for like numbered items appearing therein.

FIG. **21** is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package **200** contains the PCON functional components **1801** and the PCON side of the ACM-to-PCON Interconnection **1900**. The PCON functional components **1801** comprise primary display **1810**, a primary input **1820**, a primary power supply **1830**, interface and support **1840**, secondary mass storage **1850**, other devices **1860**, and expansion slots **1870**.

The PCON side of the ACM-to-PCON Interconnection **1900** comprises a Peripheral Interface Controller (PIC) component **1940**, a PCON connector component **1950**, console-type component **1942**, and flash memory device **1948**. The PIC **1940** and connector **1950** components couple the PCON functional components **1801** with the signals of an ACM-to-PCON interface bus **1910** used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus **1910** comprises conveyance for electrical power **1914** and signals for a peripheral bus **1912**, video **1916**, video port **1917**, and console-type **1918**. The preferred ACM-to-PCON Interconnection **1900** is described in detail in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference.

Connector component **1950** may be selected to mate directly with the connector component **1930** of an ACM (shown in FIG. **18**). Alternatively, connector component **1950** may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment, such as cable **1964** shown in FIG. **19B**. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

Flash memory device **1948** provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory **1948** may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

The primary display component **1810** of the PCON functional circuitry **1801** of the presently described embodiment comprises integrated display panel **1812** and video connector **1813**. Integrated display panel **1812** is a color LCD display panel having a resolution of 640 horizontal by 480 vertical

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pixels. 640-by-480 resolution is popularly considered to be the minimum screen size to make practical use of the application software in widespread use today. One skilled in the art recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (**1710** of FIG. **17**) of an ACM presently coupled to PCON **1800**.

Integrated display panel **1812** is coupled to video signal bus **1849** and displays a screen image in response to video signals presented on bus **1849**. Certain pins of connector **1950** receive video output signals **1916** of the ACM-to-PCON interface bus **1910** from a mated connector that is coupled to an ACM. These certain pins of connector **1950** couple to video signal bus **1849** which conveys the video output signals **316** throughout the PCON **1800** as needed. Video connector **1813** is exposed at the exterior of PCON **1800** and couples to video signal bus **1849**. Connector **1813** permits easy attachment of an external display device that is compatible with the signals carried by bus **1849**, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel **1812**.

The isolation of the relatively heavy and sizable primary display **1810** from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

The primary input component **1820** of the PCON functional circuitry **1801** of the presently described embodiment comprises keyboard interface circuitry **1822**, keyboard connector **1823**, pointer interface circuitry **1824**, and pointer connector **1825**. Keyboard interface circuitry **1822** and pointer interface circuitry **1824** connect to ISA bus **1845** and are thereby coupled to the CPU component (**1710** of FIG. **17**) of any ACM attached to PCON **1800**. Keyboard interface circuitry **1822** interfaces a standard computer keyboard (not shown), attached at connector **1823**, to ISA bus **1845**. Pointer interface circuitry **1822** interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector **1825**, to ISA bus **1845**. Computer keyboards, pointing devices, connectors **1823**, **1825**, keyboard interface circuitry **1822**, and pointer interface circuitry **1824** are well known in the art. The isolation of the relatively heavy and sizable primary input devices **1820** from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

The primary power supply component **1830** of the PCON functional circuitry **1801** of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON **1800** and any ACM coupled to connector **1950**. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source **1889**, such as a wall outlet. Power supply **1830** reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply **1830** are applied to power bus **1831**. Power bus **1831** distributes the power supply outputs to the other circuitry within the PCON **1800**. Bus **1831** also connects to certain pins of connector **1950** to provide the electrical power **1914** for an ACM conveyed by ACM-to-PCON interconnection **1900**. The isolation of the usually heavy power supply **1830** from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.



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The interface and support component **1840** of the PCON functional circuitry **1801** of the presently described embodiment comprises peripheral bridge **1846**, diskette controller **1842**, IDE controller **1848**, and signal conveyance paths **1841**, **1843**, **1844**, **1845**, **1847** and **1849**. Peripheral bridge **1846** couples PCI peripheral bus **1841** with peripheral busses of other formats such as ISA peripheral bus **1845** and others **1847**. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses **1847** may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console **1800** may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection **1900**, such as PCI bus **1841**, this embodiment includes peripheral bridge **1846** to establish additional busses **1845**, **1847**. The additional busses **1845**, **1847** permit the use of the many low-cost and readily available components compatible with these bus specifications.

Diskette controller **1842** interfaces a floppy disk drive **1854** with the CPU component **1710** of an attached ACM (shown in FIG. **18**) so that the CPU may control and use the diskette drive **1854** hardware to store and retrieve data. Diskette controller **1842** couples to the CPU via a connection to ISA bus **1845**. Diskette controller **1842** connects to the diskette drive **1854** via one of device cables **1843**.

Similarly, IDE controller **1848** interfaces a hard disk drive **1852** and a CDROM drive **1856** with the CPU component **1710** of an attached ACM (shown in FIG. **18**) so that the CPU may control and use the hard disk drive **1852** and CDROM **1856** hardware to store and retrieve data. IDE controller **1848** couples to the CPU via connection to PCI peripheral bus **1841**. IDE controller **1848** connects to each of hard disk drive **1852** and CD-ROM drive **1856** via one of device cables **1843**. Some embodiments of PCON **1800** may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371SB integrated circuit includes circuitry for both the peripheral bridge **1846** and the IDE controller **1848** in a single package.

The secondary mass storage component **1850** of the PCON functional circuitry **1801** of the presently described embodiment comprises diskette drive **1854**, hard disk drive **1852**, and CD-ROM drive **1856**. Secondary mass storage **1850** generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage **1850** are not part of a computer user's core computing power and environment. Secondary mass storage **1850** may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console **1800**, or archival copies of data files that are maintained in primary mass storage **1750** of an ACM (shown in FIG. **18**). Storage capacities for secondary mass storage **1850** devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive **1854**, to more than 10 gigabytes for a large format (5-inch) hard disk drive **1852**. Hard disk drive **1852** employs fixed recording media, while diskette drive **1854** and CD-ROM drive **1856** employ removable media. Diskette drive **1854** and hard disk drive **1852** support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive **1856** supports only read operations.

The other devices component **1860** of the PCON functional circuitry **1801** of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog

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signal for processing by the computer. Video capture cards at present are considered a specialty, i.e., not ubiquitous, component of personal computer systems. Digitized picture information from video capture card **1860** is carried via signal conveyance path **1844** to the peripheral interface controller **1940** which transforms it to the video port signals **1917** of the ACM-to-PCON interconnection **1900** for coupling to the advanced graphics processor **1752** in an attached ACM (shown in FIG. **18**).

Video capture card **1860** is merely representative of the many types of "other" devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card **1860** is shown installed in one of expansion slots **1870** for coupling to the interface and control circuitry **1840** of the PCON. Any of other devices **1860** could be coupled to the interface and control circuitry **1840** of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry **1840**; e.g., a motherboard.

The expansion slots component **1870** of the PCON functional circuitry **1801** of the presently described embodiment comprises PCI connectors **1871** and ISA connectors **1872**. A circuit card may be inserted into one of the connectors **1871**, **1872** in order to be operatively coupled with the CPU **1710** of an attached ACM (shown in FIG. **18**). Each of connectors **1871** electrically connects to PCI bus **1841**, and may receive and hold a printed circuit card which it electrically couples to PCI bus **1841**. Each of connectors **1872** electrically connects to ISA bus **1845**, and may receive and hold a printed circuit card which it electrically couples to ISA bus **1845**. The PCI **1841** and ISA **1845** busses couple to the CPU **1710** of an attached ACM (shown in FIG. **18**) by circuitry already described.

An embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises, an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary input circuitry when said interconnection circuitry is disconnected from a peripheral console.

An alternative embodiment of a detachable computing module in accordance with the present invention, for attachment to a peripheral console for forming a fully operational computer system, comprises an enclosure, a CPU, a memory coupled to said CPU, and a mass storage coupled to said CPU. The module further comprises interconnection circuitry coupled to said CPU, said interconnection circuitry connectable to a peripheral console. The CPU is uncoupled from any primary output circuitry when said interconnection circuitry is disconnected from a peripheral console.

Various modifications to the preferred embodiment can be made without departing from the spirit and scope of the invention. (A limited number of modifications have already been described in the preceding discussion.) For example, a particular embodiment may insert another layer of bus bridging between the CPU bridge and the Peripheral bridge. This may be desirable if, for example, a vendor wants to implement a proprietary, general-purpose bus having intermediate performance characteristics that fall between those of the high-performance general purpose bus originating at the CPU, and the slower general purpose PCI bus. Thus, the foregoing description is not intended to limit the invention as set forth.

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In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

FIG. 22 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 22, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 2200, and a second portion, which includes a hard drive module 2220. A common printed circuit board 2237 houses these modules and the like. Among other features, the ACM includes the central processing unit module 2200 with a cache memory 2205, which is coupled to a north bridge unit 2221, and a host interface controller 2201. The host interface controller includes a lock control 2203. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 2217. Here, the CPU module is spatially located near connector 2217.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 2201 is coupled to BIOS/flash memory 2205. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 2203 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 2220. Among other elements, the hard drive module includes north bridge 2221, graphics accelerator 2223, graphics memory 2225, a power controller 2227, an IDE controller 2229, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal

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computer interface ("PCI") bus 2231, 2232. A power regulator 435 is disposed near the PCI bus.

In a specific embodiment, north bridge unit 2221 often couples to a computer memory, to the graphics accelerator 2223, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 2223 typically couples to a graphics memory 2223, and other elements. IDE controller 2229 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit 2220 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 2220 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 2240 may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

FIG. 23 is a simplified block diagram 2300 of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 2300 has a variety of features such as those noted above, as well as others. In the present reference numerals are used to show the operation of the present system.

The block diagram is an attached computer module 2300. The module 2300 has a central processing unit, which communicates to a north bridge 2341, by way of a CPU bus 2327. The north bridge couples to main memory 2323 via memory

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bus **2329**. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem **2315** via bus **2342**. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2½ inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **2302** and **2331**. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus **2337** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **2305** with a BIOS. The flash memory device **2305** also has codes for a user password that can be stored in the device. The flash memory device generally provides the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller **2307** communicates to the north bridge via bus **2335** and host PCI bus. The host interface controller also has a Lock control **2309**, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller **2307** communicates to the console using bus **2311**, which couples to connection **2313**.

In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device **505**. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

In a specific embodiment, the present invention also includes a real-time clock **510** in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz **508** that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source **506** such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety

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of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.



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The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

1. A computer system comprising:  
a console comprising  
a plurality of coupling sites,  
a serial communication hub controller, and  
an enclosure housing the coupling sites and the serial communication hub controller; and  
a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising  
a processing unit,  
a main memory coupled to the processing unit,  
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,  
a serial controller coupled to the serial communication hub controller, and  
a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.
2. The computer system of claim 1, wherein the computer modules are similar in design to each other.
3. The computer system of claim 1, wherein the console further comprises a second interface controller to communicate with the at least one of the computer modules through the LVDS channel.
4. The computer system of claim 1, wherein the console further comprises a hard disk drive coupled to the at least one of the computer modules.
5. The computer system of claim 1, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.
6. A computer system comprising:  
a console comprising  
a plurality of coupling sites, and  
an enclosure housing the coupling sites; and  
a plurality of computer modules coupled to respective ones of the coupling sites, each of the computer modules comprising  
a processing unit,  
a main memory coupled to the processing unit,  
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,  
an Ethernet controller to communicate with an external network, and  
a first interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

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7. The computer system of claim 6, wherein the computer modules are similar in design to each other.

8. The computer system of claim 6, wherein the console further comprises a second interface controller to communicate with the first interface controller of at least one of the computer modules through the LVDS channel of the at least one of the computer modules.

9. The computer system of claim 6, wherein the console further comprises an Ethernet hub controller coupled to the Ethernet controller of at least one of the computer modules to communicate with the external network.

10. The computer system of claim 6, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

11. A computer system comprising:  
a console comprising  
a plurality of coupling sites, each of the coupling sites comprising a slot,  
a power supply, and  
an enclosure housing the coupling sites and the power supply; and  
a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising  
a processing unit,  
a main memory coupled to the processing unit,  
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions, and  
an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,  
wherein the computer modules receive power from the power supply upon coupling to the console.

12. The computer system of claim 11, wherein the computer modules are similar in design to each other.

13. The computer system of claim 11, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

14. The computer system of claim 11, wherein the console further comprises a mass storage device that is shared between the computer modules.

15. The computer system of claim 11, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

16. A computer system comprising:  
a console comprising  
a plurality of coupling sites,  
a power supply,  
a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,  
an interface controller coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and  
an enclosure housing the coupling sites, the power supply, the LVDS channel, and the interface controller; and  
a computer module coupled to one of the coupling sites and comprising  
a processing unit,  
a main memory coupled to the processing unit, and  
a mass storage device coupled to the processing unit,  
wherein the computer module receives power from the power supply for operation.



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17. The computer system of claim 16, wherein the mass storage device comprises a flash memory.

18. The computer system of claim 16, wherein the computer module further comprises a serial controller coupled to the console for data communication.

19. The computer system of claim 16, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

20. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a pair of unidirectional, multiple serial bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data in opposite directions, and an enclosure housing the coupling sites and the LVDS channels; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a serial communication controller, wherein the serial communication controller is coupled to the console for data communication upon coupling of the computer module to the console.

21. The computer system of claim 20, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

22. The computer system of claim 20, wherein the computer module further comprises a computing environment for a personal computer user.

23. A computer system comprising:

a console comprising

a plurality of coupling sites, at least one of the coupling sites comprising a connector,

a Digital Versatile Disk (DVD) drive,

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the DVD drive, and the first differential signal channel; and

a computer module coupled to the at least one of the coupling sites through the connector, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory,

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an interface controller coupled to the console through the second differential signal channel and the connector,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console.

24. The computer system of claim 23, wherein the computer module further comprises a computing environment for a personal computer user.

25. The computer system of claim 23, wherein the console further comprises a power supply, and the computer module receives power from the power supply upon insertion of the computer module into the console.

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26. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector,

a power supply,

an integrated Liquid Crystal Display (LCD),

a first differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions, and

an enclosure housing the coupling sites, the power supply, the LCD, and the first differential signal channel; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device comprising a flash memory, and

a second differential signal channel comprising a pair of unidirectional, serial bit channels to transmit data in opposite directions,

wherein the first differential signal channel and the second differential signal channel are coupled to each other upon insertion of the computer module into the console, and the computer module is at least partially powered by the power supply for operation.

27. The computer system of claim 26, wherein the computer module further comprises a computing environment for a personal computer user.

28. The computer system of claim 26, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

29. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a connector, and

a first pair of unidirectional, multiple bit, low voltage differential signal (LVDS) channels to transmit encoded Peripheral Component Interconnect (PCI) bus transaction as serial data along a pair of directions that are different from each other; and

a computer module coupled to one of the coupling sites through the connector of the one of the coupling sites, the computer module comprising

a processing unit,

a main memory coupled to the processing unit,

a mass storage device coupled to the processing unit,

a second pair of unidirectional, multiple bit, LVDS channels to transmit encoded PCI bus transaction as serial data along a pair of directions that are different from each other, and

an interface controller coupled to the second pair of LVDS channels,

wherein the interface controller is coupled to the console for data communication upon coupling of the computer module to the console.

30. The computer system of claim 29, wherein the console further comprises a Digital Versatile Disk (DVD) drive.

31. The computer system of claim 29, wherein the computer module further comprises a password mechanism to control access to the computer module.

32. The computer system of claim 20, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

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33. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, each of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the mass storage device is coupled to the computer modules during operation.

34. The computer system of claim 33, wherein the serial communication controller of at least one of the computer modules is coupled to the console for data communication.

35. The computer system of claim 33, wherein the console further comprises a power supply to supply power to the computer modules.

36. The computer system of claim 33, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

37. A computer system comprising:

a console comprising

a plurality of coupling sites, each of the coupling sites comprising a slot,

a mass storage device, and

an enclosure housing the coupling sites and the mass storage device; and

a plurality of computer modules, each of the computer modules coupled to a respective one of the coupling sites through the slot of the respective one of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit,

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a serial communication controller, and

an interface controller coupled to the LVDS channel to transmit encoded Peripheral Component Interconnect (PCI) bus transaction data,

wherein the computer modules are similar in design to each other, and wherein the at least one of the computer modules is configured to provide protection against failure of another one of the computer modules.

38. The computer system of claim 37, wherein the serial communication controller of the at least one of the computer modules is coupled to the console for data communication.

39. The computer system of claim 37, wherein the mass storage device is coupled to the computer modules upon insertion of the computer modules into the console.

40. The computer system of claim 37, wherein the encoded PCI bus transaction data comprises encoded PCI address and data bits.

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41. A computer system comprising:

a plurality of coupling sites;

a power supply;

a low voltage differential signal (LVDS) channel associated with at least one of the coupling sites, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a first interface controller associated with the at least one of the coupling sites and coupled to the LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a plurality of computer modules coupled to respective ones of the coupling sites, at least one of the computer modules comprising

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller coupled to the first interface controller through the LVDS channel,

wherein the computer modules receive power from the power supply for operation.

42. The computer system of claim 41, wherein at least one of the computer modules further comprises an Ethernet controller to communicate with an external network.

43. The computer system of claim 41, wherein the computer system further comprises a mass storage device that is shared between the computer modules.

44. The computer system of claim 41, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

45. A computer system comprising:

a console comprising

a first coupling site,

a second coupling site,

a power supply,

a first low voltage differential signal (LVDS) channel associated with the first coupling site, the first LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a second LVDS channel associated with the second coupling site, the second LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions,

a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, and

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the first interface controller.

46. The computer system of claim 45, further comprising: a first computer module coupled to the first coupling site; and

a second computer module coupled to the second coupling site, wherein at least one of the first computer module and the second computer module comprises

a processing unit,

a main memory coupled to the processing unit, and

a second interface controller to communicate with the console through one of the first LVDS channel and the second LVDS channel.

47. The computer system of claim 46, wherein each of the first computer module and the second computer module receives power from the power supply for operation.

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48. The computer system of claim 45, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

49. A computer system comprising:

- a console comprising:
  - a coupling site,
  - a power supply,
  - a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,
  - a second differential channel associated with the coupling site, the second differential channel comprising two sets of unidirectional, serial bit channels in opposite directions,
  - a first interface controller coupled to the second differential channel, and
  - an enclosure housing the coupling site, the power supply, the first LVDS channel, the second differential channel, and the first interface controller.

50. The computer system of claim 49, further comprising: a computer module coupled to the coupling site, wherein the computer module comprises

- a processing unit,
- a main memory coupled to the processing unit, and
- a second interface controller to communicate, via Universal Serial Bus (USB) communication, with the console through the second differential channel.

51. The computer system of claim 50, wherein the computer module receives at least partial power from the power supply of the console for operation upon coupling to the console.

52. The computer system of claim 50, wherein the computer module further comprises a computing environment for a personal computer user.

53. The computer system of claim 49, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

54. A computer module insertable into a coupling site of a console for data communication, comprising:

- a main circuit board;
- a processing unit coupled to the main circuit board;
- a main memory coupled to the processing unit;
- a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and
- a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.

55. The computer module of claim 54, further comprising a removable hard disk drive.

56. The computer module of claim 54, further comprising a serial communication controller to couple to the console for data communication.

57. The computer module of claim 54, wherein the computer module is configured to operate upon receiving power from the console.

58. The computer module of claim 54, further comprising an enclosure housing the main circuit board, the processing unit, the main memory, the LVDS channel, and the interface controller, and the enclosure is insertable into the coupling site of the console.

59. The computer module of claim 54, further comprising a connector distinct from the main circuit board, and the

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connector is configured to couple to the coupling site of the console for data communication.

60. The computer module of claim 54, wherein the peripheral bridge corresponds to a north bridge.

61. The computer module of claim 54, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

62. The computer module of claim 56, wherein the data communication of the serial communication controller comprises Ethernet communication.

63. The computer module of claim 56, wherein the data communication of the serial communication controller comprises Universal Serial Bus (USB) communication.

64. The computer module of claim 59, wherein the interface controller is configured to communicate the encoded serial bit stream of PCI bus transaction through the LVDS channel and the connector.

65. A computer module comprising:

- an enclosure insertable into a slot of a console for guidance to a first connector of the console for operation;
- a processing unit housed in the enclosure;
- a main memory coupled to the processing unit and housed in the enclosure;
- an Ethernet controller coupled to the processing unit and housed in the enclosure;
- a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions;
- a second connector configured to couple to the first connector of the console; and
- an interface controller housed in the enclosure and coupled to the second connector through the LVDS channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

66. The computer module of claim 65, wherein the Ethernet controller is configured to couple to the first connector of the console for data communication.

67. The computer module of claim 66, wherein the Ethernet controller is coupled to the second connector.

68. The computer module of claim 66, wherein the Ethernet controller is configured to communicate with an external network through the console.

69. The computer module of claim 65, wherein the computer module is configured to operate only upon receiving power from the console.

70. The computer module of claim 65, wherein the enclosure defines a set of grooves to engage a corresponding set of rails of the slot of the console.

71. The computer module of claim 65, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

72. A computer module comprising:

- a main circuit board;
- a first connector distinct from the main circuit board;
- a processing unit coupled to the main circuit board;
- a main memory coupled to the processing unit;
- a hard disk drive coupled to the processing unit;
- a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions; and
- an interface controller coupled to the LVDS channel and the first connector for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction,

wherein the computer module is configured to engage rails on opposite sides of a slot of a console for guidance towards a second connector of the console.

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73. The computer module of claim 72, wherein the LVDS channel is configured to couple to the console.

74. The computer module of claim 72, wherein the first connector of the computer module is configured to mate with the second connector of the console upon the computer module being inserted into the console for operation.

75. The computer module of claim 74, wherein the LVDS channel is configured to couple to the console through the first connector of the computer module and the second connector of the console.

76. The computer module of claim 72, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

77. A computer module comprising:

a processing unit;

a main memory coupled to the processing unit;

a mass storage device coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and a serial communication controller configured to couple to a console,

wherein the computer module is insertable into a slot of the console for guidance to a connector of the console for serial data communication.

78. The computer module of claim 77, wherein the mass storage device comprises a SCSI hard disk drive.

79. The computer module of claim 77, wherein the computer module is configured to operate only upon receiving power from the console.

80. The computer module of claim 77, wherein the serial communication controller comprises an Ethernet controller to communicate with an external network through the console.

81. A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;

a second coupling site to couple to a second computer module;

a power supply coupled to at least one of the first coupling site and the second coupling site;

a printed circuit board;

a first low voltage differential signal (LVDS) channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a second LVDS channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions; and an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the printed circuit board.

82. The computer module of claim 77, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

83. The console of claim 81, further comprising a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.

84. The console of claim 83, wherein at least one of the first computer module and the second computer module comprises a second interface controller, and the first interface controller is configured to couple to the second interface controller.

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85. The console of claim 81, wherein the power supply is configured to provide power to each of the first computer module and the second computer module for operation.

86. The console of claim 81, further comprising a hard disk drive configured to couple to at least one of the first computer module and the second computer module.

87. The console of claim 81, further comprising an Ethernet hub controller configured to couple to at least one of the first computer module and the second computer module for communication with an external network.

88. The console of claim 83, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

89. A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;

a second coupling site to couple to a second computer module;

a power supply;

a printed circuit board coupled to the first coupling site and the second coupling site;

a serial communication hub controller coupled to the printed circuit board;

a low voltage differential signal (LVDS) channel associated with at least one of the first coupling site and the second coupling site, the LVDS channel comprising two sets of unidirectional, multiple serial bit channels in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

an enclosure housing the first coupling site, the second coupling site, the power supply, the printed circuit board, the serial communication hub controller, and the LVDS channel.

90. The console of claim 89, wherein each of the first coupling site and the second coupling site comprises a slot and a connector.

91. The console of claim 89, further comprising an interface controller housed in the enclosure and coupled to the LVDS channel to communicate the encoded serial bit stream of PCI bus transaction.

92. The console of claim 89, further comprising an integrated display device.

93. The console of claim 89, wherein the serial communication hub controller comprises a multi-port, serial communication hub controller to support communication between the first computer module and the second computer module and with an external network.

94. The console of claim 89, further comprising a storage subsystem housed in the enclosure and shared by the first computer module and the second computer module.

95. The console of claim 89, wherein the power supply is configured to provide power to each of the first computer module and the second computer module for operation.

96. The console of claim 89, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

97. A server comprising:

a processing unit;

a main memory coupled to the processing unit;

a mass storage device coupled to the processing unit;

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

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a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel; wherein the processing unit is configured to couple to an external network through the LVDS channel.

98. The server of claim 97, further comprising an Ethernet controller coupled to the LVDS channel.

99. The server of claim 97, wherein the peripheral bridge corresponds to a north bridge.

100. The server of claim 97, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

101. A server comprising:  
a processing unit;  
a main memory coupled to the processing unit;  
a SCSI hard disk drive coupled to the processing unit;

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a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and an interface controller coupled to the LVDS channel; wherein the processing unit is coupled to the interface controller for data communication with an external Ethernet network.

102. The server of claim 101, further comprising an Ethernet controller coupled to the LVDS channel.

103. The server of claim 101, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

\* \* \* \* \*





US008041873C1

(12) **INTER PARTES REEXAMINATION CERTIFICATE** (601st)**United States Patent****Chu**(10) **Number:** **US 8,041,873 C1**(45) **Certificate Issued:** **\*May 14, 2013**

(54) **MULTIPLE MODULE COMPUTER SYSTEM AND METHOD INCLUDING DIFFERENTIAL SIGNAL CHANNEL COMPRISING UNIDIRECTIONAL SERIAL BIT CHANNELS TO TRANSMIT ENCODED PERIPHERAL COMPONENT INTERCONNECT BUS TRANSACTION DATA**

(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)

(73) Assignee: **ACQIS LLC**, McKinney, TX (US)

**Reexamination Request:**

No. 95/001,787, Oct. 18, 2011

**Reexamination Certificate for:**

Patent No.: **8,041,873**  
 Issued: **Oct. 18, 2011**  
 Appl. No.: **12/504,534**  
 Filed: **Jul. 16, 2009**

(\*) Notice: This patent is subject to a terminal disclaimer.

**Related U.S. Application Data**

(63) Continuation of application No. 12/077,503, filed on Mar. 18, 2008, now Pat. No. 7,676,624, which is a continuation of application No. 11/166,656, filed on Jun. 24, 2005, now Pat. No. 7,376,779, which is a continuation of application No. 11/097,694, filed on Mar. 31, 2005, now Pat. No. 7,363,415, which is a continuation of application No. 10/772,214, filed on Feb. 3, 2004, now Pat. No. 7,099,981, which is a continuation of application No. 09/569,758, filed on May 12, 2000, now Pat. No. 6,718,415.

(60) Provisional application No. 60/134,122, filed on May 14, 1999.

(51) **Int. Cl.**  
**G06F 13/20** (2006.01)

(52) **U.S. Cl.**  
 USPC ..... **710/313**; 709/227; 710/301; 710/315

(58) **Field of Classification Search**  
 None  
 See application file for complete search history.

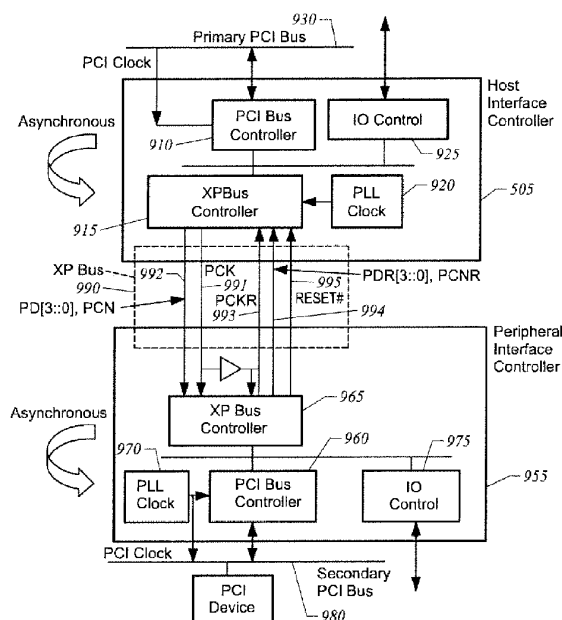
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To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 95/001,787, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

*Primary Examiner* — Majid A. Banankhah

(57) **ABSTRACT**

A computer system for multi-processing purposes. The computer system has a console comprising a first coupling site and a second coupling site. Each coupling site comprises a connector. The console is an enclosure that is capable of housing each coupling site. The system also has a plurality of computer modules, where each of the computer modules is coupled to a connector. Each of the computer modules has a processing unit, a main memory coupled to the processing unit, a graphics controller coupled to the processing unit, and a mass storage device coupled to the processing unit. Each of the computer modules is substantially similar in design to each other to provide independent processing of each of the computer modules in the computer system.





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**INTER PARTES  
REEXAMINATION CERTIFICATE  
ISSUED UNDER 35 U.S.C. 316**

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

**Matter enclosed in heavy brackets [ ] appeared in the patent, but has been deleted and is no longer a part of the patent; matter printed in italics indicates additions made to the patent.**

AS A RESULT OF REEXAMINATION, IT HAS BEEN  
DETERMINED THAT:

The patentability of claims **1-22, 29-80, 82** and **89-103** is confirmed.

Claims **23-28** and **83** are cancelled.

Claims **81, 84** and **88** are determined to be patentable as amended.

Claims **85, 86** and **87**, dependent on an amended claim, are determined to be patentable.

**81.** A console to couple to a plurality of computer modules to form a server system, comprising:

a first coupling site to couple to a first computer module;  
a second coupling site to couple to a second computer module;

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a power supply coupled to at least one of the first coupling site and the second coupling site;

a printed circuit board;

a first low voltage differential signal (LVDS) channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions;

a second LVDS channel coupled to the printed circuit board and comprising two sets of unidirectional, multiple serial bit channels in opposite directions; **[and]**

an enclosure housing the first coupling site, the second coupling site, the power supply, the first LVDS channel, the second LVDS channel, and the printed circuit board; *and*

*a first interface controller coupled to at least one of the first LVDS channel and the second LVDS channel to communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction.*

**84.** The console of claim **[83]** *81*, wherein at least one of the first computer module and the second computer module comprises a second interface controller, and the first interface controller is configured to couple to the second interface controller.

**88.** The console of claim **[83]** *81*, wherein the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

\* \* \* \* \*



US00RE41294E

(19) **United States**  
 (12) **Reissued Patent**  
 Chu

(10) **Patent Number:** **US RE41,294 E**  
 (45) **Date of Reissued Patent:** **\*Apr. 27, 2010**

(54) **PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE**

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(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)

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(73) Assignee: **ACQIS Technology, Inc.**, Mountain View, CA (US)

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(21) Appl. No.: **11/474,256**

(22) Filed: **Jun. 23, 2006**

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Reissue of:

(64) Patent No.: **6,321,335**  
 Issued: **Nov. 20, 2001**  
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 Filed: **Oct. 30, 1998**

(51) **Int. Cl.**  
**H04L 9/32** (2006.01)

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(52) **U.S. Cl.** ..... **713/193; 710/301; 726/9; 726/18; 726/28**

(58) **Field of Classification Search** ..... 713/164, 713/172, 189, 190, 194, 193; 711/164; 710/100, 710/301; 726/2, 9, 17, 18, 19, 20, 28; 361/687  
 See application file for complete search history.

*Primary Examiner*—Beemnet W Dada

(74) *Attorney, Agent, or Firm*—Cooley Godward Kronish LLP

(57) **ABSTRACT**

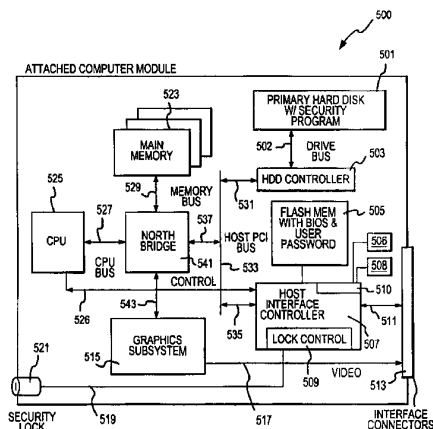
A method and device for securing a removable Attached Computer Module (“ACM”) 10. ACM 10 inserts into a Computer Module Bay (“CMB”) 40 within a peripheral console to form a functional computer such as a desktop computer or portable computer. The present ACM 10 includes a locking system, which includes hardware and software 600, 700, to prevent accidental removal or theft of the ACM from the peripheral console. While ACM is in transit, further security is necessary against illegal or unauthorized use. If ACM contains confidential data, a high security method is needed to safeguard against theft.

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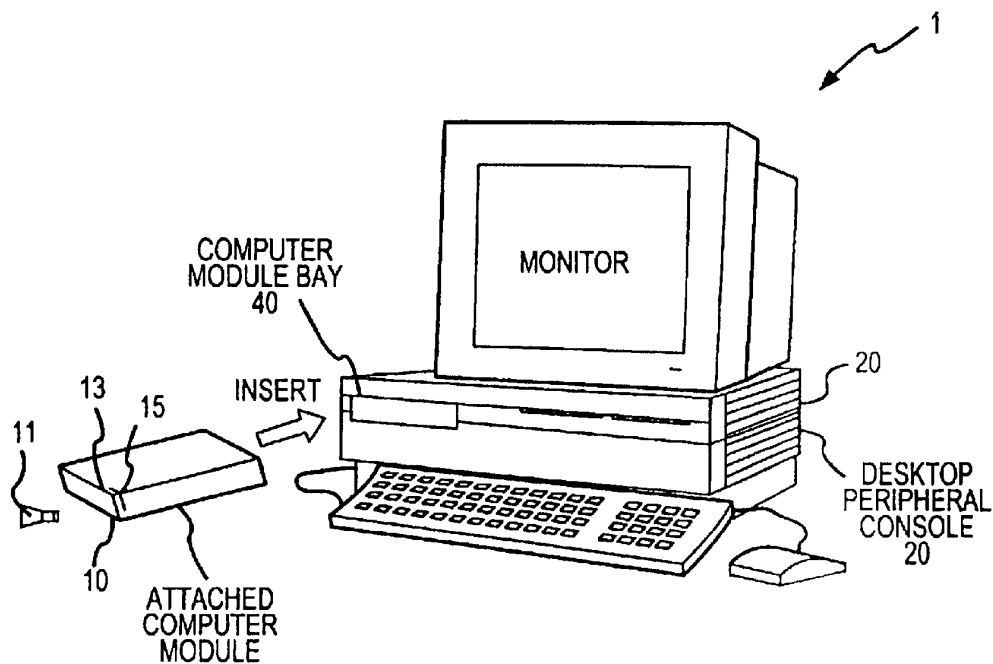


FIG.1



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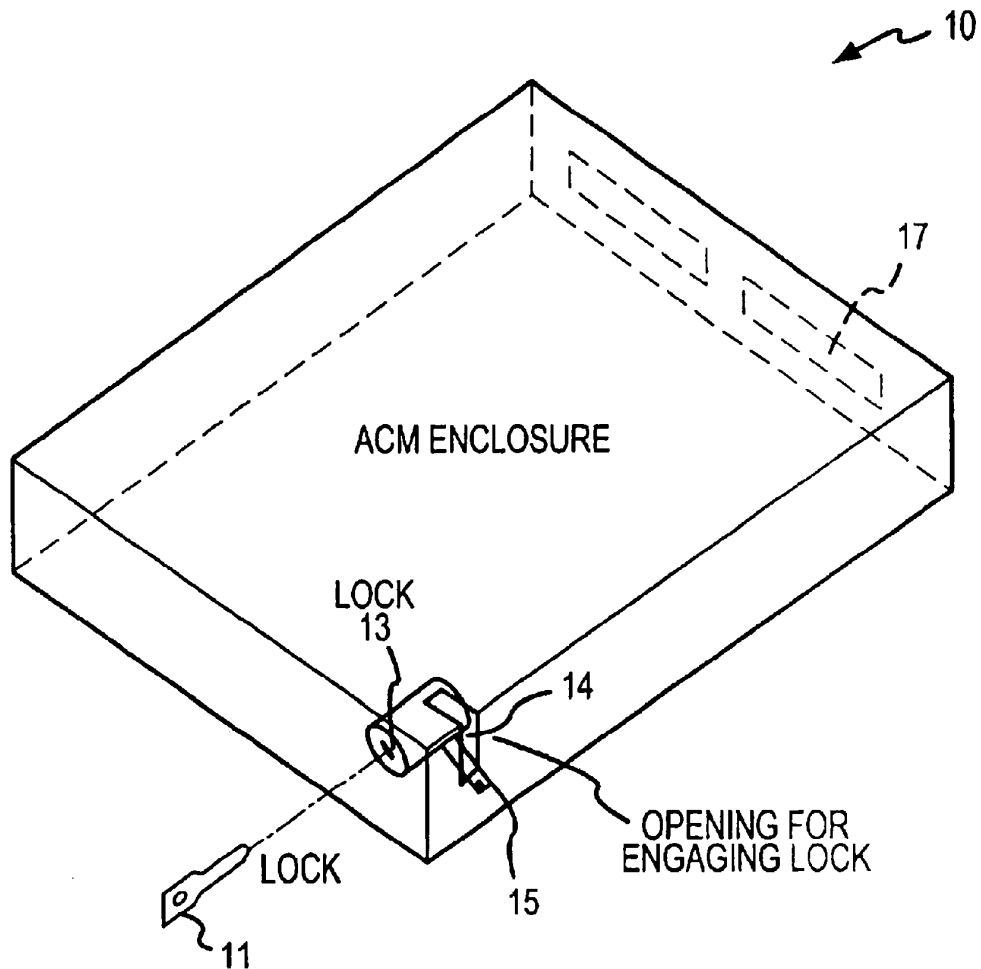


FIG.2

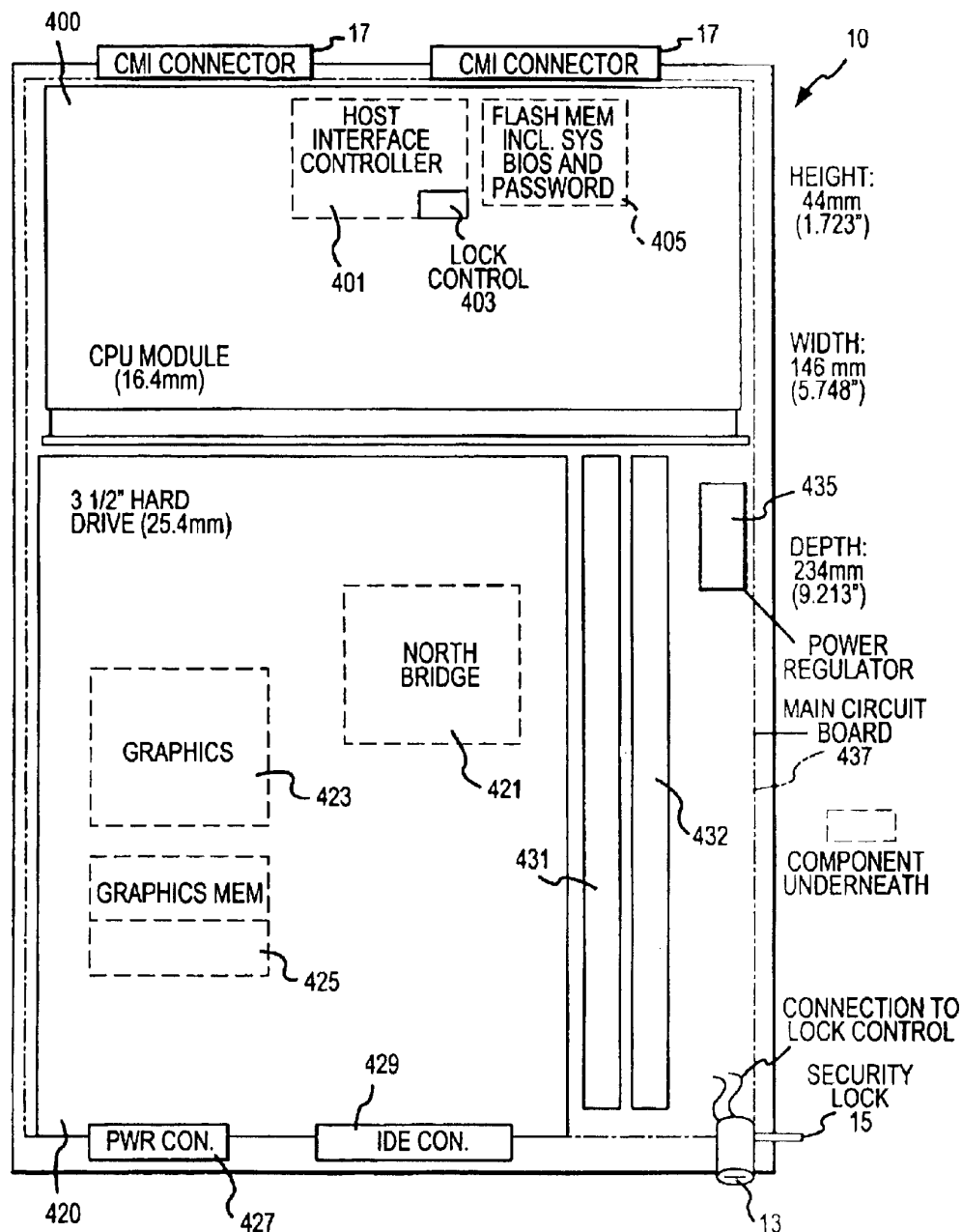


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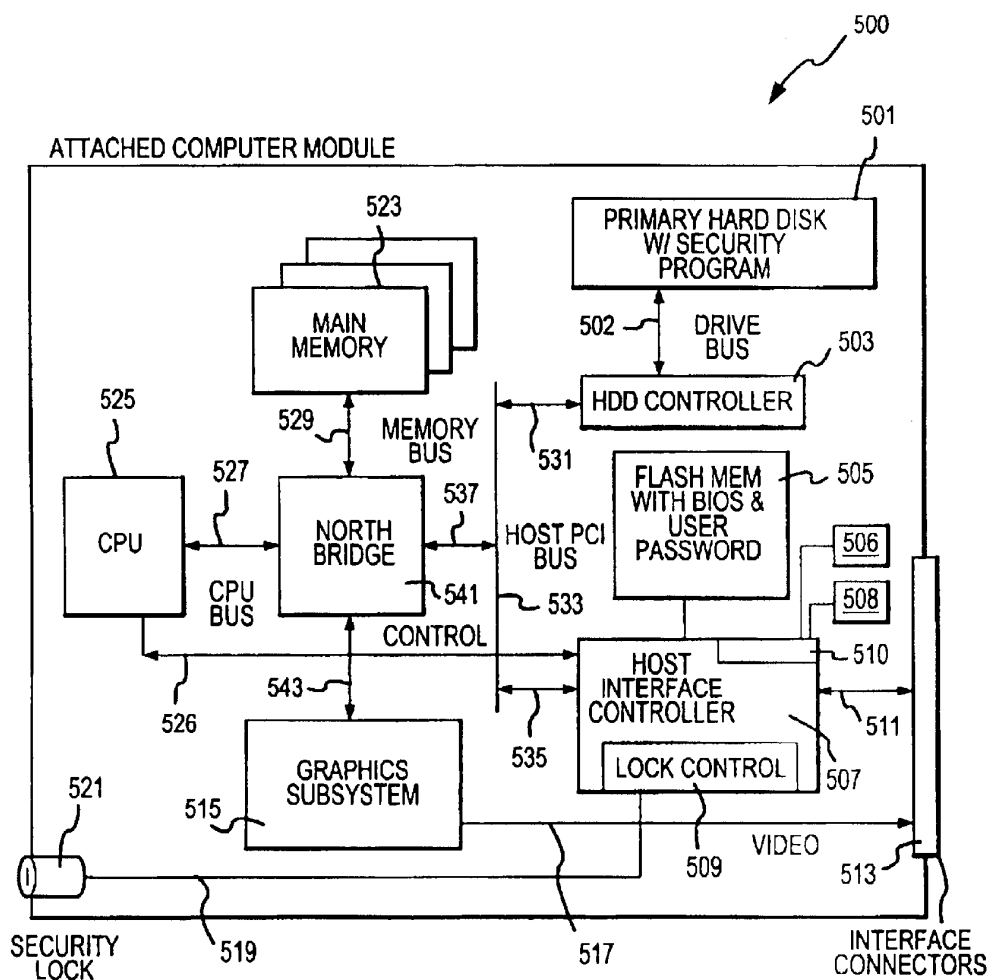


FIG.5

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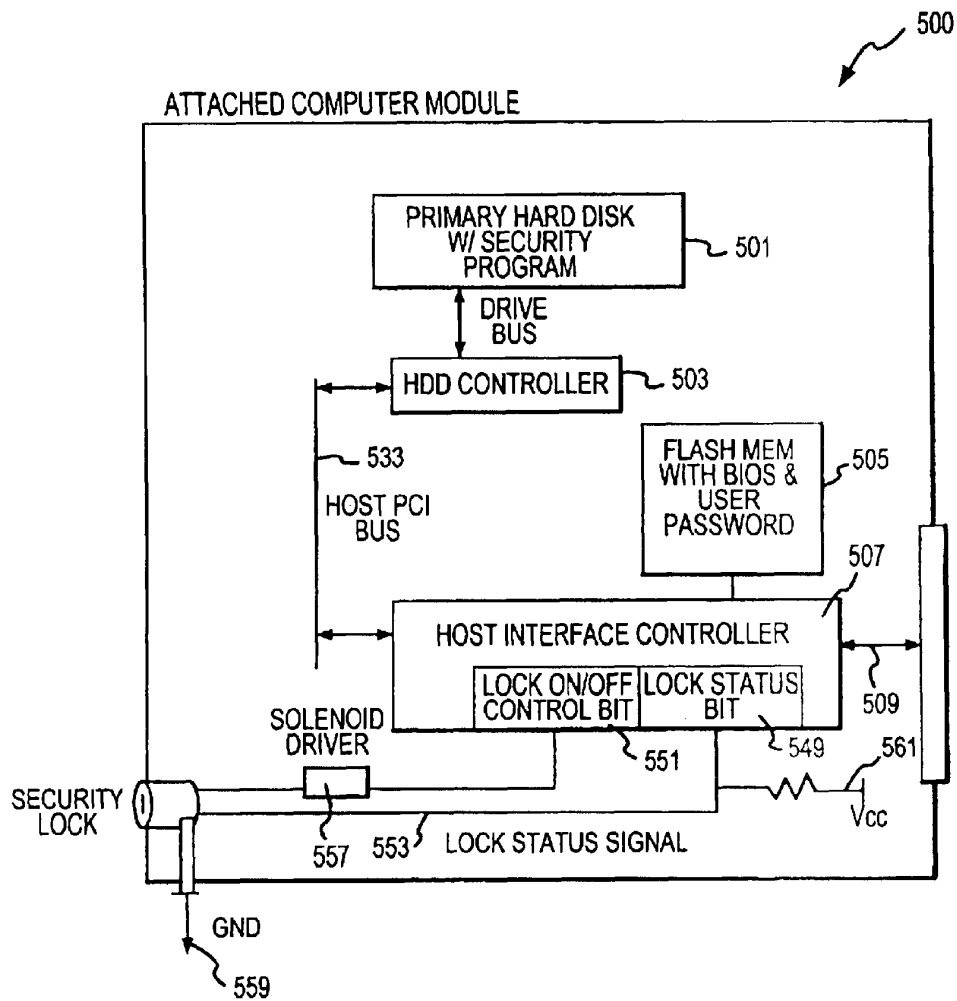


FIG.5A

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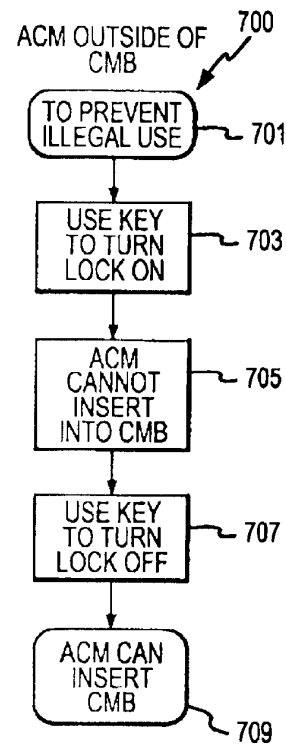
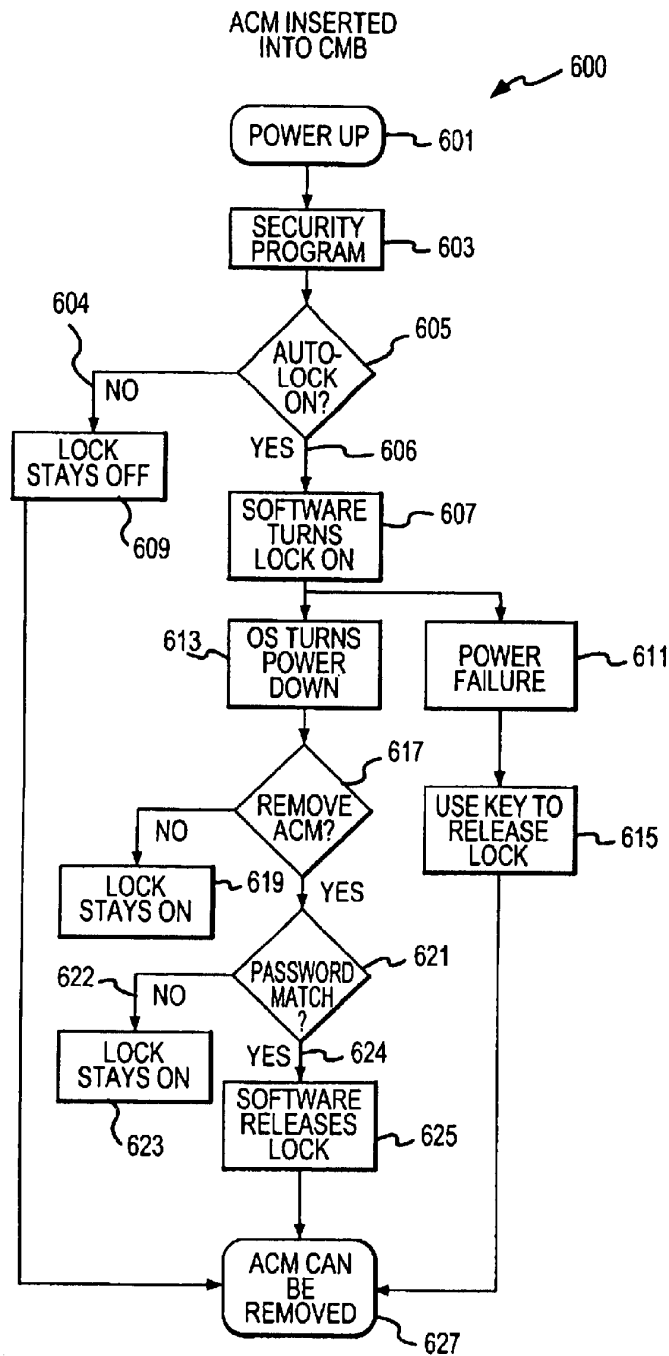


FIG.7



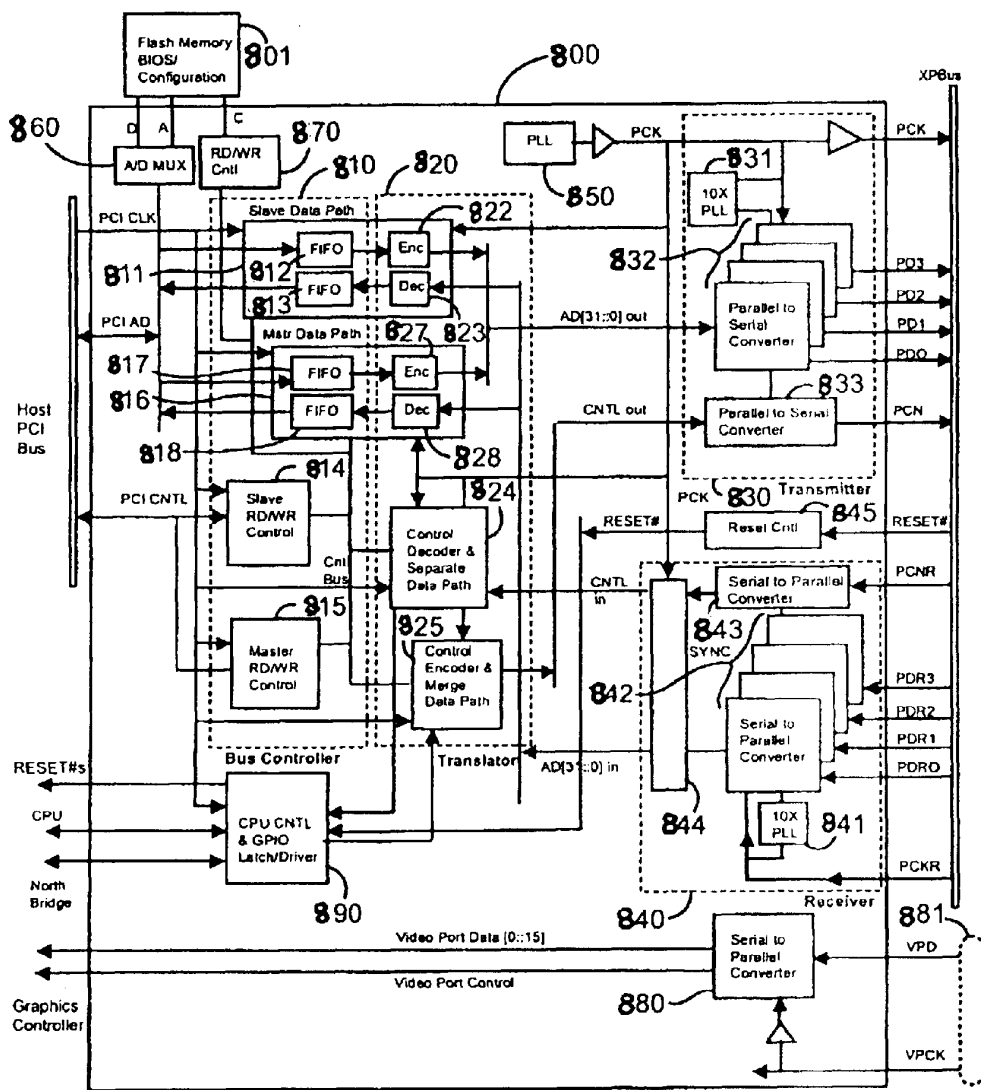


FIG. 8

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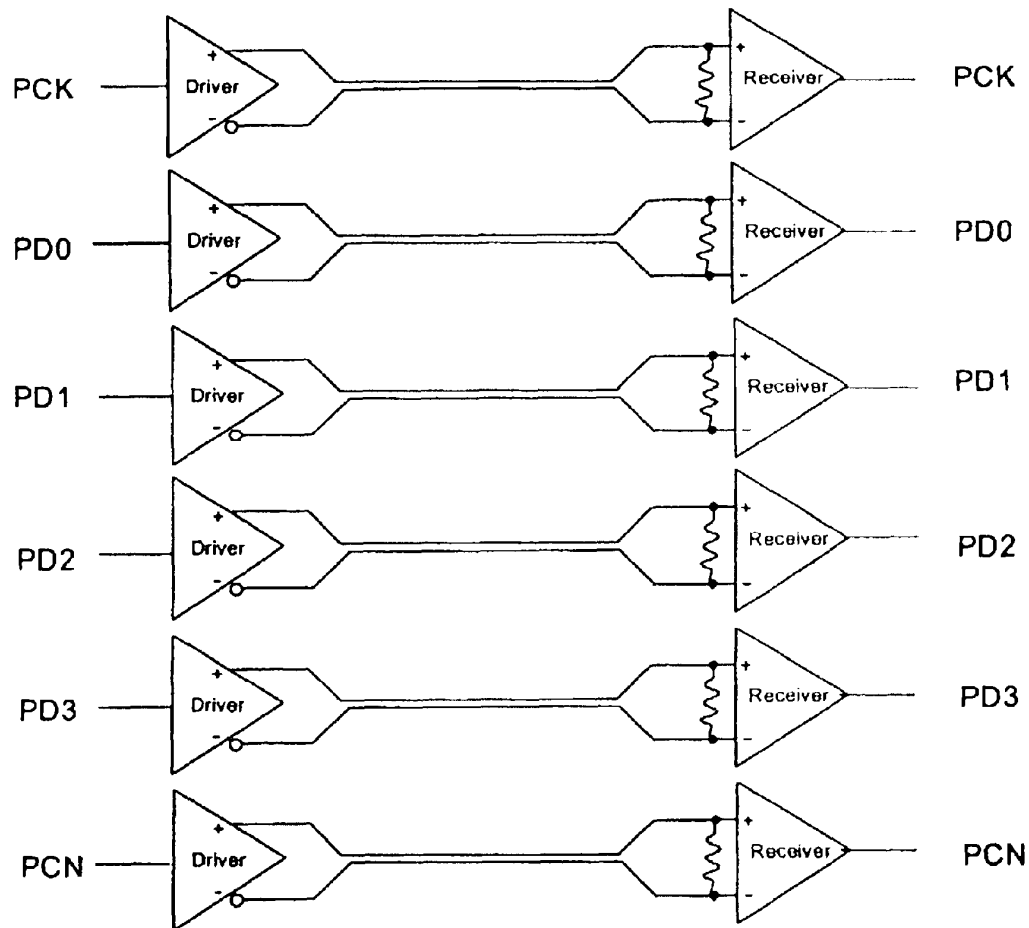


FIG. 9

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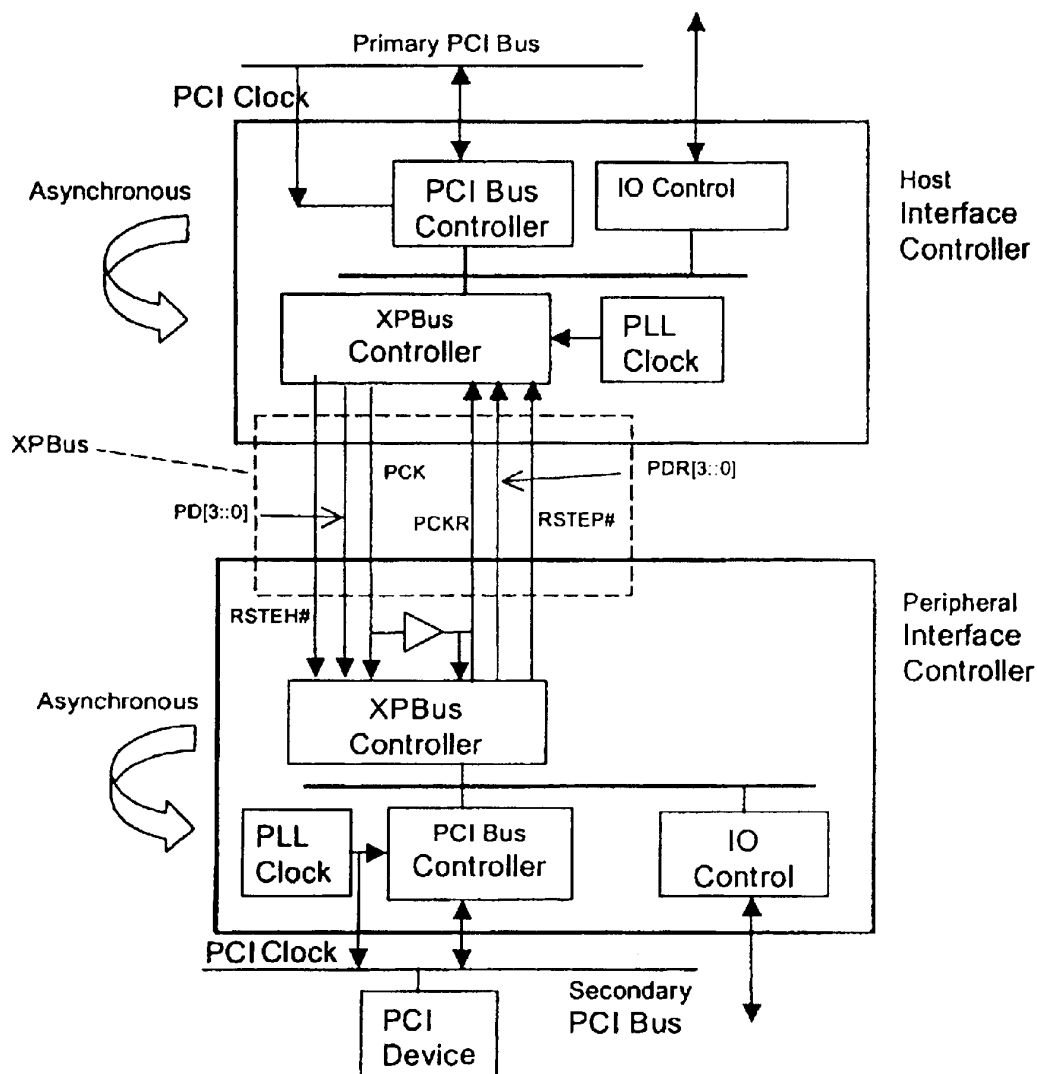


FIG. 10

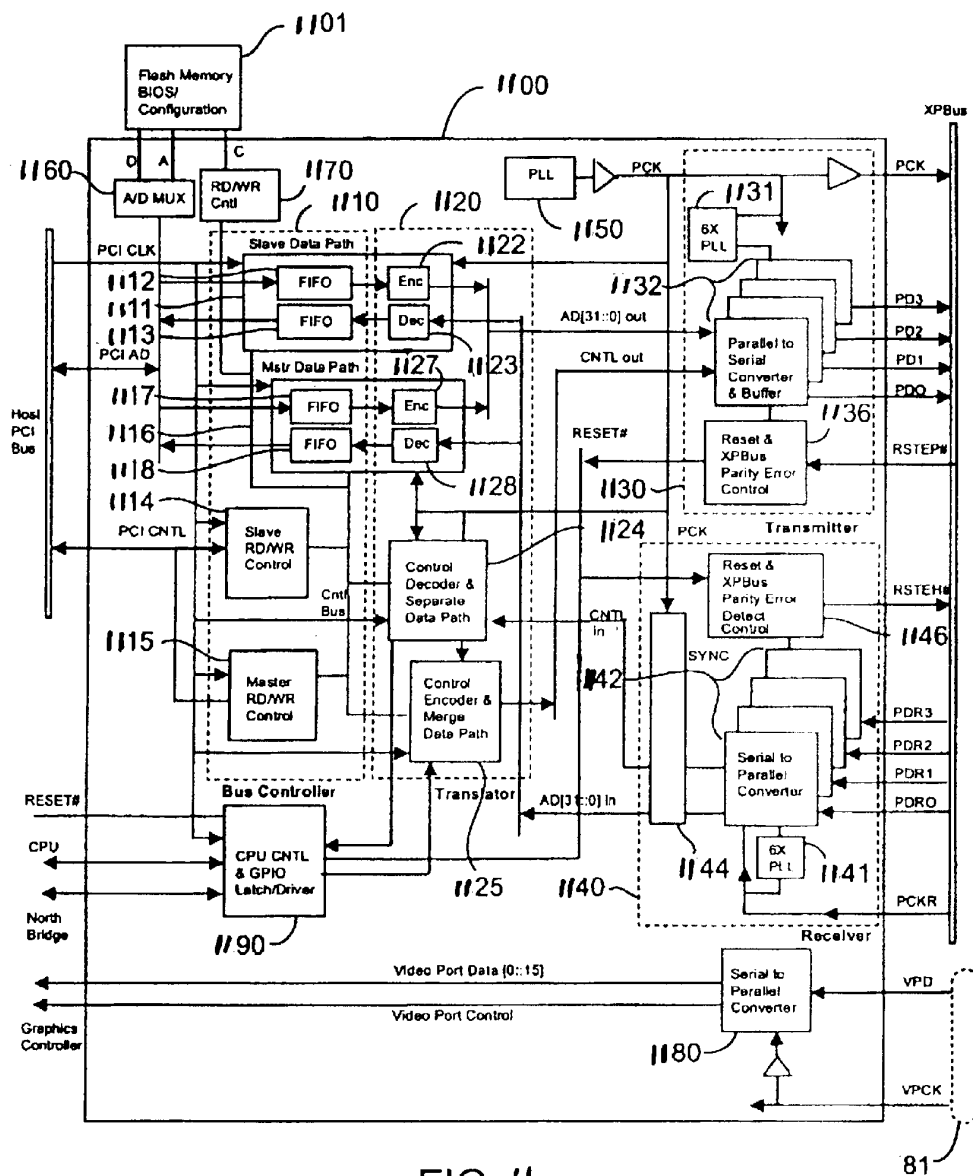


FIG. II

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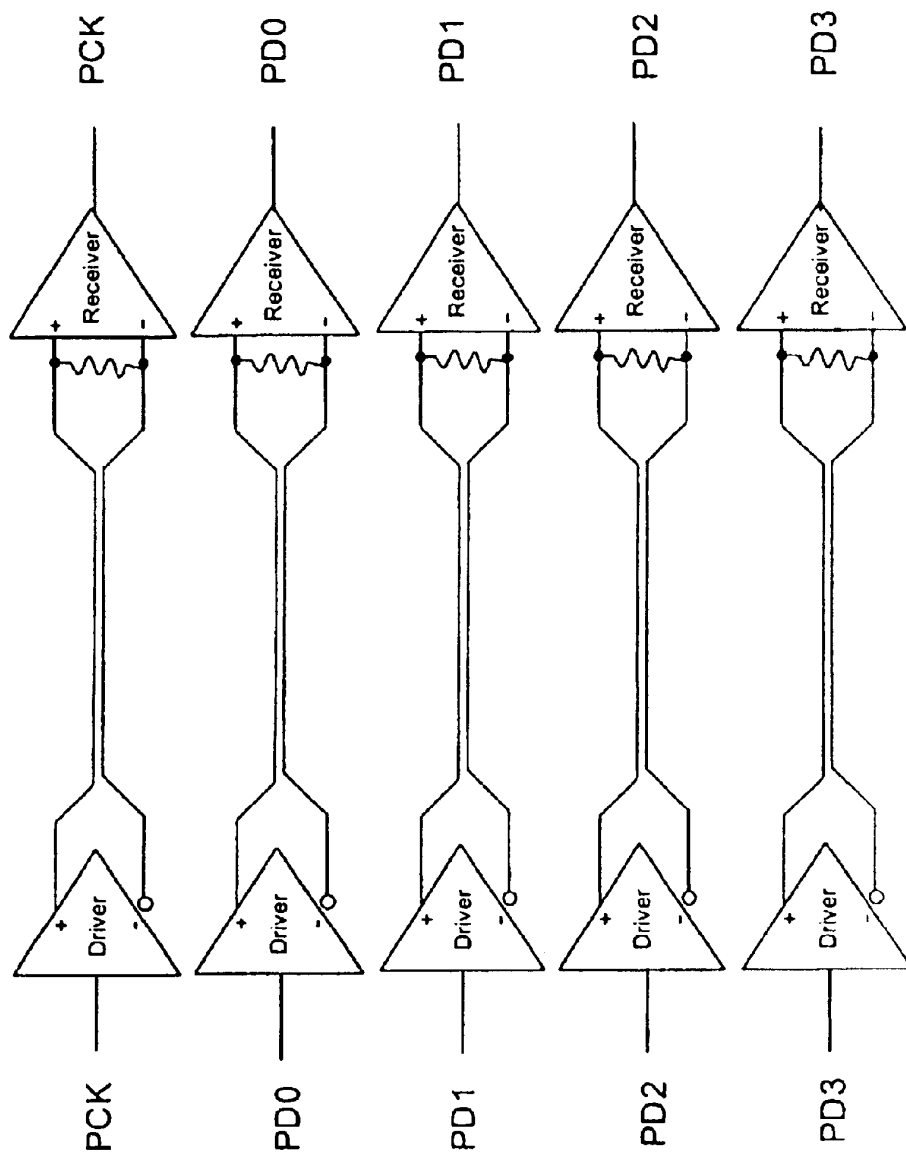


FIG. 12

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PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

CROSS REFERENCE TO RELATED  
APPLICATIONS

[The following two commonly-owned copending applications, including this one, are being filed concurrently and the other one is hereby incorporated by reference in their entirety for all purposes:]

[1. U.S. patent application Ser. No. 09/183,816, William W. Y. Chu, entitled, "Modular Computer Security Method and Device". and]

[2. U.S. patent application Ser. No. 09/183,493, William W. Y. Chu, entitled, "Password Protected Modular Computer Method and Device".]

*Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,321,335. The reissue applications are application Ser. No. 10/963,825 filed Oct. 12, 2004, application Ser. No. 11/474,256 filed Jun. 23, 2006 (the present application), application Ser. No. 11/517,601 filed Sep. 6, 2006, and application Ser. No. 12/322,858 filed Feb. 5, 2009, the present application being a continuation reissue of U.S. Pat. No. 6,321,335.*

## BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box using password protection techniques. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripherals devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and other. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to

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a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics, accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations



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can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have proprietary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

Thus what is needed are computer systems that provide reduced user investment in redundant computer components and provide a variable level of performance based upon computer configuration.

## SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent "finger print" on the attached computer module.

In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module ("ACM") into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., flat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The

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present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified side-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention;

FIG. 5 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention; and

FIGS. 6 and 7 show simplified flow diagrams of security methods according to embodiments of the present invention.

FIG. 8 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention.

FIG. 9 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 10 is a block diagram of another embodiment of the HIC and PIC of the present invention and the interface therebetween.

FIG. 11 is a detailed block diagram of another embodiment of the HIC of the present invention.

FIG. 12 is a schematic diagram of the signal lines PCK and PD0 to PD3.

## DESCRIPTION OF SPECIFIC EMBODIMENTS

## I. System Hardware

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 1 includes an attached computer module (i.e., ACM) 10, a desktop console 20, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, ACM 10 includes computer components, as will be described below, including a central processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 40 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM 10. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending patent appli-

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cation Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998, commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking system includes at least a key 11. The key 11 mates with key hole 13 in a lock, which provides a mechanical latch 15 in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the Fig. below.

FIG. 2 is a simplified diagram of a computer module 10 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous Fig. for easy reading. The computer module 10 includes key 11, which is insertable into keyhole 13 of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening 14, which allows the latch to move into and out of the ACM. The ACM also has openings 17 in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. 3 is a simplified side-view diagram of a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. As shown, the ACM module inserts into the computer module bay frame 19, which is in the console. A side 27 and a bottom 19 of ACM slide and fit firmly into the computer module bay frame, which has at least a bottom portion 19 and back portion 26. A backside 23 of the ACM faces backside 26 of the frame. ACM also has a front-side or face 25 that houses the lock and exposes the keyhole 13 to a user. The key 11 is insertable from the face into the keyhole.

As the ACM inserts into the frame, connector 17 couples and inserts into connector 21. Connector 17 electrically and mechanically interface elements of the ACM to the console through connector 21. Latch 14 should be moved away from the bottom side 19 of the module bay frame before inserting the ACM into the frame. Once the ACM is inserted fully into the frame, latch 15 is placed in a closed or lock position, where it keeps the ACM firmly in place. That is, latch 15 biases against a backside portion 29 of the ACM enclosure to hold the ACM in place, where the connector 17 firmly engages, electrically and mechanically, with connector 21. To remove the ACM, latch 15 is moved away or opened from the back side portion of the ACM enclosure. ACM is manually pulled out of the computer module bay frame, where connector 17 disengages with connector 21. As shown, the key 11 is used to selectively move the latch in the open or locked position to secure the ACM into the frame module.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

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- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

FIG. 4 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 10, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 400, and a second portion, which includes a hard drive module 420. A common printed circuit board 437 houses these modules and the like. Among other features, the ACM includes the central processing unit module 400 with a cache memory 405, which is coupled to a north bridge unit 421, and a host interface controller 401. The host interface controller includes a lock control 403. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 17. Here, the CPU module is spatially located near connector 17.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 401 is coupled to BIOS/flash memory 405. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 403 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 420. Among other elements, the hard drive module includes north bridge 421, graphics accelerator 423, graphics memory 425, a power controller 427, an IDE controller 429, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus 431, 432. A power regulator 435 is disposed near the PCI bus.

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In a specific embodiment, north bridge unit **421** often couples to a computer memory, to the graphics accelerator **423**, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator **423** typically couples to a graphics memory **423**, and other elements. IDE controller **429** generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **420** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **420** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame the provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

FIG. 5 is a simplified block diagram **500** of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram **500** has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram is an attached computer module **500**. The module **500** has a central processing unit, which communicates to a north bridge **541**, by way of a CPU bus **527**. The north bridge couples to main memory **523** via memory bus **529**. The main memory can be any suitable high speed

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memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem **515** via bus **542**. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **502** and **531**. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus **537** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **505** with a BIOS. The flash memory device **505** also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller **507** communicates to the north bridge via bus **535** and host PCI bus. The host interface controller also has a lock control **509**, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller **507** communicates to the console using bus **511**, which couples to connection **513**.

In one aspect of the present invention the security system uses a combination of electrical and mechanical locking mechanisms. Referring to FIG. 5A, for example, the present system provides a lock status mechanism in the host interface controller **509**. The lock status of the lock is determined by checking a lock status bit **549**, which is in the host interface controller. The lock status bit is determined by a signal **553**, which is dependent upon the position of the lock. Here, the position of the lock is closed in the ground **559** position, where the latch couples to a ground plane in the module and/or system. Alternatively, the signal of the lock is at Vcc, for example, which is open. Alternatively, the signal can be ground in the open position and Vcc in the closed position, depending upon the application. Other signal schemes can also be used depending upon the application.

Once the status is determined, the host interface controller turns the lock via solenoid **557** in a lock on or lock off position, which is provided through the control bit **551**, for example. The control bit is in a register of the host interface controller in the present example. By way of the signal schemes noted and the control bit, it is possible to place the lock in the lock or unlock position in an electronic manner. Once the status of the lock is determined, the host interface controller can either lock or unlock the latch on the module using a variety of prompts, for example.

In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unau-



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thorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device 505. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

In a specific embodiment, the present invention also includes a real-time clock 510 in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz 508 that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source 506 such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

## II. SECURITY DETECTION PROGRAMS

FIGS. 6 and 7 show simplified flow diagrams 600, 700 of security methods according to embodiments of the present invention. These diagrams are merely illustrations and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Referring to FIG. 6, which considers an example for when the ACM is inserted into the computer module bay in the console, ACM has already been inserted into the console and is firmly engaged in an electrical and mechanical manner. A computer system is powered up 601, which provides selected signals to the microprocessor.

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The microprocessor oversees the operation of the computer system. The microprocessor searches the memory in, for example, the hard disk drive and execute a security program, step 603.

The security program runs through a sequence of steps before allowing a user to operate the present system with the ACM. Among other processes, the security program determines if an "Auto-lock" is ON. If so, the security program goes via branch 606 to step 607. Alternatively, the security program goes to step 609, which determines that the lock stays OFF and loops to step 627, which indicates that the ACM can be removed physically from the console. In step 607, the security program turns a switch or switching means that turns ON a lock, which can be electrical, mechanical, or a combination of electrical and mechanical.

In a specific embodiment, the security program turns OFF the power of the ACM and console. Here, the security program directs the OS to turn the power OFF, step 613. In an embodiment where power failure occurs (step 611), a key is used to release a latch in the ACM on the lock 615, where the ACM can be removed, step 627. From step 613, the security program determines if the ACM is to be removed, step 617. If not, the lock stays ON, step 619. Alternatively, the security detection program determines if the password (or other security code) matches with the designated password, step 621. If not, the lock stays ON, step 623. Alternatively, the security program releases the lock 625, which frees the ACM. Next, the ACM can be removed, step 627.

In an alternative embodiment, the present invention provides a security system for the ACM, which is outside the console or computer module bay. See, FIG. 7, for example. As shown, the security system is implemented to prevent illegal or unauthorized use (step 701) of the ACM, which has not been used in the console. Here, a key turns ON a lock (step 703). The lock moves a latch in the ACM to a specific spatial location that physical blocks the passage of the ACM into the computer module bay. Accordingly, the ACM cannot insert (step 705) into the computer module bay.

In an alternative aspect, the key can be used to turn the lock OFF, step 707. Here, the key moves the latch in a selected spatial location that allows the ACM to be inserted into the computer bay module. In the OFF position, the ACM inserts into the computer module bay, step 709. Once the ACM is in the bay, a user can begin operating the ACM through the console. In one embodiment, the computer console including the ACM goes through the sequence of steps in the above FIG., but is not limited.

In a specific embodiment, the present invention implements the sequences above using computer software. In other aspects, computer hardware can also be used and is preferably in some applications. The computer hardware can include a mechanical lock, which is built into the ACM. An example of such mechanical lock is shown above, but can also be others. In other aspects, the lock can be controlled or accessed electronically by way of computer software. Here, the key can be used to as a manual override if the ACM or computer fails.

The lock is used to prevent theft and accidental removal inside CMB. The current invention locates the lock inside the ACM to allow a user to keep a single key as ACM is moved from console to console at different locations. When ACM is in transit, the lock can be engaged using the key so that the latch extends outside ACM's enclosure. The extended latch prevents ACM from being inserted into any CMB. This prevents any illegal use of ACM by someone other than the user.

In one aspect of the invention, the user password is programmable. The password can be programmable by way of

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the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

Embodiments in accordance with the present invention may interface two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In accordance with embodiments of the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the

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number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

FIG. 8 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention. As shown in FIG. 8, HIC 800 comprises bus controller 810, translator 820, transmitter 830, receiver 840, a PLL 850, an address/data multiplexer (A/D MUX) 860, a read/write controller (RD/WR Cntl) 870, a video serial to parallel converter 880 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 890.

HIC 800 is coupled to an optional flash memory BIOS configuration unit 801. Flash memory unit 801 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 860 and RD/WR Control 870, which control the programming, read, and write of flash memory unit 801.

Bus controller 810 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 810 includes a slave (target) unit 811 and a master unit 816. Both slave unit 811 and master unit 816 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 816 as well as the two FIFOs in the slave unit 811 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 811 includes encoder 822 and decoder 823, while master unit 816 includes encoder 827 and decoder 828. The FIFOs 812, 813, 817 and 818 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 8 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 812 and 817 before they are encoded by encoders 822 and 823. Encoders 822 and 823 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 823 and 828 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 813 and 818 prior to being transferred to the host PCI bus. FIFOs 812, 813, 817 and 818, allow bus controller 810 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller 810 also comprises slave read/write control (RD/WR Cntl) 814 and master read/write control (RD/WR Cntl) 815. RD/WR controls 814 and 815 are involved in the transfer of PCI control signals between bus controller 810 and the host PCI bus.

Bus controller 810 is coupled to translator 820. Translator 820 comprises encoders 822 and 827, decoders 823 and 828, control decoder & separate data path unit 824 and control encoder & merge data path unit 825. As discussed above encoders 822 and 827 are part of slave data unit 811 and master data unit 816, respectively, receive PCI address and data information from FIFOs 812 and 817, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to

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transmittal on the XPBus. Similarly, decoders 823 and 828 are part of slave data unit 811 and master data unit 816, respectively, and format address and data information from receiver 840 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 825 receives PCI control signals from the slave RD/WR control 814 and master RD/WR control 815. Additionally, control encoder & merge data path unit 825 receives control signals from CPU CNTL & GPIO latch/driver 890, which is coupled to the CPU and north bridge (not shown in FIG. 8). Control encoder & merge data path unit 825 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 830, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 824 receives control bits from receiver 840 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 824 separates the control bits it receives from receiver 840 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

Transmitter 830 receives multiplexed parallel address/data (A/D) bits and control bits from translator 820 on the AD[31:0] out and the CNTL out lines, respectively. Transmitter 830 also receives a clock signal from PLL 850. PLL 850 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 66 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 66 MHz rather than 33 MHz or having 64 rather than 32 multiplexed address/data lines.

The multiplexed parallel A/D bits and some control bits input to transmitter 830 are serialized by parallel to serial converters 832 of transmitter 830 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 833 into 10 bit packets and send out on control line PCN of the XPBus.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 9, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physi-

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cal or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

FIG. 9 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 9, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 9 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

FIG. 10 is a block diagram of another embodiment of the HIC and PIC of the present invention and the interface therebetween. One important difference between the XPBuses shown in FIGS. 8 and 10 is the fact that unlike the XPBus of FIG. 8, the XPBus of FIG. 10 does not have control lines PCN and PCNR. Another difference lies in the fact that the XPBus of FIG. 10 has two dedicated reset lines RSTEH# and RSTEP# instead of only one as is the case for the XPBus of FIG. 8. RSTEH# and RSTEP# are unidirectional reset and error condition signal lines that transmit a reset and error condition signal from the host PCI to the peripheral PCI and from the peripheral PCI to host PCI, respectively.

FIG. 11 shows a detailed block diagrams of the HIC shown in FIG. 10. HIC 1100 shown in FIG. 11 is, other than for a few difference, identical to HIC 800 shown in FIG. 8. Accordingly, reference numbers for components in HIC 1100 have been selected such that a component in HIC 1100 and its corresponding component in HIC 800 have reference numbers that differ by 300 and have the same two least significant digits. One of the differences between HIC 1100 and HIC 800 is the fact that, unlike HIC 800, HIC 1100 does not have a parallel to serial converter or a serial to parallel converter dedicated exclusively to CNTL out and CNTL in



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signals, respectively. This is due to the fact that XPBus for HIC 1100 does not contain a PCN or PCNR line. Another important difference between HIC 1100 and HIC 800 is the fact that HIC 1100, unlike HIC 800, has two reset lines, RSTEP# and RSTE#H, instead of only one reset line. Reset line RSTEP# is coupled to Reset & XPBus Parity Error Control Unit 1136 which receives, on the reset line RSTEP#, a reset signal and a parity error signal generated by the PIC, sends a reset signal to the CPU CNTL & GPIO latch/driver 1190, and controls retransmission of bits from the parallel to serial converters 1132. Reset & XPBus Parity Error Detection and Control Unit 1146 takes bits from serial to parallel converters 1142, performs a parity check to detect any transmission error, and sends reset and parity error signals to the PIC on the reset line RSTE#H. The reset and parity error signals may be distinguished by different signal patterns and/or different signal durations. In the two reset line system, the reset and error parity signals are transmitted on the same line and it is possible to send a parity error confirmation signal on one line while receiving a reset signal on the other line. Because HIC 1100 provides for parity error detection, the parallel to serial converters 1132 include buffers. The buffers in parallel to serial converters 1132 store previously transmitted bits (e.g., those transmitted within the previous two clock cycles) for retransmission if transmission error is detected and a parity error signal is received on line RSTEP#. It is to be noted that parallel to serial converters 832 do not contain buffers such as those contained in parallel to serial converters 1132 for purposes of retransmission since HIC 800 does not provide for parity error signal detection. Yet another difference between HIC 800 and HIC 1100 is the fact that in HIC 1100 clock multipliers 1131 and 1141 multiply the PCK and PCKR clocks, respectively, by a factor of 6 rather than 10 because the XPBus coupled to HIC 1100 transmits six bit packets instead of ten bit packets during each XPBus clock cycle. Sending a smaller number of bits per XPBus clock cycle provides the benefit of improving synchronization between the data latching clock output by clock multipliers 1131 and 1141 and the XPBus clocks, PCK and PCKR. In another embodiment, one may send 5 or some other number of bits per XPBus clock cycle. As mentioned above, the remaining elements in HIC 1100 are identical to those in HIC 800 and reference to the description of the elements in HIC 800 may be made to understand the function of the corresponding elements in HIC 1100.

FIG. 12 is a schematic diagram of the lines PCK and PD0 to PD3. These lines are unidirectional LVDS lines for transmitting signals from HIC 1100 to the PIC of FIG. 10. Another set of lines, namely PCKR and PDR0 to PDR3, are used to transmit clock signals and bits from the PIC to HIC 1100.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

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What is claimed is:

- [1. A computer module, said module comprising: an enclosure, said enclosure being insertable into a console; a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip; a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit; and a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing a possibility of unauthorized use of said hard disk drive.]
- [2. The computer module of claim 1 further comprising a host interface controller for providing a status of a locking device in said enclosure.]
- [3. The computer module of claim 1 further comprising a mechanical locking device that is coupled to said programmable memory device.]
- [4. The computer module of claim 1 further comprising a host interface controller coupled to a mechanical locking device, said host interface controller being coupled to said programmable memory device.]
- [5. The computer module of claim 1 wherein said programmable memory device comprises a flash memory device.]
- [6. The computer module of claim 1 wherein said programmable memory device comprises a flash memory device having at least 8 Mbits of cells and greater.]
- [7. The computer module of claim 1 further comprising a security program in a main memory.]
- [8. The computer module of claim 7 wherein said security program comprises a code for storing a password on said programmable memory device.]
- [9. The computer module of claim 8 wherein said security program comprises a code for checking a time from said real-time clock circuit.]
- [10. The computer module of claim 1 further comprising a host interface controller coupled to a solenoid that drives a mechanical lock in a first position to a second position.]
- [11. The computer module of claim 10 wherein said solenoid also drives said mechanical lock from said second position to said first position.]
- [12. The computer module of claim 1 further comprising a real-time clock circuit coupled to said central processing unit.]
- [13. The computer module of claim 12 further comprising a battery coupled to a host interface controller that includes said real-time clock.]
- [14. A method for operating a computer system, said method comprising: inserting an attached computer module ("ACM") into a bay of a modular computer system, said ACM comprising a microprocessor unit coupled to a mass memory storage device; applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and prompting for a user password from a user on a display.]
- [15. The method of claim 14 wherein said ACM comprises an enclosure that houses said microprocessor unit and said mass memory storage device.]
- [16. The method of claim 14 further comprising providing a user password to said security program.]
- [17. The method of claim 14 further comprising a flash memory device for storing a desired password for said ACM.]

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[18. The method of claim 17 wherein said flash memory device maintains said desired password when power is removed from said ACM.]

[19. The method of claim 18 wherein said flash memory device is coupled to a host interface controller that is coupled to said microprocessor based unit.]

[20. The method of claim 14 wherein said mass memory storage device comprises a code directed to comparing said user password with a desired password.]

[21. The method of claim 14 further comprising identifying a permanent password or user code on said attached computer module.]

[22. The method of claim 21 wherein said permanent password or user code is stored in said microprocessor unit.]

[23. The method of claim 21 wherein said permanent password or user code is stored in a flash memory device coupled to said microprocessor unit.]

24. A computer module, said module comprising:

an enclosure, said enclosure being insertable into a console;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

an interface controller coupled to a differential signal channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

25. The computer module of claim 24 wherein the encoded serial bit stream comprises 10 bit packets.

26. The computer module of claim 24 wherein the serial bit stream of PCI bus transaction comprises encoded PCI address and data bits.

27. The computer module of claim 24 wherein the computer module communicates to the console through serial bit based lines transmitting data packets in Universal Serial Bus (USB) protocol.

28. A computer module comprising:

an enclosure insertable into a console to form a functional computer, said console comprising a first interface controller;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a second interface controller coupled to the first interface controller through a differential signal channel comprising two sets of unidirectional serial bit channels in opposite directions which transmit data in 10 bit packets; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

29. The computer module of claim 28 wherein the differential signal channels communicate an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus address and data transaction.

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30. The computer module of claim 28 further comprising a security program configured to manage a user's access privilege of data based on said password.

31. A computer module comprising:

an enclosure being insertable into a console;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

an interface controller coupled to a differential signal channel for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, wherein the differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive;

wherein the computer module communicates to the console through serial bit based lines transmitting data packets in Universal Serial Bus (USB) protocol.

32. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a modular computer system, said ACM comprising,

an interface controller coupled to a differential signal channel for communicating encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction, the differential signal channel transmitting data in two sets of unidirectional serial bit channels in opposite directions, and

a microprocessor unit coupled to a mass memory storage device;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and

prompting for a user password from a user on a display.

33. The method of claim 32 wherein said security program is configured to manage a user's privilege to access data based on said password.

34. The method of claim 32 further comprises transmitting the encoded serial bit stream in 10 bit packets.

35. The method of claim 32 further comprises the serial bit stream of PCI bus transaction transmitting encoded PCI address and data bits.

36. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a modular computer system housed in a console, said console comprising a first interface controller; said ACM comprising,

a microprocessor unit coupled to a mass memory storage device including a plurality of application software program files, the microprocessor unit configured to execute the plurality of application software program files, and

a second interface controller;

applying power to said computer system such that said ACM communicates with the console through said interface controllers, the ACM executing a security program, said security program being stored in said mass storage device;

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storing a user password in said ACM; and  
 prompting for said user password from a user on a display  
 coupled to the console; wherein said interface control-  
 lers communicates through a differential signal channel  
 for communicating an encoded serial bit stream of 5  
 Peripheral Component Interconnect (PCI) bus  
 transaction, the differential signal channel transmitting  
 data in two sets of unidirectional serial bit channels in  
 opposite directions.

37. The method of claim 36 wherein said mass memory 10  
 storage device comprises flash memory.

38. The method of claim 36 wherein said security program  
 manages a user's privilege to access data based on said  
 password.

39. The method of claim 36 further comprises transmitting 15  
 the encoded serial bit stream in 10 bit packets.

40. The method of claim 36 further comprises the serial  
 bit stream of PCI bus transaction transmitting encoded PCI  
 address and data bits.

41. A computer module comprising:

an enclosure configured to be inserted into a console to 20  
 form a functional computer;

a central processing unit in said enclosure, said central  
 processing unit comprising a microprocessor based  
 integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive 25  
 coupled to said central processing unit;

a differential signal channel in said enclosure, said differ-  
 ential signal channel comprising two sets of unidirec-  
 tional serial bit channels in opposite directions; 30

a first interface controller configured to be coupled to the  
 console upon insertion of the enclosure into the  
 console, the first interface controller configured to  
 transmit Peripheral Component Interconnect (PCI) bus  
 transaction on the differential signal channel; and 35

a programmable memory device in said enclosure, said  
 programmable memory device being configurable to  
 store a password for preventing unauthorized use of  
 said hard disk drive.

42. The computer module of claim 41 wherein the first 40  
 interface controller is configured to be coupled with a sec-  
 ond interface controller of the console through the differ-  
 ential signal channel.

43. A computer module comprising:

an enclosure configured to be inserted into a console; 45

a central processing unit in said enclosure, said central  
 processing unit comprising a microprocessor based  
 integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive 50  
 being coupled to said central processing unit;

a differential signal channel in said enclosure, said differ-  
 ential signal channel comprising two sets of unidirec-  
 tional serial channels in opposite directions;

an interface controller coupled to the differential signal 55  
 channels and configured to communicate data in a form  
 of encoded bit stream of Peripheral Component Inter-  
 connect (PCI) bus transaction; and

a programmable memory device in said enclosure, said  
 programmable memory device being configurable to 60  
 store a password for preventing unauthorized use of  
 said hard disk drive.

44. A method for operating a computer system, said  
 method comprising:

inserting an attached computer module ("ACM") into a 65  
 bay of a modular computer system, said ACM  
 comprising,

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a microprocessor unit coupled to a mass memory stor-  
 age device;

a differential signal channel comprising two sets of uni-  
 directional serial channels in opposite directions; 5  
 and

an interface controller coupled to the differential signal  
 channel and configured to communicate data on the  
 serial channels comprising encoded bit stream of  
 Peripheral Component Interconnect (PCI) bus trans-  
 action;

applying power to said computer system and said ACM to  
 execute a security program, said security program  
 being stored in said mass memory storage device; and  
 prompting for a user password from a user on a display.

45. A method for operating a computer system, said  
 method comprising:

inserting an attached computer module ("ACM") into a  
 bay of a modular computer system, said ACM  
 comprising,

a microprocessor unit coupled to a mass memory stor-  
 age device;

a differential signal channel comprising two sets of uni-  
 directional serial channels in opposite directions, 20  
 and

an interface controller coupled to a connector through  
 the differential signal channel, wherein data commu-  
 nication to the serial channels comprises an encoded  
 bit stream of Peripheral Component Interconnect  
 (PCI) bus transaction;

applying power to said computer system and said ACM to  
 execute a security program, said security program  
 being stored in said mass memory storage device; and  
 prompting for a user password from a user on a display.

46. A computer module comprising:

an enclosure configured to be inserted into a slot of a  
 console comprising a power supply;

a central processing unit in said enclosure, said central  
 processing unit comprising a microprocessor based  
 integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive  
 being coupled to said central processing unit;

a low voltage differential signal (LVDS) channel in said  
 enclosure, said low voltage differential signal channel  
 comprising two sets of multiple unidirectional serial  
 differential signal channels in opposite directions;

an interface controller coupled to a connector through the  
 low voltage differential signal channel and configured  
 to communicate data in a form of encoded bit stream of  
 Peripheral Component Interconnect (PCI) bus transac-  
 tion; and

a programmable memory device in said enclosure, said  
 programmable memory device being configurable to  
 store a password for preventing unauthorized use of  
 said hard disk drive.

47. The computer module of claim 46 configured to  
 receive power from the power supply in the console after  
 insertion into the console.

48. The computer module of claim 46 wherein the LVDS  
 channel is configured to communicate in 10 bit packets.

49. The computer module of claim 46 wherein the inter-  
 face controller in the computer module is configured to  
 couple to the console upon insertion into the console.

50. A computer module comprising:

an enclosure insertable into a slot of a console to form a  
 functional computer, said console comprising a first  
 interface controller;

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a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a second interface controller coupled to the first interface controller through a low voltage differential signal (LVDS) channel comprising two sets of multiple unidirectional serial differential signal channels in opposite directions and configured to communicate data in a form of encoded bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

51. The computer module of claim 50 wherein the LVDS channel is configured to communicate in 10 bit packets.

52. The computer module of claim 50 further comprising a security program configured to manage a user's access privilege of data based on said password.

53. A computer module comprising:

an enclosure insertable into a slot of a console to form a functional computer, said console comprising a power supply;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

an interface controller coupled to the console upon insertion through a low voltage differential signal (LVDS) channel comprising two sets of multiple unidirectional serial differential signal channels in opposite directions and configured to communicate data in a form of encoded bit stream of Peripheral Component Interconnect (PCI) bus transaction; and

a programmable memory device in said enclosure, said programmable memory device being configurable to

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store a password for preventing unauthorized use of said hard disk drive.

54. The computer module of claim 53 wherein the LVDS channel is configured to communicate in 10 bit packets.

55. The computer module of claim 53 further comprising a security program configured to manage a user's access privilege of data based on said password.

56. The computer module of claim 53 configured to receive power from the power supply after insertion into the console.

57. A computer module comprising:

an enclosure configured to be inserted into a slot of a console comprising a LAN communication device;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a low voltage differential signal (LVDS) channel in said enclosure, said low voltage differential signal channel comprising two sets of multiple unidirectional serial bit channels in opposite directions and configured to communicate data in a form of encoded bit stream of Peripheral Component Interconnect (PCI) bus transaction;

an interface controller coupled to the low voltage differential signal channel; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

58. The computer module of claim 57 wherein the LVDS channel is configured to communicate in 10 bit packets.

59. The computer module of claim 57 wherein the computer module is configured to receive power to operate from a power supply in the console after insertion into the console.

\* \* \* \* \*





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**Chu**

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(54) **PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE**

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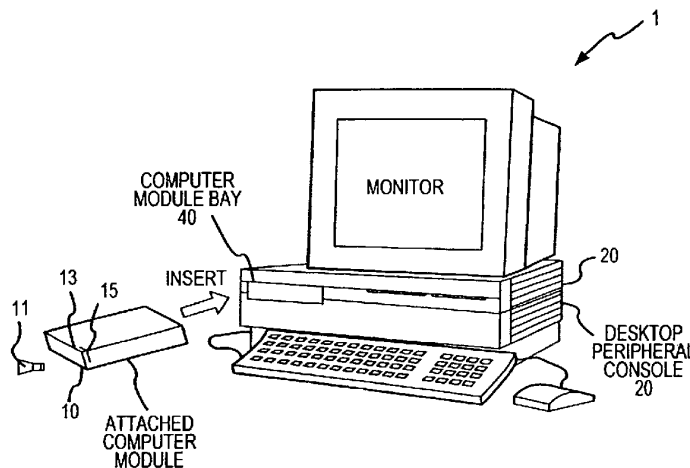
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(57) **ABSTRACT**

A method and device for securing a removable Attached Computer Module ("ACM") 10. ACM 10 inserts into a Computer Module Bay ("CMB") 40 within a peripheral console to form a functional computer such as a desktop computer or portable computer. The present ACM 10 includes a locking system, which includes hardware and software 600, 700, to prevent accidental removal or theft of the ACM from the peripheral console. While ACM is in transit, further security is necessary against illegal or unauthorized use. If ACM contains confidential data, a high security method is needed to safeguard against theft.

**30 Claims, 21 Drawing Sheets**



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- Exhibit 4, Disclosure of Asserted Claims and Infringement Contentions for Defendant Fujitsu America, Inc., submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 210 pages.
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Exhibit 7, Disclosure of Asserted Claims and Infringement Contentions for Defendant NEC Corp. Of America, submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 166 pages.

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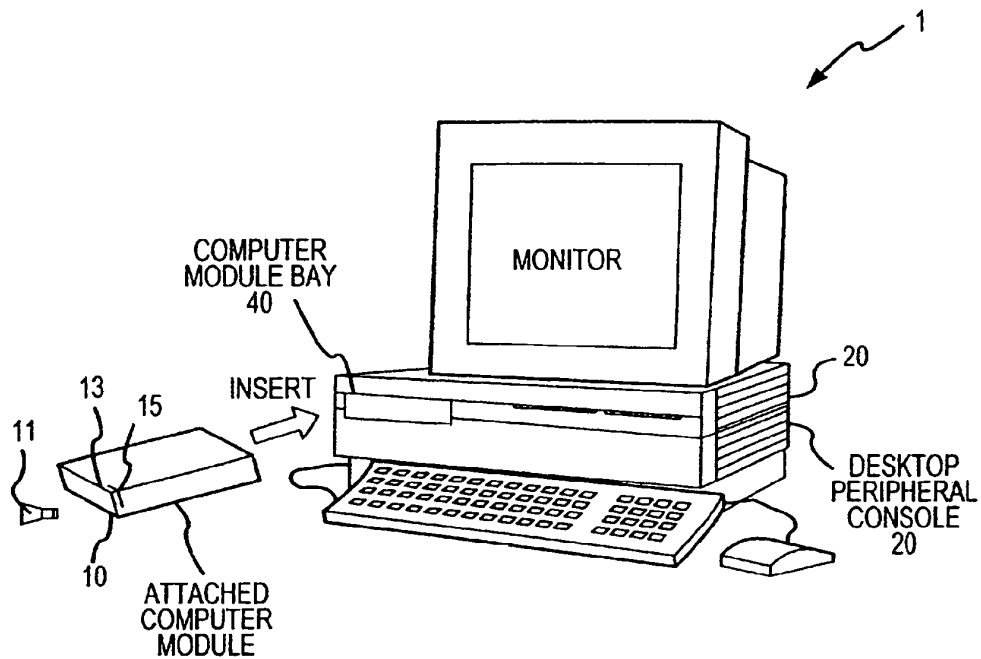


FIG.1

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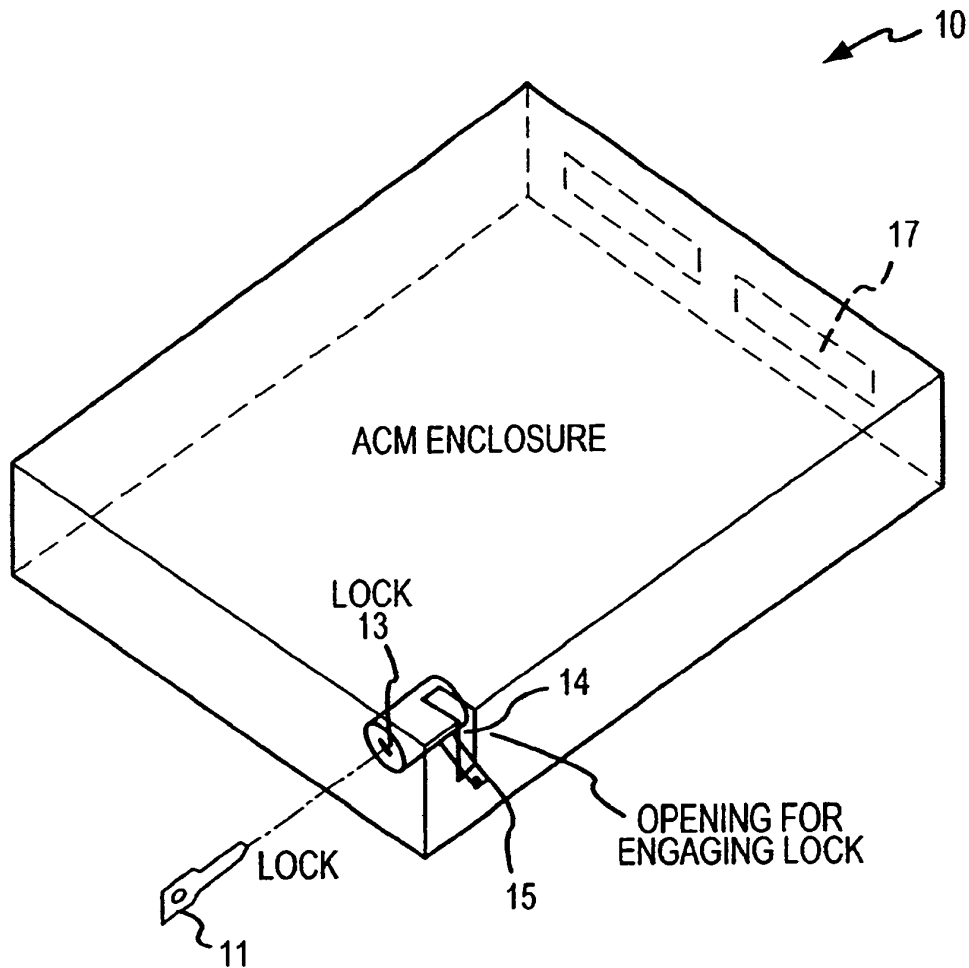


FIG.2

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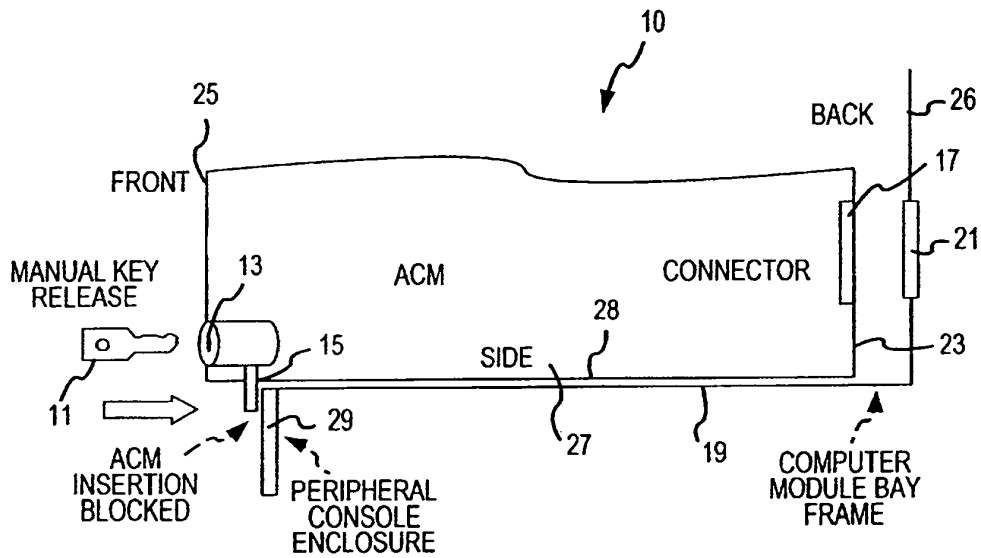


FIG.3

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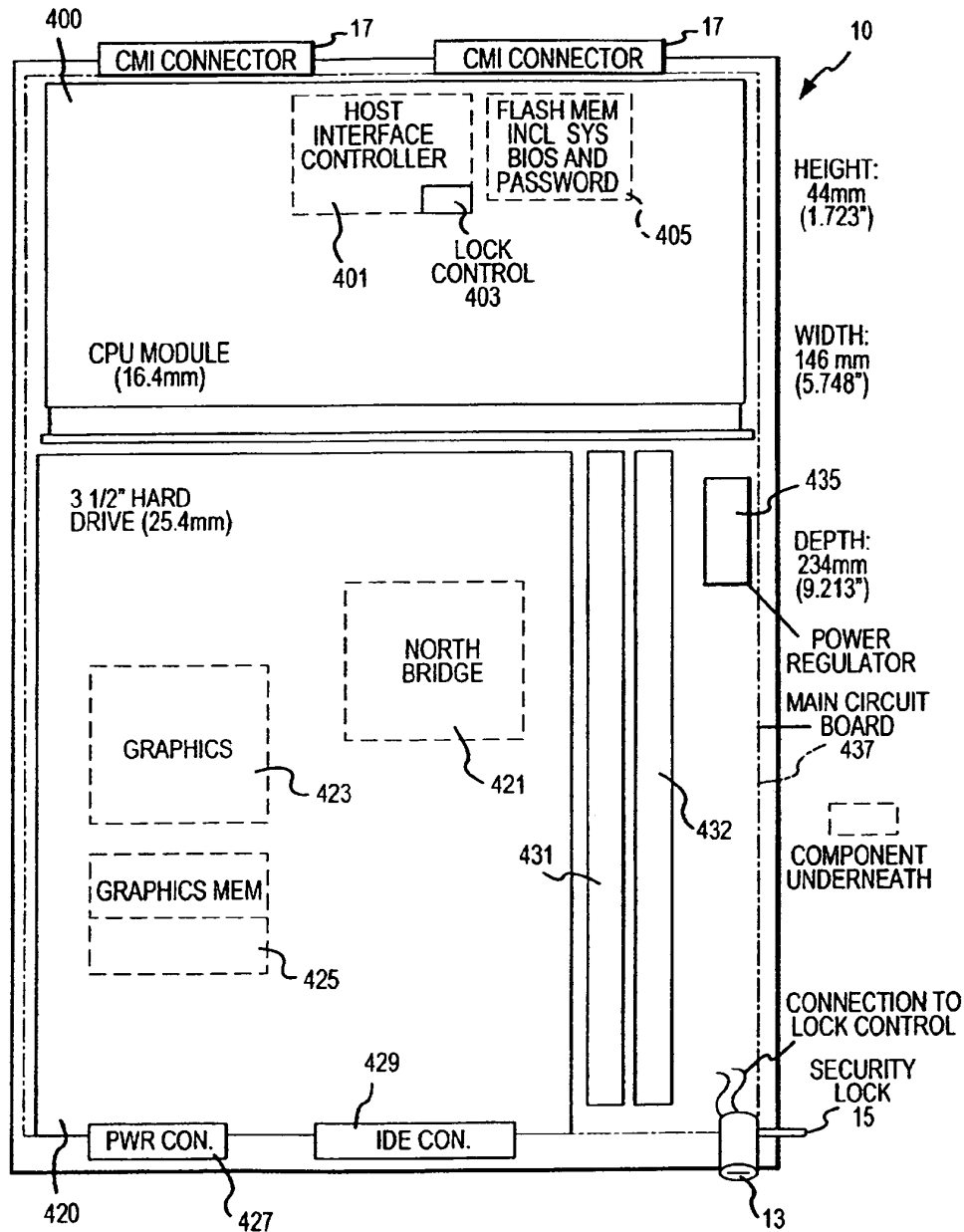


FIG.4

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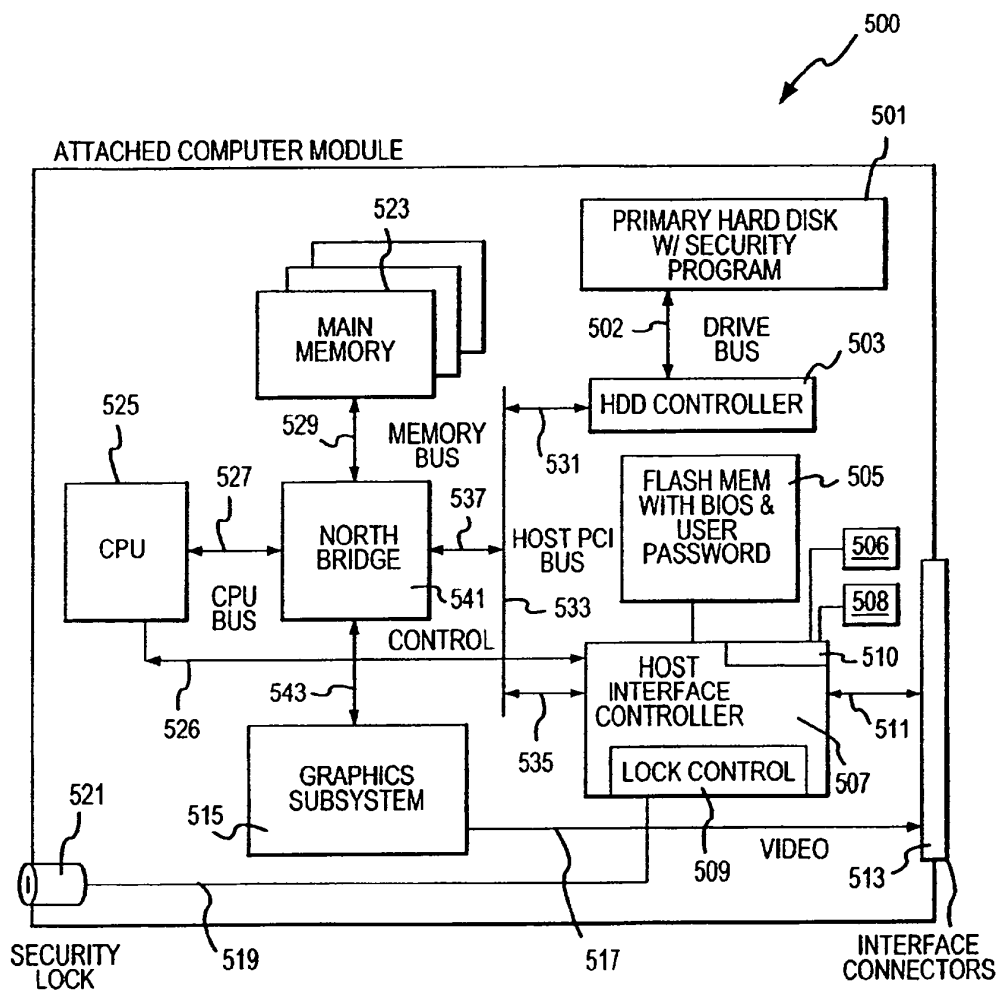


FIG.5



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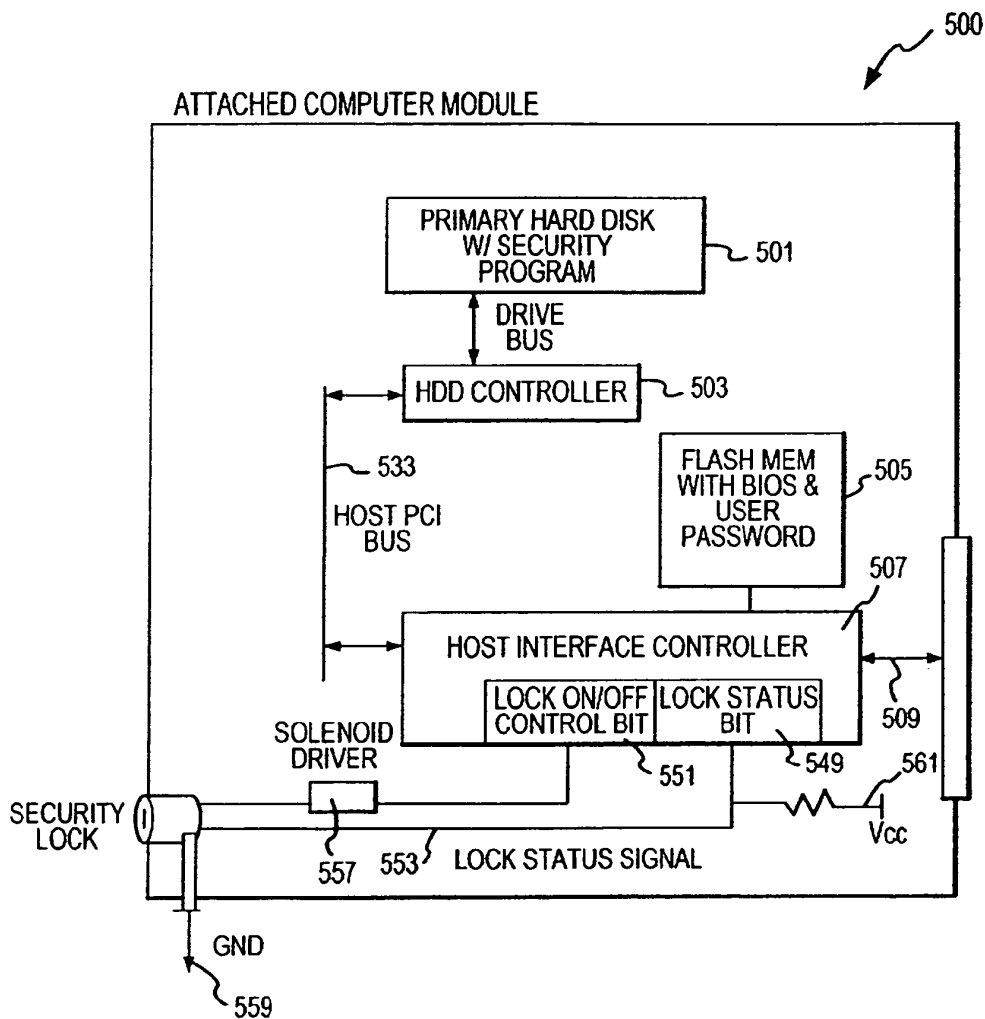


FIG.5A

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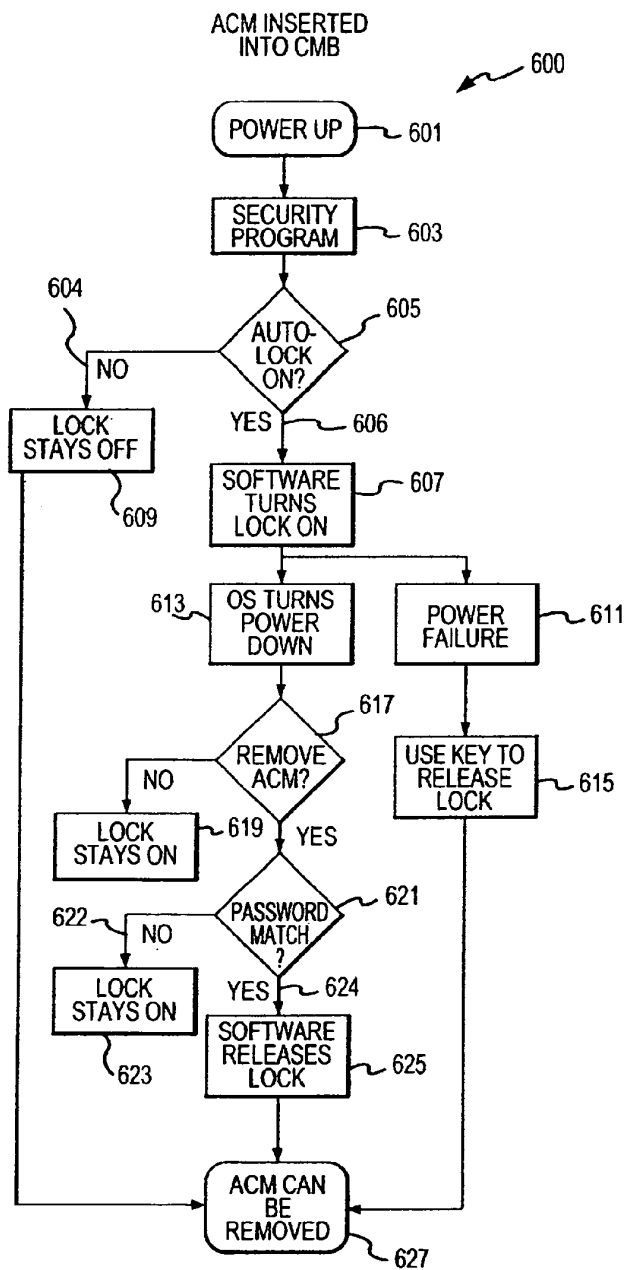


FIG.6

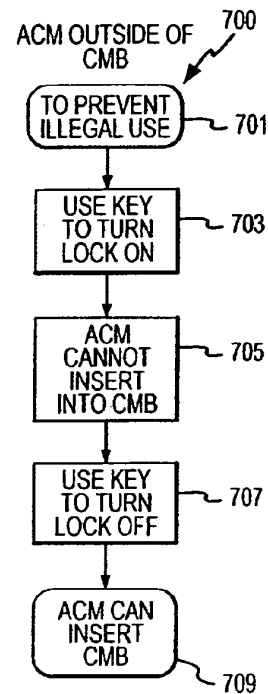


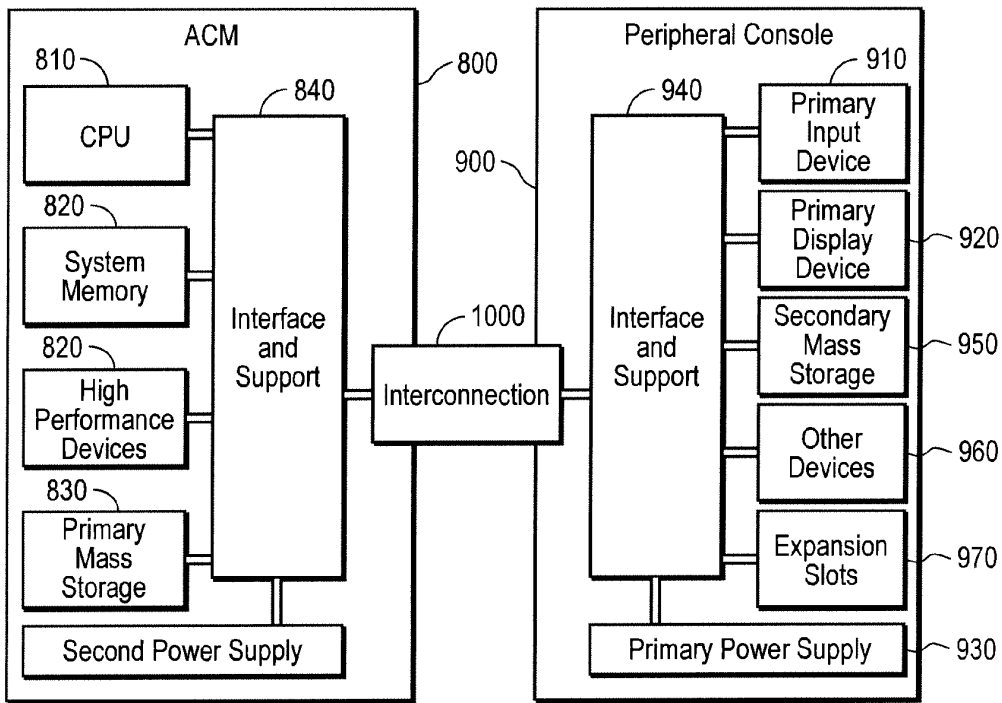
FIG.7

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**FIG. 8**

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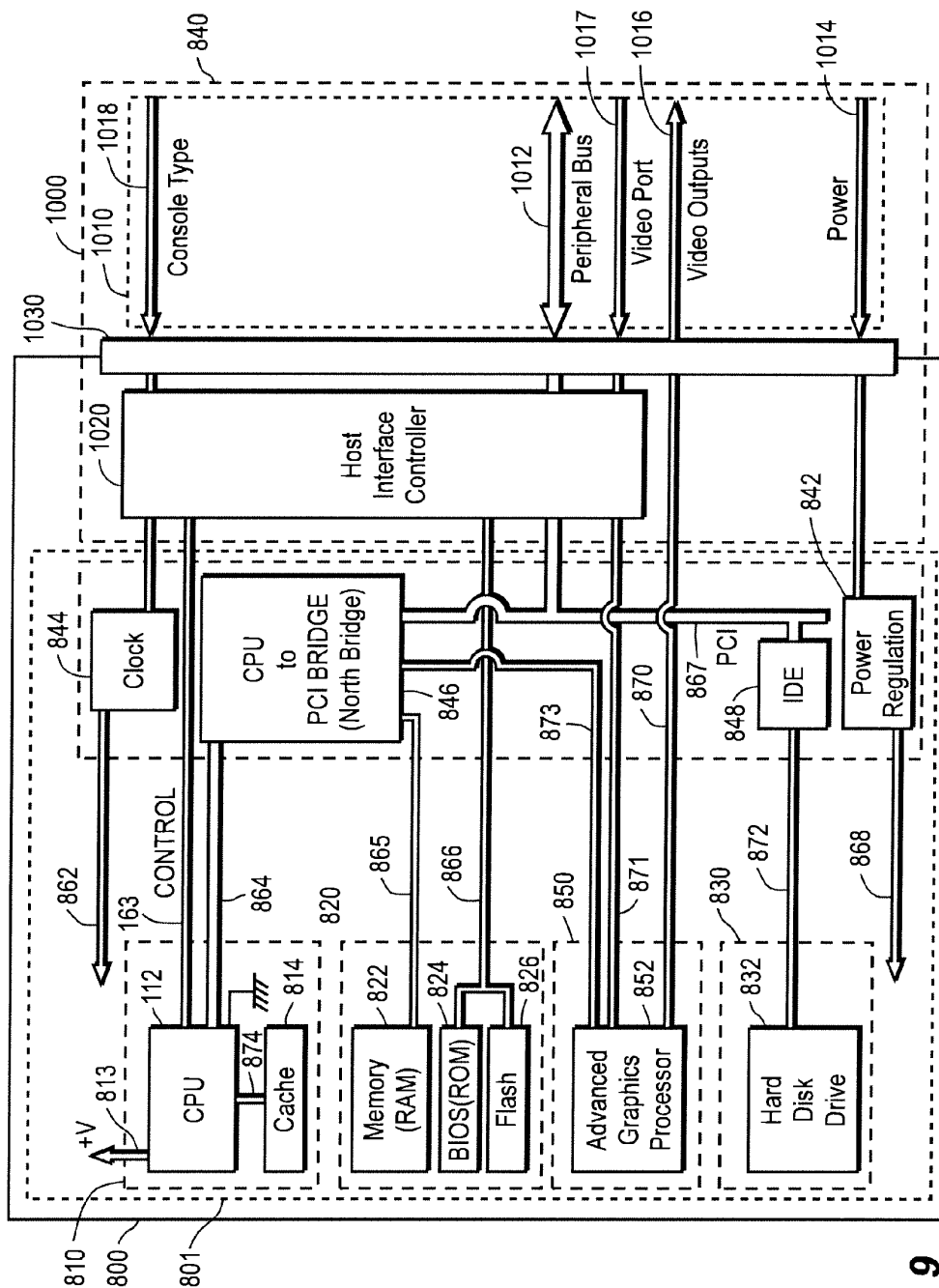
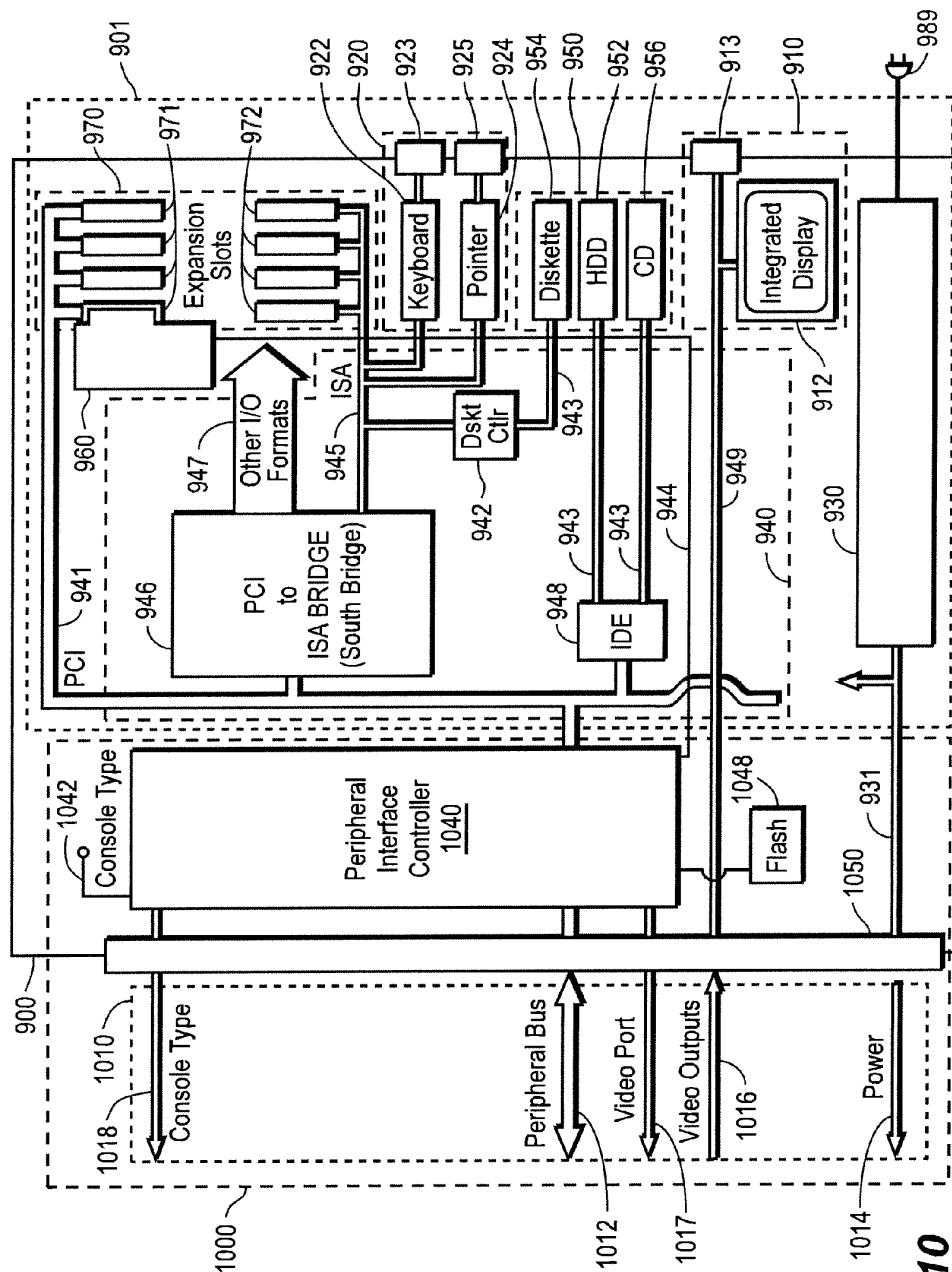


FIG. 9



**FIG. 10**

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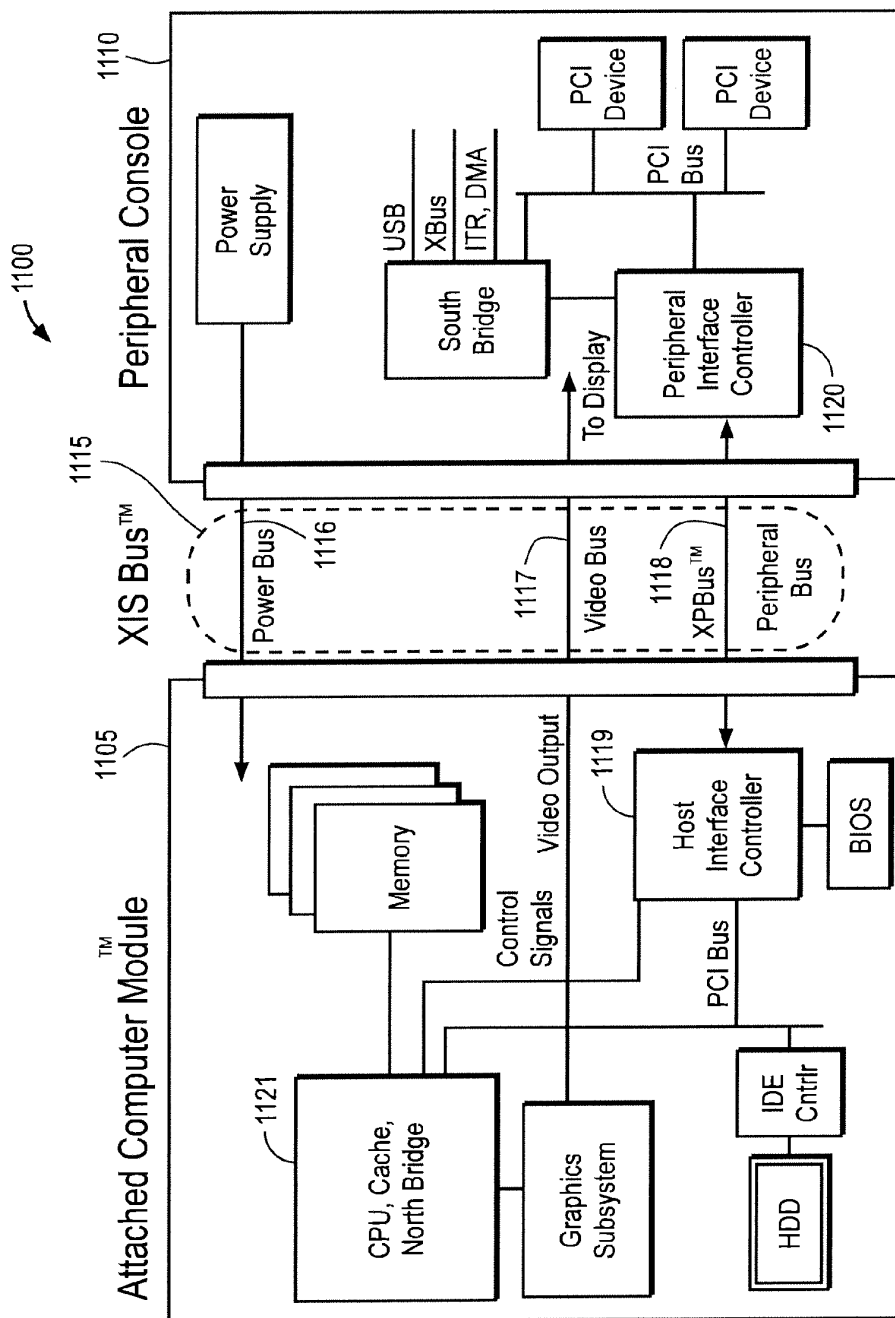


FIG. 11



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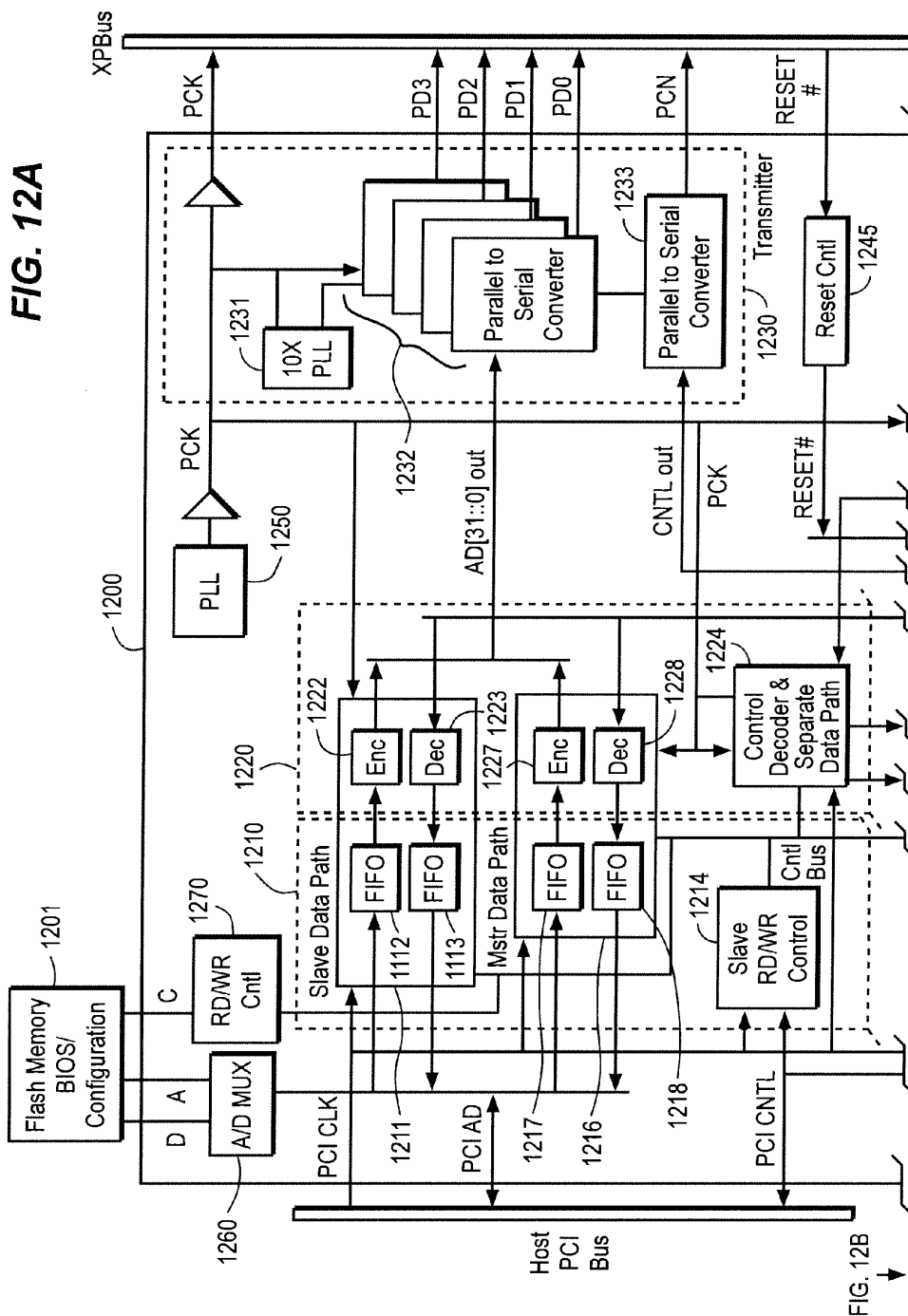


FIG. 12B

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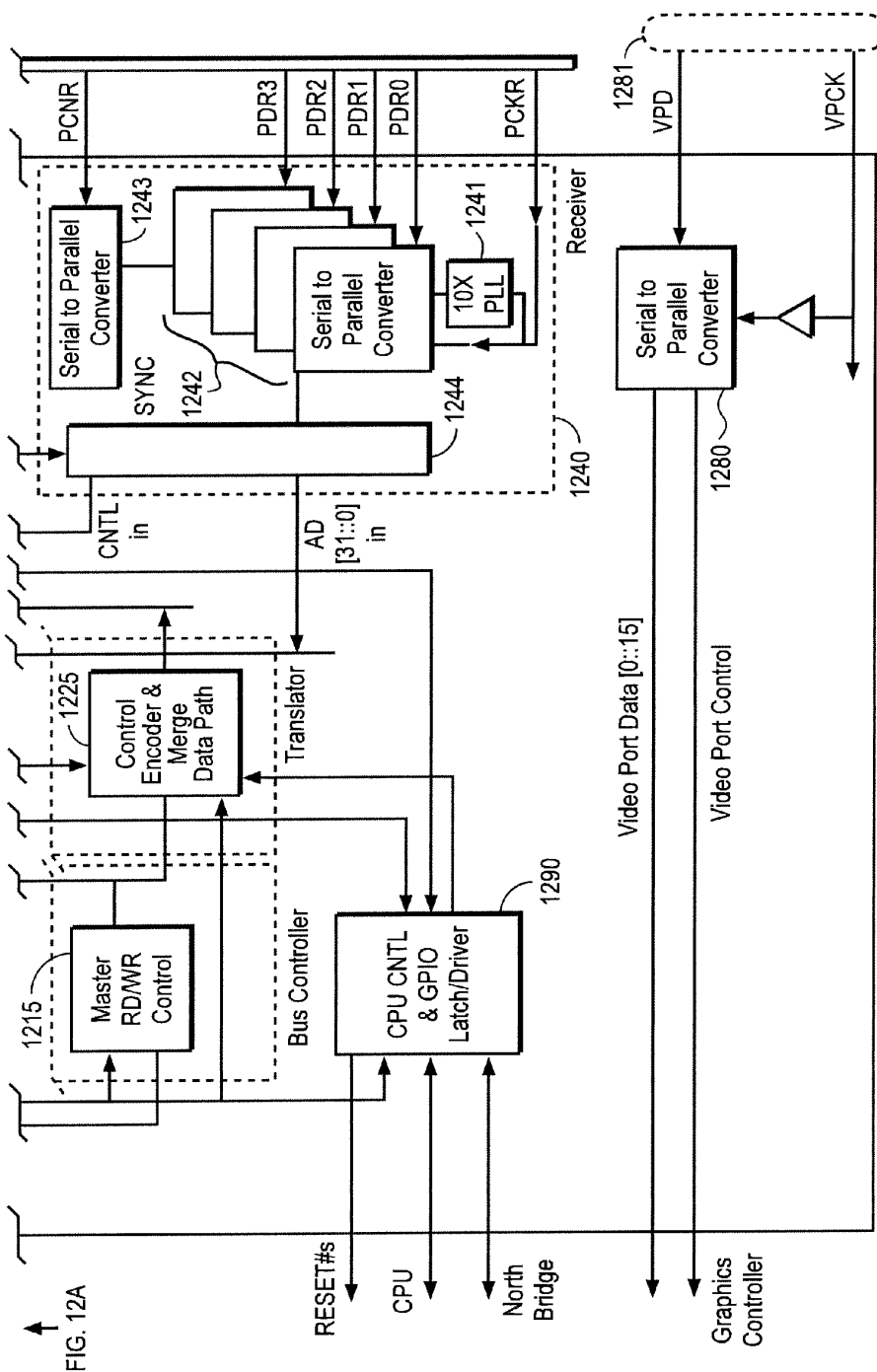


FIG. 12B

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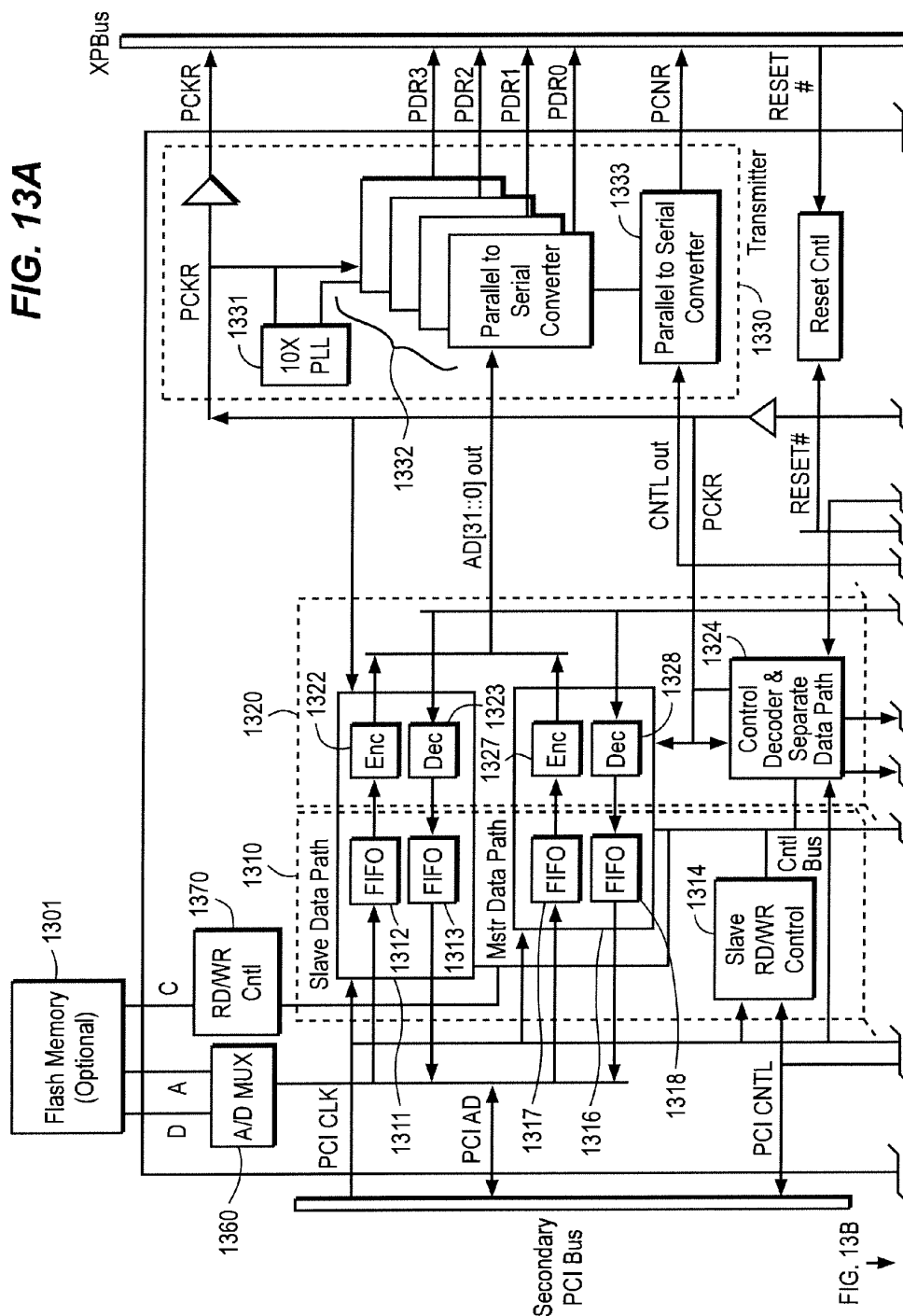
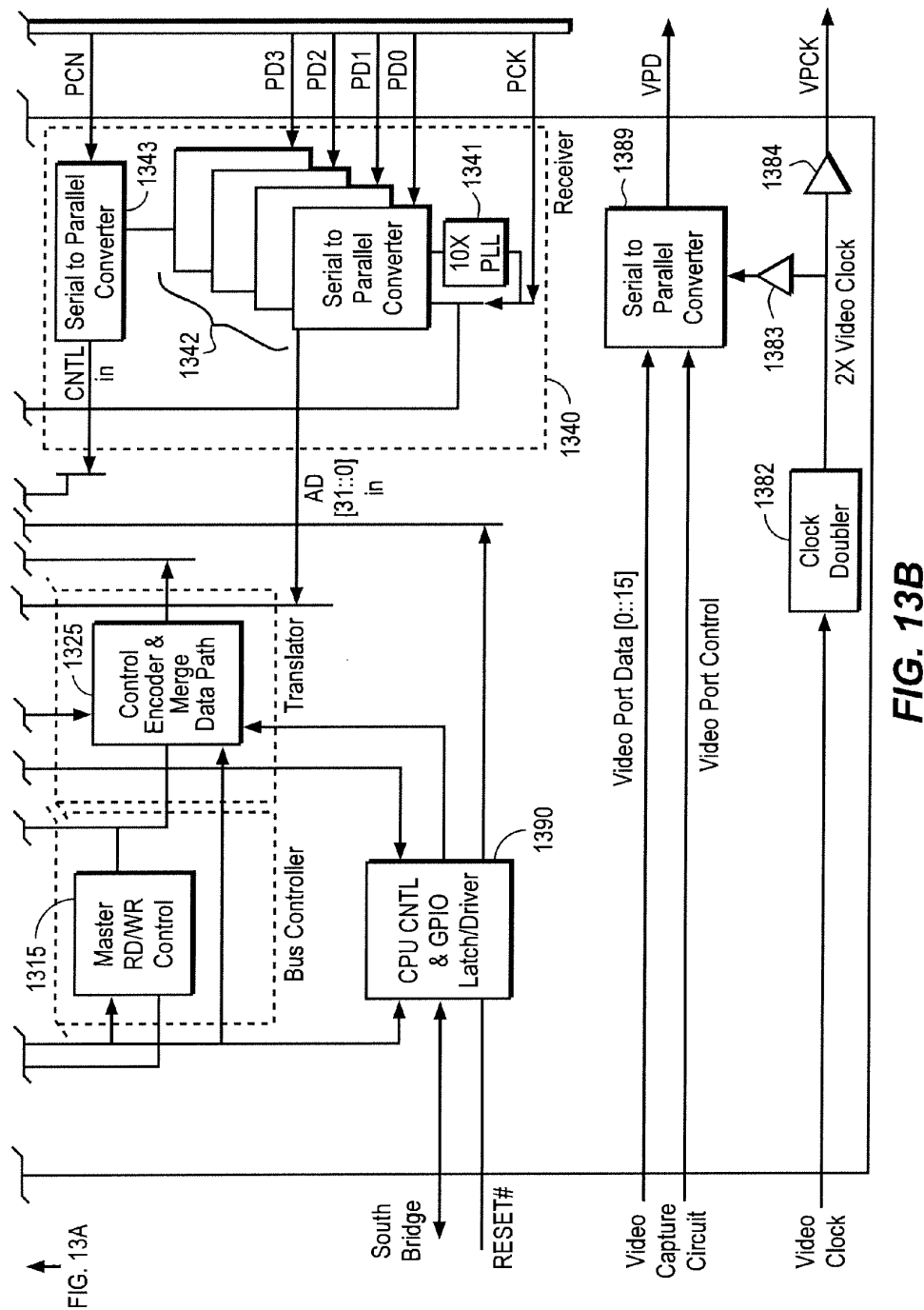


FIG. 13B



**FIG. 13B**

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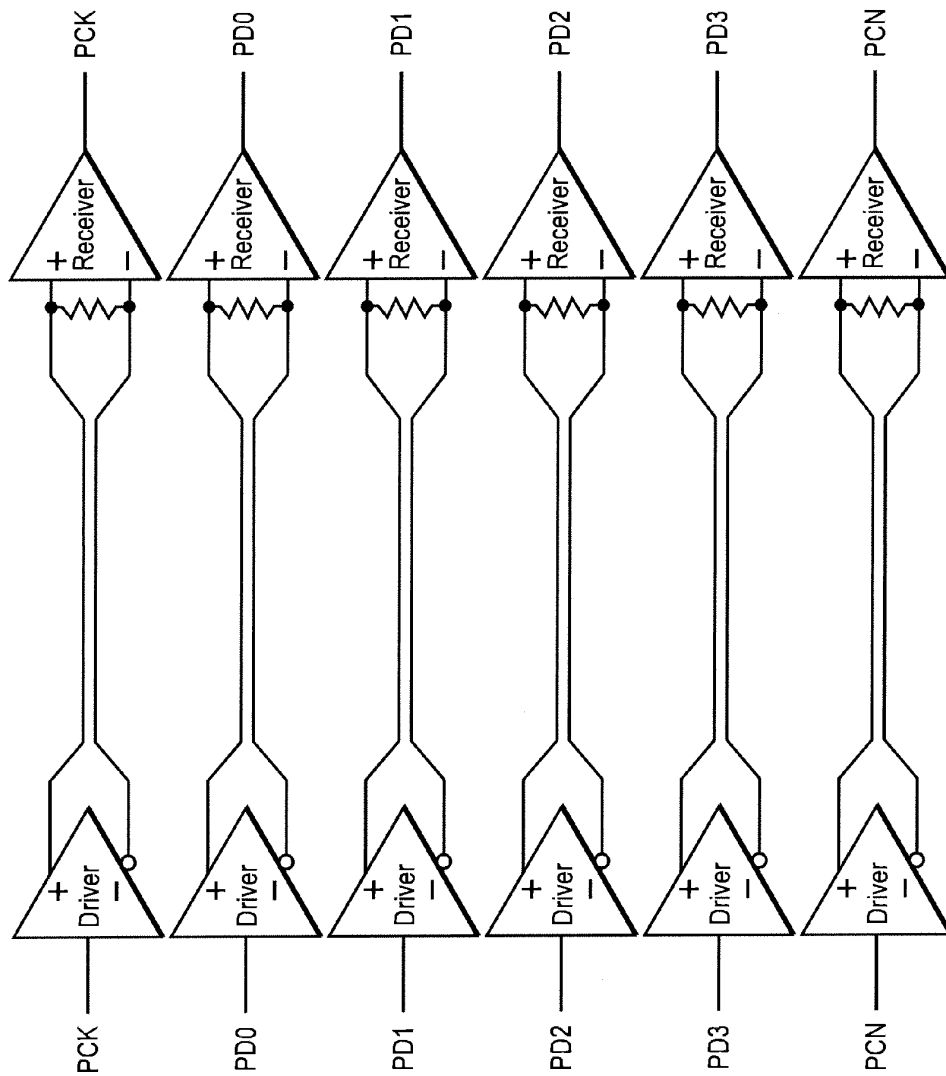


FIG. 14

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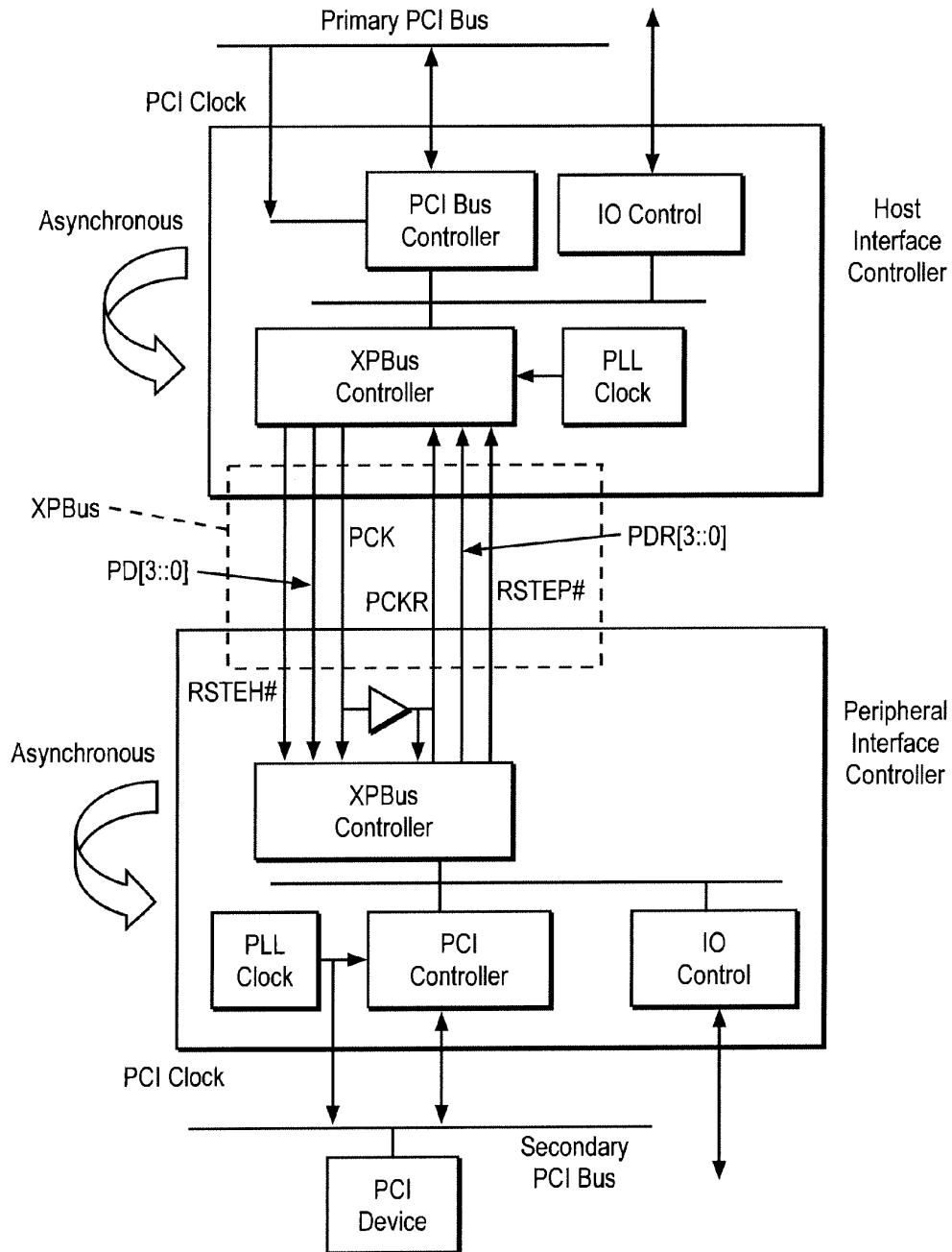


FIG. 15

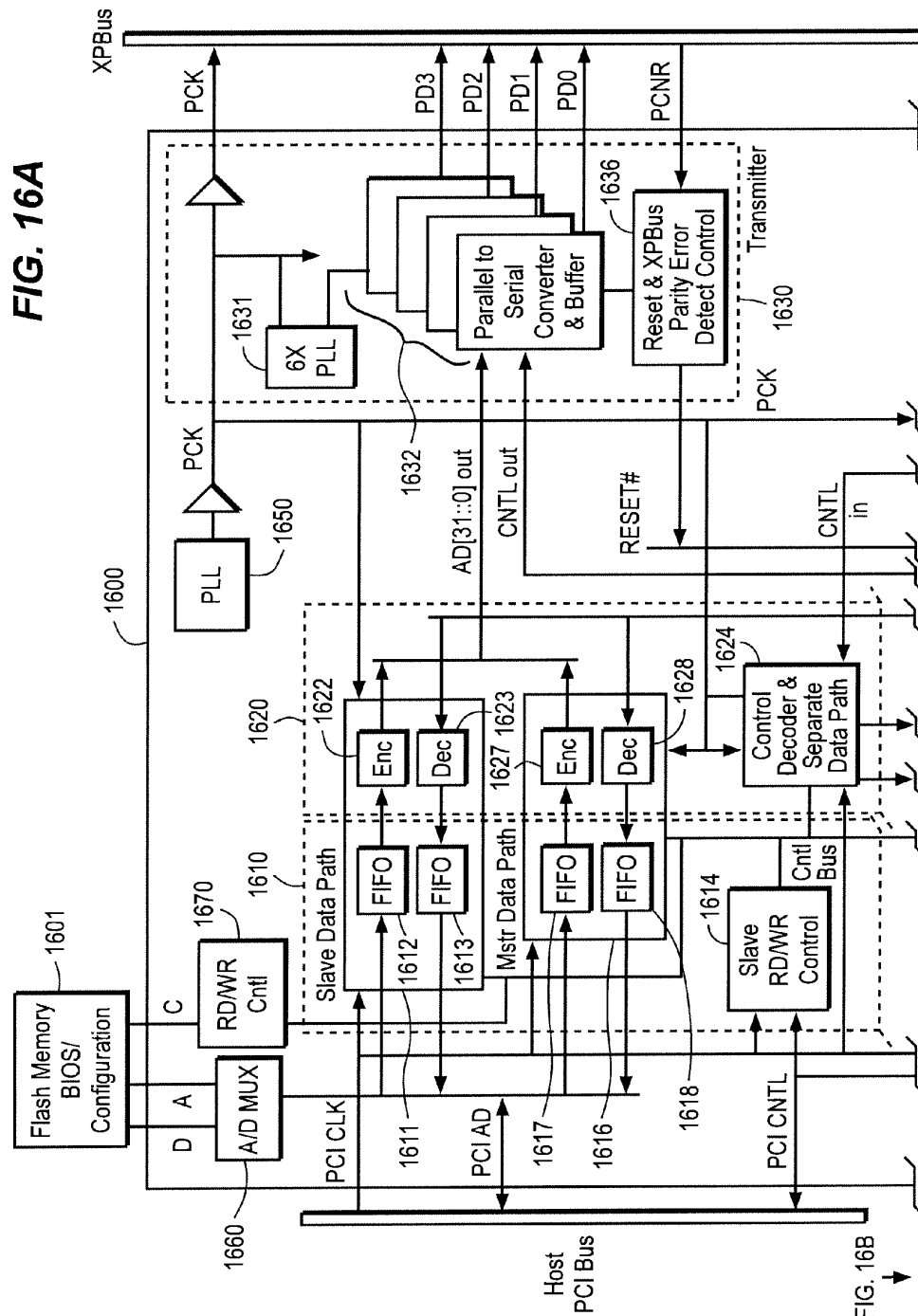


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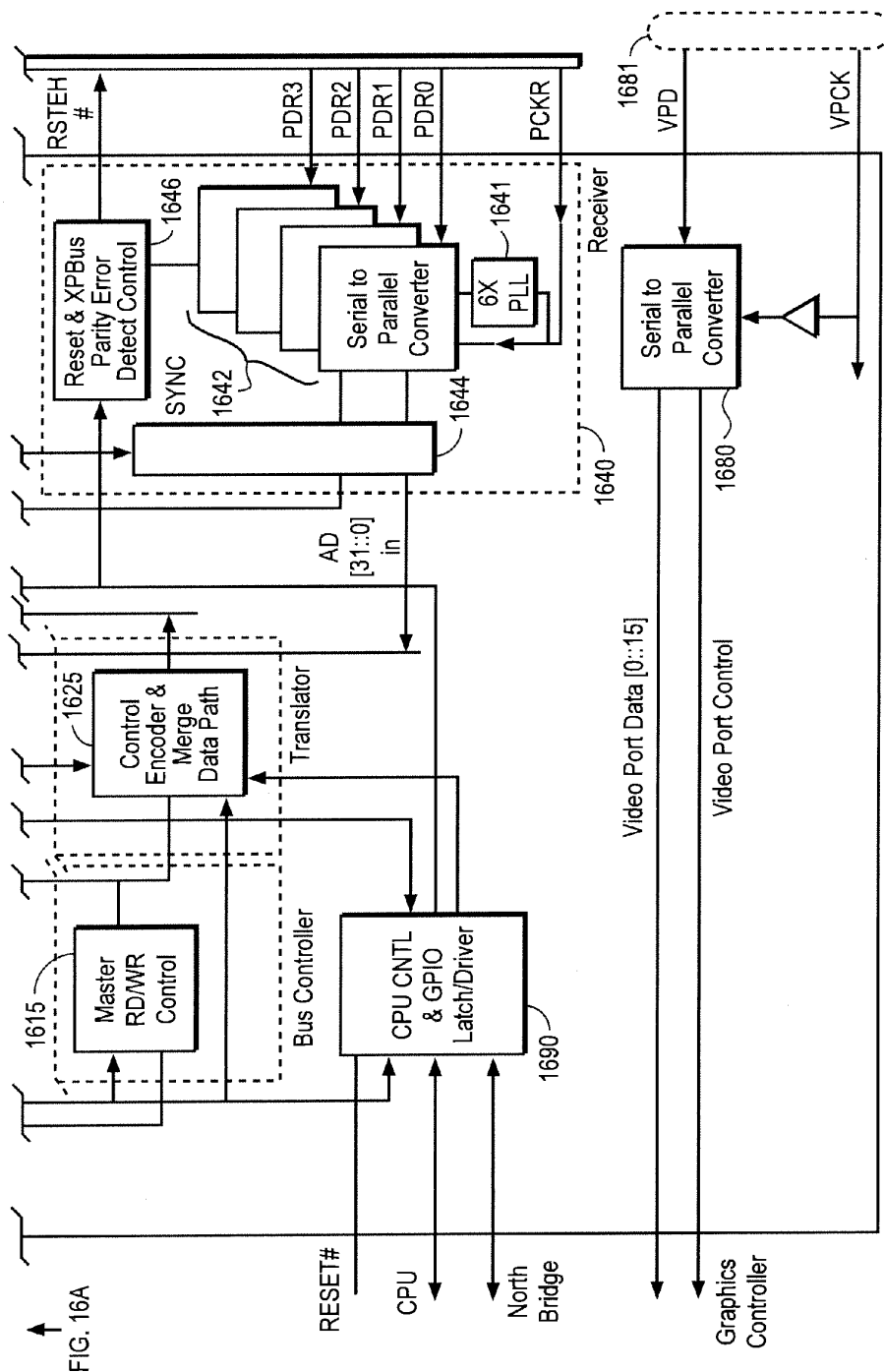


FIG. 16B

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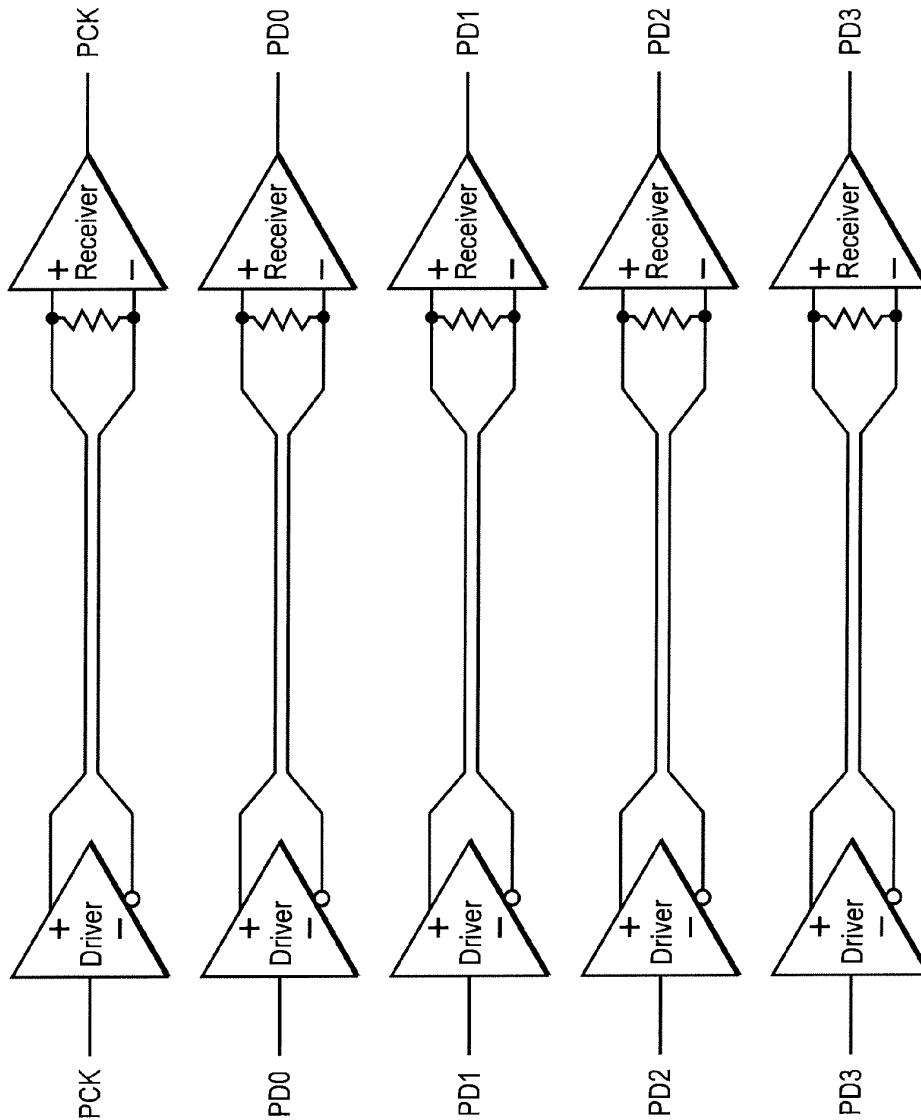


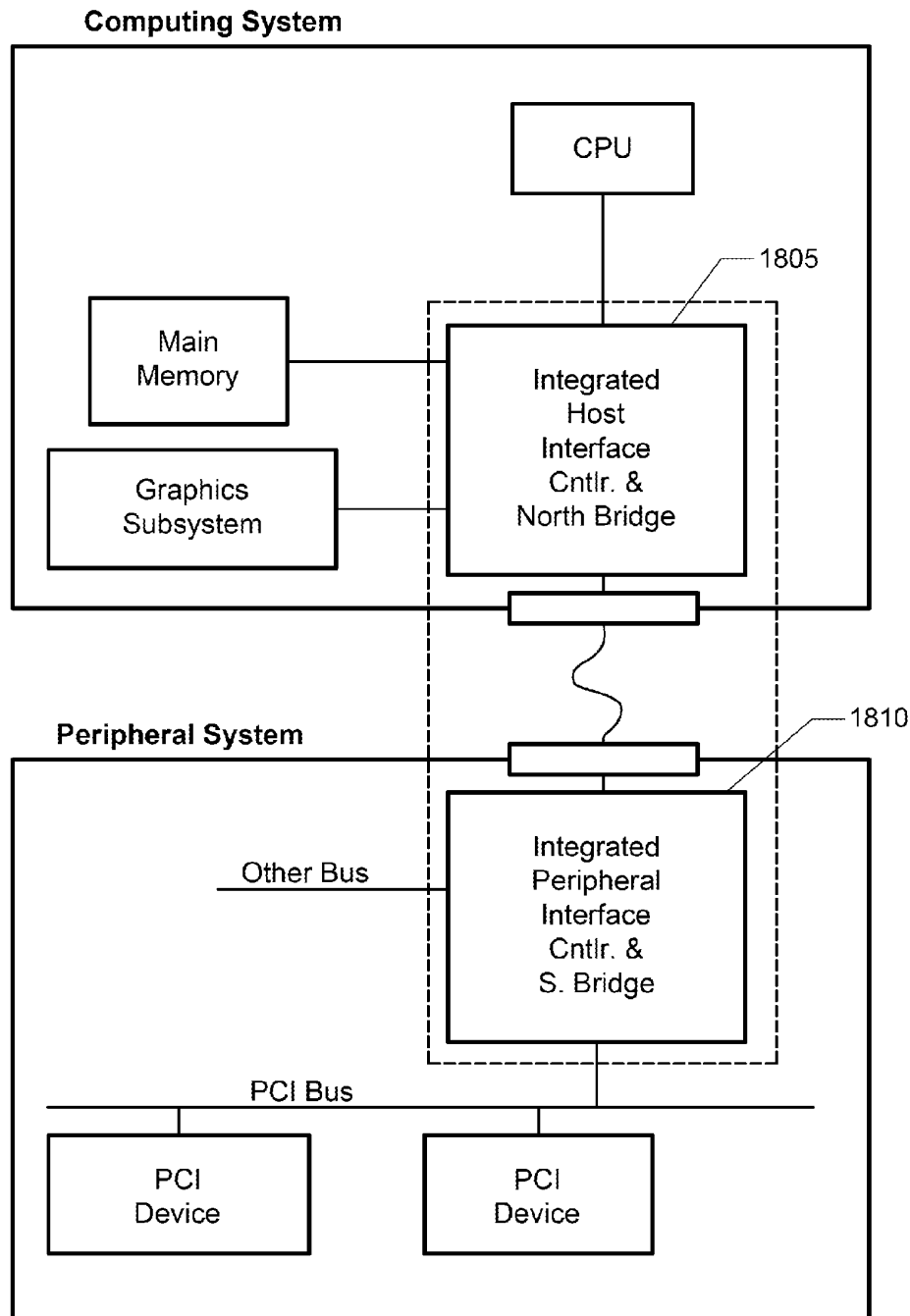
FIG. 17

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**FIGURE 18**

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PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

CROSS REFERENCE TO RELATED  
APPLICATIONS

*Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,321,335. The reissue applications are U.S. application Ser. Nos. 10/963,825 (a parent reissue application), 11/474,256 (which is a continuation reissue of the parent reissue application), 11/517,601 (which is a continuation reissue of the parent reissue application), 12/577,074 (which is a continuation reissue of the parent reissue application), and 12/322,858 (the present application, which is a continuation reissue of U.S. application Ser. No. 11/517,601).*

*This application is a continuation reissue of U.S. application Ser. No. 11/517,601, which is a continuation reissue of U.S. application Ser. No. 10/963,825, which is a reissue of U.S. Pat. No. 6,321,335, which are incorporated herein by reference.*

The following two commonly-owned copending applications, including this one, are being filed concurrently and the other one is hereby incorporated by reference in their entirety for all purposes:

1. U.S. patent application Ser. No. 09/183,816, William W. Y. Chu, entitled, "Modular Computer Security Method and Device", and
2. U.S. patent application Ser. No. 09/183,493, William W. Y. Chu, entitled, "Password Protected Modular Computer Method and Device".

## BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box using password protection techniques. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external

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hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals the are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than pro-

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processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have proprietary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

Thus what is needed are computer systems that provide reduced user investment in redundant computer components and provide a variable level of performance based upon computer configuration.

## SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent "finger print" on the attached computer module.

In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module ("ACM") into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., flat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

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Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified side-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention;

FIG. 5 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention; and

FIGS. 6 and 7 show simplified flow diagrams of security methods according to embodiments of the present invention.

FIG. 8 is a block diagram of one embodiment of a computer system employing the present invention.

FIG. 9 is a block diagram of an attached computing module (ACM).

FIG. 10 is a block diagram of a peripheral console (PCON).

FIG. 11 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 12 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention.

FIG. 13 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 14 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 15 is a block diagram of another embodiment of the HIC and PIC of the present invention and the interface therebetween.

FIG. 16 is a detailed block diagram of another embodiment of the HIC of the present invention.

FIG. 17 is a schematic diagram of the signal lines PCK and PD0 to PD3.

FIG. 18 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

## DESCRIPTION OF SPECIFIC EMBODIMENTS

## I. System Hardware

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alterna-



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tives. The computer system **1** includes an attached computer module (i.e., ACM) **10**, a desktop console **20**, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, work-

In the present embodiment, ACM **10** includes computer components, as will be described below, including a central processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) **40** is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM **10**. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending patent application Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998, commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking system includes at least a key **11**. The key **11** mates with key hole **13** in a lock, which provides a mechanical latch **15** in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the Fig. below.

FIG. **2** is a simplified diagram of a computer module **10** according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous Fig. for easy reading. The computer module **10** includes key **11**, which is insertable into keyhole **13** of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening **14**, which allows the latch to move into and out of the ACM. The ACM also has openings **17** in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. **3** is a simplified side-view diagram of a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. As shown, the ACM module inserts into the computer module bay frame **19**, which is in the console. A side **27** and a bottom **19** of ACM slide and fit firmly into the computer module bay frame, which has at least a bottom portion **19** and back portion **26**. A backside **23** of the ACM faces backside **26** of the frame. ACM also has a front-side or face **25** that houses the lock and exposes the keyhole **13** to a user. The key **11** is insertable from the face into the keyhole.

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As the ACM inserts into the frame, connector **17** couples and inserts into connector **21**. Connector **17** electrically and mechanically interface elements of the ACM to the console through connector **21**. Latch **14** should be moved away from the bottom side **19** of the module bay frame before inserting the ACM into the frame. Once the ACM is inserted fully into the frame, latch **15** is placed in a closed or lock position, where it keeps the ACM firmly in place. That is, latch **15** biases against a backside portion **29** of the ACM enclosure to hold the ACM in place, where the connector **17** firmly engages, electrically and mechanically, with connector **21**. To remove the ACM, latch **15** is moved away or opened from the back side portion of the ACM enclosure. ACM is manually pulled out of the computer module bay frame, where connector **17** disengages with connector **21**. As shown, the key **11** is used to selectively move the latch in the open or locked position to secure the ACM into the frame module.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

FIG. **4** is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module **10**, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module **400**, and a second portion, which includes a hard drive module **420**. A common printed circuit board **437** houses these modules and the like. Among other features, the ACM includes the central processing unit module **400** with a cache memory **405**, which is coupled to a north bridge unit **421**, and a host interface controller **401**. The host interface controller includes a lock control **403**. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors **17**. Here, the CPU module is spatially located near connector **17**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and

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the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller **401** is coupled to BIOS/flash memory **405**. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control **403** to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module **420**. Among other elements, the hard drive module includes north bridge **421**, graphics accelerator **423**, graphics memory **425**, a power controller **427**, an IDE controller **429**, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus **431**, **432**. A power regulator **435** is disposed near the PCI bus.

In a specific embodiment, north bridge unit **421** often couples to a computer memory, to the graphics accelerator **423**, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator **423** typically couples to a graphics memory **425**, and other elements. IDE controller **429** generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **420** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **420** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a

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printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

FIG. **5** is a simplified block diagram **500** of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram **500** has a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram is an attached computer module **500**. The module **500** has a central processing unit, which communicates to a north bridge **541**, by way of a CPU bus **527**. The north bridge couples to main memory **523** via memory bus **529**. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem **515** via bus **542**. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **502** and **531**. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus **537** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **505** with a BIOS. The flash memory device **505** also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller **507** communicates to the north bridge via bus **535** and host PCI bus. The host interface controller also has a lock control **509**, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller **507** communicates to the console using bus **511**, which couples to connection **513**.

In one aspect of the present invention the security system uses a combination of electrical and mechanical locking mechanisms. Referring to FIG. **5A**, for example, the present system provides a lock status mechanism in the host interface controller **509**. The lock status of the lock is determined by checking a lock status bit **549**, which is in the host interface controller. The lock status bit is determined by a signal **553**, which is dependent upon the position of the lock. Here, the position of the lock is closed in the ground **559** position, where the latch couples to a ground plane in the module and/or system. Alternatively, the signal of the lock is at Vcc,

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for example, which is open. Alternatively, the signal can be ground in the open position and Vcc in the closed position, depending upon the application. Other signal schemes can also be used depending upon the application.

Once the status is determined, the host interface controller turns the lock via solenoid **557** in a lock on or lock off position, which is provided through the control bit **551**, for example. The control bit is in a register of the host interface controller in the present example. By way of the signal schemes noted and the control bit, it is possible to place the lock in the lock or unlock position in an electronic manner. Once the status of the lock is determined, the host interface controller can either lock or unlock the latch on the module using a variety of prompts, for example.

In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device **505**. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

In a specific embodiment, the present invention also includes a real-time clock **510** in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz **508** that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source **506** such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like.

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In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

## II. SECURITY DETECTION PROGRAMS

FIGS. **6** and **7** show simplified flow diagrams **600**, **700** of security methods according to embodiments of the present invention. These diagrams are merely illustrations and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Referring to FIG. **6**, which considers an example for when the ACM is inserted into the computer module bay in the console, ACM has already been inserted into the console and is firmly engaged in an electrical and mechanical manner. A computer system is powered up **601**, which provides selected signals to the microprocessor. The microprocessor oversees the operation of the computer system. The microprocessor searches the memory in, for example, the hard disk drive and execute a security program, step **603**.

The security program runs through a sequence of steps before allowing a user to operate the present system with the ACM. Among other processes, the security program determines if an "Auto-lock" is ON. If so, the security program goes via branch **606** to step **607**. Alternatively, the security program goes to step **609**, which determines that the lock stays OFF and loops to step **627**, which indicates that the ACM can be removed physically from the console. In step **607**, the security program turns a switch or switching means that turns ON a lock, which can be electrical, mechanical, or a combination of electrical and mechanical.

In a specific embodiment, the security program turns OFF the power of the ACM and console. Here, the security program directs the OS to turn the power OFF, step **613**. In an embodiment where power failure occurs (step **611**), a key is used to release a latch in the ACM on the lock **615**, where the ACM can be removed, step **627**. From step **613**, the security program determines if the ACM is to be removed, step **617**. If not, the lock stays ON, step **619**. Alternatively, the security detection program determines if the password (or other security code) matches with the designated password, step **621**. If not, the lock stays ON, step **623**. Alternatively, the security program releases the lock **625**, which frees the ACM. Next, the ACM can be removed, step **627**.

In an alternative embodiment, the present invention provides a security system for the ACM, which is outside the console or computer module bay. See, FIG. **7**, for example. As shown, the security system is implemented to prevent illegal or unauthorized use (step **701**) of the ACM, which has not been used in the console. Here, a key turns ON a lock (step **703**). The lock moves a latch in the ACM to a specific spatial location that physically blocks the passage of the ACM into the computer module bay. Accordingly, the ACM cannot insert (step **705**) into the computer module bay.

In an alternative aspect, the key can be used to turn the lock OFF, step **707**. Here, the key moves the latch in a selected spatial location that allows the ACM to be inserted into the computer bay module. In the OFF position, the ACM inserts into the computer module bay, step **709**. Once the ACM is in the bay, a user can begin operating the ACM through the console. In one embodiment, the computer console including the ACM goes through the sequence of steps in the above FIG., but is not limited.

In a specific embodiment, the present invention implements the sequences above using computer software. In other aspects, computer hardware can also be used and is preferably in some applications. The computer hardware can include a mechanical lock, which is built into the ACM. An example of



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such mechanical lock is shown above, but can also be others. In other aspects, the lock can be controlled or accessed electronically by way of computer software. Here, the key can be used to as a manual override if the ACM or computer fails.

The lock is used to prevent theft and accidental removal inside CMB. The current invention locates the lock inside the ACM to allow a user to keep a single key as ACM is moved from console to console at different locations. When ACM is in transit, the lock can be engaged using the key so that the latch extends outside ACM's enclosure. The extended latch prevents ACM from being inserted into any CMB. This prevents any illegal use of ACM by someone other than the user.

In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

FIG. 8 is a block diagram of the components in one computer system employing the present invention. The computer system comprises an attached computer module (ACM), a peripheral console (PCON), and the interconnection apparatus between them. The ACM includes the central processing unit (CPU) 810, system memory 820, high performance devices 850, primary mass storage 830, and related interface and support circuitry 840. The PCON includes primary display 910, primary input 920, secondary mass storage 950, other devices 960, expansion slots 970, the primary power supply 930, and related interface and support circuitry 940. The interconnection apparatus 1000 includes circuitry to convey power and operational signals between the ACM and PCON.

Within the ACM 800, the CPU 810 executes instructions and manipulates data stored in the system memory. The CPU 810 and system memory 820 represent the user's core computing power. The core computing power may also include high performance devices 850 such as advanced graphics

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processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU. The primary mass storage 830 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device represent the user's computing environment. Interface and support circuitry 840 primarily includes interface chips and signal buses that interconnect the CPU, system memory, high performance devices, and primary mass storage. The interface and support circuitry also connects ACM-resident components with the ACM-to-PCON interconnection apparatus as needed.

Within the PCON 900, the primary display component 910 may include an integrated display device or connection circuitry for an external display device. This primary display device may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU can communicate toward the user.

The primary input component 920 of the PCON may include an integrated input device or connection circuitry for attachment to an external input device. The primary input may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component is the paramount vehicle by which programs executing on the CPU receive signals from the user.

The PCON may contain secondary mass storage 950 to provide additional high capacity storage for data and software. Secondary mass storage may have fixed or removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

The PCON may be enhanced with additional capability through the use of integrated "Other Devices" 960 or add-on cards inserted into the PCON's expansion slots 970. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 940 primarily includes interface chips, driver chips, and signal buses that interconnect the other components within the PCON. The interface and support circuitry also connects PCON-resident components with the ACM-to-PCON interconnection apparatus as needed.

Importantly, the PCON houses the primary power supply 930. The primary power supply has sufficient capacity to power both the PCON and the ACM 800 for normal operation. Note that the ACM may include a secondary "power supply" in the form, for example, of a small battery. Such a power supply would be included in the ACM to maintain, for example, a time-of-day clock, configuration settings when the ACM is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU at its rated speed, along with the memory and primary mass storage, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

FIG. 9 is a block diagram of an attached computing module (ACM) 800. The physical ACM package 800 contains the ACM functional components 801 and the ACM side of the ACM-to-PCON Interconnection 1000. The ACM 801 comprises a CPU component 810, a system memory component

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820, a primary mass storage component 830, a high performance devices components 850, and an interface and support component 840.

The ACM side of the ACM-to-PCON Interconnection 1000 comprises a Host Interface Controller (HIC) component 1020 and an ACM connector component 1030. The HIC 1020 and connector 1030 components couple the ACM functional components 800 with the signals of an ACM-to-PCON interface bus 1010 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1010 comprises conveyance for electrical power 1014 and signals for a peripheral bus 1012, video 1016, video port 1017, and console type 1018. The preferred ACM-to-PCON Interconnection 1000 is described in detail in a companion U.S. patent application Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," by the same inventor, filed on the same day herewith, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1000 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1000. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

The CPU component 810 of the ACM functional circuitry 801 of the presently described embodiment comprises a microprocessor 812, which is the chief component of the personal computer system, power supply connection point 813, and cache memory 814 tightly coupled to the microprocessor 812 by the CPU-to-cache bus 874 comprising signal paths for address, data, and control information. The microprocessor 812 of this embodiment is one of the models from the Pentium II family of processors from Intel Corporation. Microprocessor 812 receives electrical power from power bus 168 via connection point 813. Microprocessor 812 couples to the Host Interface Controller (HIC) 320 via CPU-to-HIC bus 863 comprising signal paths to exchange control information such as an interrupt request. Microprocessor 812 also couples to CPU Bridge 846 via CPU main bus 864 comprising signal paths for address, data, and control information.

The CPU Bridge component 846 of the interface and support circuitry 840 operates to couple the high speed CPU main bus 864 to specialty buses of varying speeds and capability that connect other computer components. The CPU Bridge of the presently described embodiment incorporates memory controller circuitry, advanced graphics processor support circuitry, and a general, industry-standard PCI bus controller in a single package. A CPU Bridge 146 such as the 82443LX PCI/AGP Controller from Intel Corporation may be used.

The system memory component 820 of the ACM functional circuitry 801 in the present embodiment comprises main system memory (RAM) 822, BIOS memory 824, and flash memory 826. The system memory 820 is used to contain data and instructions that are directly addressable by the CPU. The RAM 822 comprises volatile memory devices such as DRAM or SDRAM memory chips that do not retain their stored contents when power is removed. This form of memory represents the largest proportion of total system memory 820 capacity. The BIOS memory 824 comprises non-volatile memory devices such as ROM or EPROM memory chips that retain their stored contents regardless of the application of power and are read-only memory under normal operating

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conditions. The BIOS memory 824 stores, for example, start-up instructions for the microprocessor 812 and sets of instructions for rudimentary input/output tasks. The flash memory 826 comprises non-volatile memory devices that retain their stored contents regardless of the application of power. Unlike the BIOS non-volatile memory, however, the stored contents of the flash memory 826 are easily changed under normal operating conditions. The flash memory 826 may be used to store status and configuration data, such as security identifiers or ACM specifications like the speed of the microprocessor 812. Some embodiments may combine the BIOS functions into the flash memory device, thus permitting BIOS contents to be rewritten, improving field upgradability.

The main system memory (RAM) 822 is coupled to memory controller circuitry resident within the CPU Bridge 846 via direct memory bus 865. The BIOS 824 and flash memory 826 are coupled to HIC 1020 via switched memory bus 866. This permits the BIOS 824 and flash 826 memories to be accessed by circuitry in the HIC 1020 or other circuitry connected thereto. The direct memory bus 865 and the switch memory bus 866 each comprises conductors to convey signals for data, address, and control information.

The primary mass storage component 830 of the ACM functional circuitry 801 in the present embodiment comprises a compact hard disk drive with an industry-standard, IDE interface. The hard disk drive (HDD) 832 has a formatted storage capacity sufficient to contain an operating system for the computer, application software desired by the user, and related user configuration and operating parameter data. The HDD 832 in the present embodiment serves as the "boot" device for the personal computer from which the operating system is loaded into RAM 122 by the start-up program stored in the BIOS 824.

The present HDD 832 has a capacity of approximately 2,000 megabytes to provide adequate storage for common software configurations and reasonable space for user data. One example of a common software configuration includes the Windows 95 operating system from Microsoft Corporation, a word processing program, a spreadsheet program, a presentation graphics program, a database program, an email program, and a web browser such as Navigator from Netscape Corporation. The hard disk 832 stores program and data files for each software component, including files distributed by the vendor as well as files created or updated by operation of the software after it is installed. For example, a word processor program may maintain information about a user's identity and latest preferences in an operating system registry file. Or, for example, the web browser may maintain a file of the user's favorite web sites or most recently viewed web pages. An HDD with 2000 megabyte capacity is readily available in the small size of hard disk (e.g., 2.5-inch or 3.5-inch) to minimize the space required within the ACM for the primary mass storage device 130.

The HDD 832 is coupled to IDE controller circuitry 848 via IDE bus 872. The IDE controller circuitry 848 is coupled to the CPU Bridge 846 via the Host PCI bus 867. IDE controllers and busses, and the PCI bus are well known and understood in the industry. The above components operate together to couple the hard disk drive 832 to the microprocessor 812.

The high performance devices component 850 of the ACM functional circuitry 801 in the present embodiment comprises an Advanced Graphics Processor (AGP) 852. The Model 740 Graphics Device from Intel Corporation may be used in the present embodiment as the AGP.

Increases in computer screen size, graphics resolution, color depth, and visual motion frame rates, used by operating

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system and application software alike, have increased the computing power required to generate and maintain computer screen displays. An AGP removes a substantial portion of the graphics computing burden from the CPU to the specialized high-performance processor, but a high level of interaction between the CPU and the specialized processor is nonetheless required. To maximize the effective contribution of having a specialized processor in the presently described embodiment, the AGP 852 is located in the ACM 800, where it is in close proximity to the microprocessor 812. The AGP 852 is coupled to the microprocessor 812 via the advanced graphics port bus 873 of the CPU Bridge 846. The visual display signal generated by the AGP are conveyed toward actual display devices at the peripheral console (PCON) via video signal bus 870. Video information from a source external to the ACM and appearing as video port signals 1017 may be conveyed to the AGP 852 via video port signal path 871.

Other types of high performance components may be included in different ACM configurations. For example, an interface to an extremely high speed data communication facility may be desirable in some future computer where CPU-to-network interaction is of comparable intensity to today's CPU-to-graphics interaction. Because such high performance components tend to be high in cost, their inclusion in the ACM is desirable. Inclusion of high cost, high performance components in the ACM concentrates a user's core computing power and environment in a portable package. This represents a further advantage of the invention.

The interface and support component 840 of the ACM functional circuitry 801 in the present embodiment comprises circuitry for power regulation 842, clocking 844, CPU Bridge 846, IDE controller 848, and signal conveyance paths 861-874. The CPU Bridge 846 couples the CPU component 810 of the ACM 800 with the other components of the ACM 820-850 and the CPU-to-PCON Interconnection 1000. The CPU Bridge 846 and IDE controller 848 have already been discussed. Power regulation circuitry 842 receives electrical power via the electrical power conduction path 1014 of the CPU-to-PCON Interconnection 1000, conditions and distributes it to the other circuitry in the ACM using power distribution bus 868. Such regulation and distribution is well known and understood in the art.

Clocking circuitry 844 generates clock signals for distribution to other components within the ACM 800 that require a timing and synchronization clock source. The CPU 810 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 800 includes circuitry that can vary the frequency of the main CPU clock signal conveyed to the CPU via signal path 862, in response to a signal received from the host interface controller (HIC) 1020 via signal path 861. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU (and thus the entire ACM) can be varied.

The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1020 of the presently described embodiment adjusts the frequency control signal sent via signal path 861 to the clocking circuitry 844, based on the "console type" information signal 1018 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1000. In this arrangement, the console type signal originating from a desktop PCON would result in the generation of a maximum speed CPU clock. The desktop PCON, presumably has unlimited power from an electrical wall outlet and does not need to sacrifice

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speed for power conservation. The console type signal originating from a notebook PCON would, however, result in the generation of a CPU clock speed reduced from the maximum in order to conserve battery power and extend the duration of computer operation obtained from the energy stored in the battery. The console type signal originating from a notepad PCON would result in the generation of a CPU clock speed reduced further yet, the notepad PCON presumably having smaller batteries than the notebook PCON. Inclusion of control signals and circuitry to effect a CPU clock signal varying in frequency according to characteristics of the PCON to which the ACM is connected facilitates the movement of the user's core computing power and environment to different work settings, which is a further advantage of the present invention.

FIG. 10 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 900 contains the PCON functional components 901 and the PCON side of the ACM-to-PCON Interconnection 1000. The PCON functional components 901 comprise primary display 910, a primary input 920, a primary power supply 930, interface and support 940, secondary mass storage 950, other devices 960, and expansion slots 970.

The PCON side of the ACM-to-PCON Interconnection 1000 comprises a Peripheral Interface Controller (PIC) component 1040, a PCON connector component 1050, console-type component 1042, and flash memory device 1048. The PIC 1040 and connector 1050 components couple the PCON functional components 901 with the signals of an ACM-to-PCON interface bus 1010 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1010 comprises conveyance for electrical power 1014 and signals for a peripheral bus 1012, video 1016, video port 1017, and console-type 1018. The preferred ACM-to-PCON Interconnection 1000 is described in detail in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference.

Connector component 1050 may be selected to mate directly with the connector component 1030 of an ACM (shown in FIG. 9). Alternatively, connector component 1050 may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

Flash memory device 1048 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller to which it is connected. As such, flash memory 1048 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

The primary display component 910 of the PCON functional circuitry 901 of the presently described embodiment comprises integrated display panel 912 and video connector 913. Integrated display panel 912 is a color LCD display panel having a resolution of 640 horizontal by 480 vertical pixels. 640-by-480 resolution is popularly considered to be the minimum screen size to make practical use of the application software in widespread use today. One skilled in the art



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recognizes that the type and resolution of the display can vary greatly from embodiment to embodiment, depending on factors such as cost and intended application. Any display device may be used, without departing from the scope and spirit of the invention, that provides principal visual output to the computer user for operating system and application software executing in its customary and intended fashion using the CPU component (810 of FIG. 8) of an ACM presently coupled to PCON 900.

Integrated display panel 912 is coupled to video signal bus 949 and displays a screen image in response to video signals presented on bus 949. Certain pins of connector 1050 receive video output signals 1016 of the ACM-to-PCON interface bus 1010 from a mated connector that is coupled to an ACM. These certain pins of connector 1050 couple to video signal bus 949 which conveys the video output signals 1016 throughout the PCON 900 as needed. Video connector 913 is exposed at the exterior of PCON 900 and couples to video signal bus 949. Connector 913 permits easy attachment of an external display device that is compatible with the signals carried by bus 949, such as a CRT monitor (not shown). The external display device may be used in addition, or as an alternative, to integrated display panel 912.

The isolation of the relatively heavy and sizable primary display 910 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

The primary input component 920 of the PCON functional circuitry 901 of the presently described embodiment comprises keyboard interface circuitry 922, keyboard connector 923, pointer interface circuitry 924, and pointer connector 925. Keyboard interface circuitry 922 and pointer interface circuitry 924 connect to ISA bus 945 and are thereby coupled to the CPU component (810 of FIG. 8) of any ACM attached to PCON 900. Keyboard interface circuitry 922 interfaces a standard computer keyboard (not shown), attached at connector 923, to ISA bus 945. Pointer interface circuitry 922 interfaces a standard computer pointing device (not shown), such as a computer mouse attached at connector 925, to ISA bus 945. Computer keyboards, pointing devices, connectors 923, 925, keyboard interface circuitry 922, and pointer interface circuitry 924 are well known in the art. The isolation of the relatively heavy and sizable primary input devices 920 from the core computing power and user environment contained within an ACM represents a further advantage of the present invention.

The primary power supply component 930 of the PCON functional circuitry 901 of the presently described embodiment provides electrical energy for the sustained, normal operation of the PCON 900 and any ACM coupled to connector 1050. The power supply may be of the switching variety well known in the art that receives electrical energy from an AC source 989, such as a wall outlet. Power supply 930 reduces the alternating current input voltage, to a number of distinct outputs of differing voltages and current capacities. The outputs of power supply 930 are applied to power bus 931. Power bus 931 distributes the power supply outputs to the other circuitry within the PCON 900. Bus 931 also connects to certain pins of connector 1050 to provide the electrical power 1014 for an ACM conveyed by ACM-to-PCON interconnection 1000. The isolation of the usually heavy power supply 930 from the core computing power and user environment contained within the ACM represents a further advantage of the present invention.

The interface and support component 940 of the PCON functional circuitry 901 of the presently described embodiment comprises peripheral bridge 246, diskette controller

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242, IDE controller 948, and signal conveyance paths 941, 943, 944, 945, 947 and 949. Peripheral bridge 946 couples PCI peripheral bus 941 with peripheral busses of other formats such as ISA peripheral bus 945 and others 947. PCI and ISA peripheral busses are industry standards, well known and understood in the art. Other peripheral busses 947 may include, for example, a bus compliant with the universal serial bus (USB) industry standard. While other embodiments of a peripheral console 900 may include a single peripheral bus that is coupled to an attached ACM via ACM-to-PCON interconnection 1000, such as PCI bus 941, this embodiment includes peripheral bridge 946 to establish additional busses 945, 947. The additional busses 945, 947 permit the use of the many low-cost and readily available components compatible with these bus specifications.

Diskette controller 942 interfaces a floppy disk drive 954 with the CPU component 810 of an attached ACM (shown in FIG. 9) so that the CPU may control and use the diskette drive 954 hardware to store and retrieve data. Diskette controller 942 couples to the CPU via a connection to ISA bus 945. Diskette controller 942 connects to the diskette drive 954 via one of device cables 943.

Similarly, IDE controller 948 interfaces a hard disk drive 952 and a CDROM drive 956 with the CPU component 810 of an attached ACM (shown in FIG. 9) so that the CPU may control and use the hard disk drive 952 and CDROM 956 hardware to store and retrieve data. IDE controller 948 couples to the CPU via connection to PCI peripheral bus 941. IDE controller 948 connects to each of hard disk drive 952 and CD-ROM drive 956 via one of device cables 943. Some embodiments of PCON 900 may take advantage of VLSI integrated circuits such as an 82371SB (PIIX4) integrated circuit from Intel Corporation. An 82371SB integrated circuit includes circuitry for both the peripheral bridge 946 and the IDE controller 948 in a single package.

The secondary mass storage component 950 of the PCON functional circuitry 901 of the presently described embodiment comprises diskette drive 954, hard disk drive 952, and CD-ROM drive 956. Secondary mass storage 950 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 950 are not part of a computer user's core computing power and environment. Secondary mass storage 950 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 900, or archival copies of data files that are maintained in primary mass storage 850 of an ACM (shown in FIG. 9). Storage capacities for secondary mass storage 950 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 954, to more than 10 gigabytes for a large format (5-inch) hard disk drive 952. Hard disk drive 952 employs fixed recording media, while diskette drive 954 and CD-ROM drive 956 employ removable media. Diskette drive 954 and hard disk drive 952 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 956 supports only read operations.

The other devices component 960 of the PCON functional circuitry 901 of the presently described embodiment comprises a video capture card. A video capture card accepts analog television signals, such as those complying with the NTSC standard used for television broadcast in the United States, and digitizes picture frames represented by the analog signal for processing by the computer. Video capture cards at present are considered a specialty, i.e., not ubiquitous, component of personal computer systems. Digitized picture infor-

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mation from video capture card 960 is carried via signal conveyance path 944 to the peripheral interface controller 1040 which transforms it to the video port signals 1017 of the ACM-to-PCON interconnection 1000 for coupling to the advanced graphics processor 852 in an attached ACM (shown in FIG. 9).

Video capture card 960 is merely representative of the many types of "other" devices that may be installed in a PCON to expand the capabilities of the personal computer. Sound cards and laboratory data acquisition cards are other examples. Video capture card 960 is shown installed in one of expansion slots 970 for coupling to the interface and control circuitry 940 of the PCON. Any of other devices 960 could be coupled to the interface and control circuitry 940 of the PCON by different means, such as direct installation on the circuit board that includes the interface and control circuitry 940; e.g., a motherboard.

The expansion slots component 970 of the PCON functional circuitry 901 of the presently described embodiment comprises PCI connectors 971 and ISA connectors 972. A circuit card may be inserted into one of the connectors 971, 972 in order to be operatively coupled with the CPU 1010 of an attached ACM (shown in FIG. 9). Each of connectors 971 electrically connects to PCI bus 941, and may receive and hold a printed circuit card which it electrically couples to PCI bus 941. Each of connectors 972 electrically connects to ISA bus 945, and may receive and hold a printed circuit card which it electrically couples to ISA bus 945. The PCI 941 and ISA 945 busses couple to the CPU 1010 of an attached ACM (shown in FIG. 9) by circuitry already described.

Embodiments in accordance with the present invention may interface two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In accordance with embodiments of the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface

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channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

FIG. 11 is a block diagram of one embodiment of a computer system 1100 using the interface of the present invention. Computer system 1100 includes an attached computer module (ACM) 1105 and a peripheral console 1110. The ACM 1105 and the peripheral console 1110 are interfaced through an exchange interface system (XIS) bus 1115. The XIS bus 1115 includes power bus 1116, video bus 1117 and peripheral bus (XPBus) 1118, which is also herein referred to as an interface channel. The power bus 1116 transmits power between ACM 1105 and peripheral console 1110. In a preferred embodiment power bus 1116 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 1117 transmits video signals between the ACM 1105 and the peripheral console 1110. In a preferred embodiment, the video bus 1117 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 1118 is coupled to host interface controller (HIC) 1119 and to peripheral interface controller (PIC) 1120, which is also sometimes referred to as a bay interface controller.

FIG. 12 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention. As shown in FIG. 12, HIC 1200 comprises bus controller 1210, translator 1220, transmitter 1230, receiver 1240, a PLL 1250, an address/data multiplexer (A/D MUX) 1260, a read/write controller (RD/WR Cntl) 1270, a video serial to parallel converter 1280 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1290.

HIC 1200 is coupled to an optional flash memory BIOS configuration unit 1201. Flash memory unit 1201 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1260 and RD/WR Control 1270, which control the programming, read, and write of flash memory unit 1201.

Bus controller 1210 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1210 includes a slave (target) unit 1211 and a master unit 1216. Both slave unit 1211 and master unit 1216 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1216 as well as the two FIFOs in the slave unit 1211 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1211 includes encoder 1222 and decoder 1223, while master unit 1216 includes encoder 1227 and decoder 1228. The FIFOs 1212, 1213, 1217 and 1218 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 12 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1212 and 1217 before they are encoded by encoders 1222 and 1223. Encoders 1222 and 1223 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1223 and 1228 to a form more suitable for transmission on the host PCI bus. Thereaf-

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ter the decoded data and address information is passed through FIFOs 1213 and 1218 prior to being transferred to the host PCI bus. FIFOs 1212, 1213, 1217 and 1218, allow bus controller 1210 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller 1210 also comprises slave read/write control (RD/WR Cntl) 1214 and master read/write control (RD/WR Cntl) 1215. RD/WR controls 1214 and 1215 are involved in the transfer of PCI control signals between bus controller 1210 and the host PCI bus.

Bus controller 1210 is coupled to translator 1220. Translator 1220 comprises encoders 1222 and 1227, decoders 1223 and 1228, control decoder & separate data path unit 1224 and control encoder & merge data path unit 1225. As discussed above encoders 1222 and 1227 are part of slave data unit 1211 and master data unit 1216, respectively, receive PCI address and data information from FIFOs 1212 and 1217, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1223 and 1228 are part of slave data unit 1211 and master data unit 1216, respectively, and format address and data information from receiver 1240 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1225 receives PCI control signals from the slave RD/WR control 1214 and master RD/WR control 1215. Additionally, control encoder & merge data path unit 1225 receives control signals from CPU CNTL & GPIO latch/driver 1290, which is coupled to the CPU and north bridge (not shown in FIG. 12). Control encoder & merge data path unit 1225 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1230, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1224 receives control bits from receiver 1240 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1224 separates the control bits it receives from receiver 1240 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

Transmitter 1230 receives multiplexed parallel address/data (A/D) bits and control bits from translator 1220 on the AD[31:0] out and the CNTL out lines, respectively. Transmitter 1230 also receives a clock signal from PLL 1250. PLL 1250 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 66 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 66 MHz rather than 33 MHz or having 64 rather than 32 multiplexed address/data lines.

The multiplexed parallel A/D bits and some control bits input to transmitter 1230 are serialized by parallel to serial converters 1232 of transmitter 1230 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the

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XPBus. Other control bits are serialized by parallel to serial converter 1233 into 10 bit packets and send out on control line PCN of the XPBus.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 14, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment of FIG. 14, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

FIG. 13 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1300 is nearly identical to HIC 1200 in its function, except that HIC 1200 interfaces the host PCI bus to the XPBus while PIC 1300 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1300 serve the same function as their corresponding components in HIC 1200. Reference numbers for components in PIC 1300 have been selected such that a component in PIC 1300 and its corresponding component in HIC 1200 have reference numbers that differ by 100 and have the same two least significant digits. Thus for example, the bus controller in PIC 1300 is referenced as bus controller 1310 while the bus controller in HIC 1200 is referenced as bus controller 1210. As many of the elements in PIC 1300 serve the same functions as those served by their corresponding elements in HIC 1200 and as the functions of the corresponding elements in HIC 1200 have been described in detail above, the function of elements of PIC 1300 having corresponding elements in HIC 1200 will not be further described herein. Reference may be made to the above description of FIG. 12 for an understand-



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ing of the functions of the elements of PIC 1300 having corresponding elements in HIC 1200.

As suggested above, there are also differences between HIC 1200 and PIC 1300. Some of the differences between HIC 1200 and PIC 1300 include the following. First, receiver 1340 in PIC 1300, unlike receiver 1240 in HIC 1200, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 1200 synchronizes the PCKR clock to the PCK clock locally generated by PLL 1250. PIC 1300 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 1200. Another difference between PIC 1300 and HIC 1200 is the fact that PIC 1300 contains a video parallel to serial converter 1389 whereas HIC 1200 contains a video serial to parallel converter 1280. Video parallel to serial converter 1389 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0::15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. 11) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1300, unlike HIC 1200, contains a clock doubler 1382 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1382 through buffer 1383 and is sent to serial to parallel converter 1280 through buffer 1384. Additionally, reset control unit 1335 in PIC 1300 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 13190 and transmits the reset signal on the RESET# line to the HIC 1200 whereas reset control unit 1245 of HIC 600 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 1290 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1300 to the HIC 1200.

Like HIC 1200, PIC 1300 handles the PCI bus control signals and control bits from the XPBus representing PCI control signals in the following ways:

1. PIC 1300 buffers clocked control signals from the secondary PCI bus, encodes them and sends the encoded control bits to the XPBus;
2. PIC 1300 manages the signal locally; and
3. PIC 1300 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

PIC 1300 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

FIG. 14 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits from the HIC to the PIC. The

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bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to the HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 14, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 14 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

FIG. 15 is a block diagram of another embodiment of the HIC and PIC of the present invention and the interface therebetween. One important difference between the XPBuses shown in FIGS. 12 and 15 is the fact that unlike the XPBus of FIG. 12, the XPBus of FIG. 15 does not have control lines PCN and PCNR. Another difference lies in the fact that the XPBus of FIG. 15 has two dedicated reset lines RSTEH# and RSTEP# instead of only one as is the case for the XPBus of FIG. 12. RSTEH# and RSTEP# are unidirectional reset and error condition signal lines that transmit a reset and error condition signal from the host PCI to the peripheral PCI and from the peripheral PCI to host PCI, respectively.

In one embodiment, each of reset lines RSTEH#, RSTEP#, and RESET# (shown in FIG. 12), is preferably a non-differential signal line consisting of one physical line. In other embodiments, one or more of the above lines may be a differential signal line having more than one physical line.

FIG. 16 shows a detailed block diagrams of the HIC shown in FIG. 15. HIC 1600 shown in FIG. 16 is, other than for a few difference, identical to HIC 1200 shown in FIG. 12. Accordingly, reference numbers for components in HIC 1600 have been selected such that a component in HIC 1600 and its corresponding component in HIC 1200 have reference numbers that differ by 400 and have the same two least significant digits. One of the differences between HIC 1600 and HIC 1200 is the fact that, unlike HIC 1200, HIC 1600 does not have a parallel to serial converter or a serial to parallel converter dedicated exclusively to CNTL out and CNTL in signals, respectively. This is due to the fact that XPBus for HIC 1600 does not contain a PCN or PCNR line. Another important difference between HIC 1600 and HIC 1200 is the fact that HIC 1600, unlike HIC 1200, has two reset lines, RSTEP# and RSTEH#, instead of only one reset line. Reset line RSTEP# is coupled to Reset & XPBus Parity Error Control Unit 1636 which receives, on the reset line RSTEP#, a

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reset signal and a parity error signal generated by the PIC, sends a reset signal to the CPU CNTL & GPIO latch/driver 1690, and controls retransmission of bits from the parallel to serial converters 1632. Reset & XPBUS Parity Error Detection and Control Unit 1446 takes bits from serial to parallel converters 1642, performs a parity check to detect any transmission error, and sends reset and parity error signals to the PIC on the reset line RSTEN#. The reset and parity error signals may be distinguished by different signal patterns and/or different signal durations. In the two reset line system, the reset and error parity signals are transmitted on the same line and it is possible to send a parity error confirmation signal on one line while receiving a reset signal on the other line. Because HIC 1600 provides for parity error detection, the parallel to serial converters 1632 include buffers. The buffers in parallel to serial converters 1632 store previously transmitted bits (e.g., those transmitted within the previous two clock cycles) for retransmission if transmission error is detected and a parity error signal is received on line RSTEN#. It is to be noted that parallel to serial converters 1232 do not contain buffers such as those contained in parallel to serial converters 1632 for purposes of retransmission since HIC 1200 does not provide for parity error signal detection. Yet another difference between HIC 1200 and HIC 1600 is the fact that in HIC 1600 clock multipliers 1631 and 1641 multiply the PCK and PCKR clocks, respectively, by a factor of 6 rather than 10 because the XPBUS coupled to HIC 1600 transmits six bit packets instead of ten bit packets during each XPBUS clock cycle. Sending a smaller number of bits per XPBUS clock cycle provides the benefit of improving synchronization between the data latching clock output by clock multipliers 1631 and 1641 and the XPBUS clocks, PCK and PCKR. In another embodiment, one may send 5 or some other number of bits per XPBUS clock cycle. As mentioned above, the remaining elements in HIC 1600 are identical to those in HIC 1200 and reference to the description of the elements in HIC 1200 may be made to understand the function of the corresponding elements in HIC 1600.

FIG. 17 is a schematic diagram of the lines PCK and PD0 to PD3. These lines are unidirectional LVDS lines for transmitting signals from HIC 1600 to the PIC of FIG. 15. Another set of lines, namely PCKR and PDR0 to PDR3, are used to transmit clock signals and bits from the PIC to HIC 1600.

In the embodiment shown in FIG. 11, HIC 1119 is coupled to an integrated unit 1121 that includes a CPU, a cache and a north bridge. In yet another embodiment, such as that shown in FIG. 18, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1810 includes a PIC and a south bridge.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

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What is claimed is:

- [1. A computer module, said module comprising: an enclosure, said enclosure being insertable into a console; a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip; a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit; and a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing a possibility of unauthorized use of said hard disk drive.]
- [2. The computer module of claim 1 further comprising a host interface controller for providing a status of a locking device in said enclosure.]
- [3. The computer module of claim 1 further comprising a mechanical locking device that is coupled to said programmable memory device.]
- [4. The computer module of claim 1 further comprising a host interface controller coupled to a mechanical locking device, said host interface controller being coupled to said programmable memory device.]
- [5. The computer module of claim 1 wherein said programmable memory device comprises a flash memory device.]
- [6. The computer module of claim 1 wherein said programmable memory device comprises a flash memory device having at least 8 Mbits of cells and greater.]
- [7. The computer module of claim 1 further comprising a security program in a main memory.]
- [8. The computer module of claim 7 wherein said security program comprises a code for storing a password on said programmable memory device.]
- [9. The computer module of claim 8 wherein said security program comprises a code for checking a time from said real-time clock circuit.]
- [10. The computer module of claim 1 further comprising a host interface controller coupled to a solenoid that drives a mechanical lock in a first position to a second position.]
- [11. The computer module of claim 10 wherein said solenoid also drives said mechanical lock from said second position to said first position.]
- [12. The computer module of claim 1 further comprising a real-time clock circuit coupled to said central processing unit.]
- [13. The computer module of claim 12 further comprising a battery coupled to a host interface controller that includes said real-time clock.]
- [14. A method for operating a computer system, said method comprising: inserting an attached computer module ("ACM") into a bay of a modular computer system, said ACM comprising a microprocessor unit coupled to a mass memory storage device; applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and prompting for a user password from a user on a display.]
- [15. The method of claim 14 wherein said ACM comprises an enclosure that houses said microprocessor unit and said mass memory storage device.]
- [16. The method of claim 14 further comprising providing a user password to said security program.]
- [17. The method of claim 14 further comprising a flash memory device for storing a desired password for said ACM.]

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[18. The method of claim 17 wherein said flash memory device maintains said desired password when power is removed from said ACM.]

[19. The method of claim 18 wherein said flash memory device is coupled to a host interface controller that is coupled to said microprocessor based unit.]

[20. The method of claim 14 wherein said mass memory storage device comprises a code directed to comparing said user password with a desired password.]

[21. The method of claim 14 further comprising identifying a permanent password or user code on said attached computer module.]

[22. The method of claim 21 wherein said permanent password or user code is stored in said microprocessor unit.]

[23. The method of claim 21 wherein said permanent password or user code is stored in a flash memory device coupled to said microprocessor unit.]

24. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console in a modular computer system, the console comprising a first low voltage differential signal (LVDS) channel comprising two unidirectional serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transaction in opposite directions; said ACM comprising a microprocessor unit coupled to a mass memory storage device;

a north bridge to communicate address and data bits of PCI bus transaction in serial form, said north bridge directly coupled to said microprocessor unit;

a main memory coupled to said microprocessor unit through said north bridge; and

a second LVDS channel comprising two unidirectional serial channels that transmit data in opposite directions, said second LVDS channel extending from said north bridge to convey said address and data bits of PCI bus transaction in serial form;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and prompting for a user password from a user on a LCD display coupled to the console.

25. The method of claim 24 wherein said mass memory storage device comprises a flash memory.

26. The method of claim 24 further comprises entering the user password from a keyboard coupled to the console.

27. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a modular computer system housed in a console, said console comprising a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transaction, and an interface controller coupled to the first LVDS channel; said ACM comprising a microprocessor unit coupled to a mass memory storage device;

an integrated interface controller and bridge unit to output address and data bits of PCI bus transaction in serial form, said integrated interface controller and bridge unit directly coupled to said microprocessor unit;

a main memory coupled to said microprocessor unit through said integrated interface controller and bridge unit; and

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a second LVDS channel comprising two sets of unidirectional serial channels that transmit data in opposite directions, said second LVDS channel extending from said integrated interface controller and bridge unit to convey said address and data bits of PCI bus transaction in serial form;

applying power to said computer system, the ACM executing a security program, said security program being stored in said mass storage device;

storing a user password in said ACM; and

prompting for said user password from a user on a display coupled to the console.

28. The method of claim 27 wherein said mass memory storage device comprises a flash memory.

29. The method of claim 27 wherein said security program manages a user's privilege to access data based on said password.

30. The method of claim 27 further comprises transmitting the encoded data as a serial bit stream in 10 bit packets.

31. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console in a modular computer system, said console comprising a LAN communication device and a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional serial channels that transmit data in opposite directions, said ACM comprising a microprocessor unit coupled to a mass memory storage device;

a second LVDS channel comprising two sets of unidirectional serial channels that transmit data in opposite directions; and a peripheral bridge coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus, said peripheral bridge coupled to said second LVDS channel to communicate address and data bits of PCI bus transaction in serial form over said second LVDS channel;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and prompting for a user password from a user on a display.

32. The method of claim 31 wherein said mass memory storage device comprises a flash memory.

33. The method of claim 31 further comprises entering the user password from a keyboard coupled to the console.

34. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console in a modular computer system, said console comprising an integrated LCD display, and a first low voltage differential signal (LVDS) channel comprising two sets of unidirectional serial channels that transmit data in opposite directions, said ACM comprising

a microprocessor unit coupled to a mass memory storage device;

a peripheral bridge to output address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, said peripheral bridge coupled to said microprocessor unit without any intervening PCI bus;

a main memory coupled to said microprocessor unit through said peripheral bridge; and

a second LVDS channel comprising two sets of unidirectional serial channels that transmit data in oppo-



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site directions, said second LVDS channel extending from said peripheral bridge to convey said address and data bits of PCI bus transaction in serial form; applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and prompting for a user password from a user on the LCD display.

35. The method of claim 34 wherein said mass memory storage device comprises a flash memory.

36. The method of claim 34 further comprises entering the user password from a keyboard coupled to the console.

37. A computer module, said module comprising:  
an enclosure, said enclosure being insertable into a console, said console comprising a LAN communication device, and a first channel comprising two low voltage differential signal (LVDS), unidirectional serial channels that transmit in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a peripheral bridge in said enclosure, said peripheral bridge directly coupled to said central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, said peripheral bridge comprising an interface controller to transmit and receive address and data bits of PCI bus transaction in serial form;

a second channel in said enclosure, said second channel comprising two LVDS, unidirectional serial channels that transmit in opposite directions, said second channel extending from said peripheral bridge to convey said address and data bits of PCI bus transaction in serial form;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

38. The computer module of claim 37 wherein said first channel communicates an encoded serial bit stream of PCI bus address and data transaction.

39. The computer module of claim 37 wherein the computer module further comprises an interface device that couples to said second channel.

40. A computer module comprising:  
an enclosure insertable into a console to form a functional computer, said console comprising two sets of low voltage differential signal (LVDS), unidirectional serial bit channels to transmit data in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a peripheral bridge in said enclosure, said peripheral bridge directly coupled to said central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, said peripheral bridge comprising an interface controller coupled to the LVDS channels; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

41. The computer module of claim 40 wherein the low voltage differential signal channels communicate an encoded

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serial bit stream of Peripheral Component Interconnect (PCI) bus address and data transaction.

42. The computer module of claim 40 further comprising a security program configured to manage a user's access privilege of data based on said password.

43. A computer module comprising:  
an enclosure being insertable into a console; said console comprising an LCD display, and a first channel comprising two sets of low voltage differential signal (LVDS), unidirectional serial channels that transmit encoded data of Peripheral Component Interconnect (PCI) bus transaction in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

an integrated interface controller and bridge unit in said enclosure, said integrated interface controller and bridge unit configured to output address and data bits of PCI bus transaction in serial form, said integrated interface controller and bridge unit coupled to said central processing unit without any intervening PCI bus;

a main memory in said enclosure, said main memory coupled to said central processing unit through said integrated interface controller and bridge unit; and

a second channel in said enclosure, said second channel comprising two sets of LVDS, unidirectional serial channels that transmit data in opposite directions, said second channel extending from said integrated interface controller and bridge unit to convey said address and data bits of PCI bus transaction in serial form;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

44. The computer module of claim 43 wherein the computer module further comprises an interface device that couples to the LVDS channels in the console.

45. The computer module of claim 43 wherein the programmable memory device comprise a flash memory.

46. A computer module comprising:  
an enclosure configured to be inserted into a console to form a functional computer; said console comprises a first channel comprising two sets of low voltage differential signal (LVDS), serial channels transmitting data in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a peripheral bridge in said enclosure, said peripheral bridge configured to communicate address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, said peripheral bridge directly coupled to said central processing unit without any intervening PCI bus;

a second channel in said enclosure, said second channel comprising two sets of LVDS, serial channels transmitting data in opposite directions, said second channel extending from said peripheral bridge to convey said address and data bits of PCI bus transaction in serial form;

a hard disk drive in said enclosure, said hard disk drive coupled to said central processing unit;

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a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive; and

an interface device coupled to at least one of said first channel and said second channel.

47. The computer module of claim 46 wherein the console further comprises a LAN communication device wherein the computer module communicates to an external LAN network through the console.

48. A computer module comprising:

an enclosure insertable into a console comprising a Universal Serial Bus (USB) and an interface controller coupled to a first channel comprising two sets of low voltage differential signal (LVDS), unidirectional channels configured to communicate data in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

an integrated interface controller and bridge unit in said enclosure, said integrated interface controller and bridge unit configured to output address and data bits of Peripheral Component Interconnect (PCI) bus transaction in serial form, said integrated interface controller and bridge unit directly coupled to said central processing unit without any intervening PCI bus;

a second channel in said enclosure, said second channel comprising two sets of LVDS, unidirectional channels configured to communicate data in opposite directions, said second channel extending from said integrated interface controller and bridge unit to convey said address and data bits of PCI bus transaction in serial form;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing unauthorized use of said hard disk drive.

49. The computer module of claim 48 wherein the console further comprises a power supply that supplies power to the computer module upon insertion.

50. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console of a modular computer system, said console comprising two sets of differential signal, unidirectional serial channels configured to communicate data in opposite directions, and said ACM comprising a microprocessor unit coupled to a mass memory storage device;

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a peripheral bridge directly coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus; and

a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels configured to communicate data in opposite directions, said LVDS channel extending from said peripheral bridge to convey address and data bits of PCI bus transaction in serial form;

applying power to said computer system and said ACM executing a security program, said security program being stored in said mass memory storage device;

communicating from the computer module to the console through serial bit lines transmitting data packets in Universal Serial Bus (USB) protocol;

prompting for a user password from a user on a LCD display; and

wherein the mass storage device comprises a flash memory.

51. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console of a modular computer system, said console comprising a LAN communication device, and differential signal, unidirectional serial channels configured to communicate data in opposite directions, and said ACM comprising

a microprocessor unit coupled to a mass memory storage device comprising a flash memory;

a peripheral bridge directly coupled to said microprocessor unit without any intervening Peripheral Component Interconnect (PCI) bus; and

a low voltage differential signal (LVDS) channel comprising at least two unidirectional, differential signal pairs configured to communicate data in opposite directions, said LVDS channel extending from said peripheral bridge to convey address and data bits of PCI bus transaction in serial form;

applying power to said computer system and said ACM executing a security program, said security program being stored in said mass memory storage device;

communicating from the computer module to the console through serial bit lines transmitting data packets in Universal Serial Bus (USB) protocol;

prompting for a user password from a user on a display coupled to the console.

52. The method of claim 51 further comprises entering the user password from a keyboard coupled to the console.

53. The method of claim 51, further comprising communicating said address and data bits of PCI bus transaction data in 10 bit packets through said LVDS channel.

\* \* \* \* \*



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(12) **INTER PARTES REEXAMINATION CERTIFICATE** (684th)**United States Patent****Chu**(10) **Number:** **US RE42,814 C1**(45) **Certificate Issued:** **\*Sep. 4, 2013**(54) **PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE**(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)(73) Assignee: **Acqis Technology, Inc.**, Mountain View,  
CA (US)**Reexamination Request:**

No. 95/001,776, Oct. 4, 2011

**Reexamination Certificate for:**Patent No.: **Re. 42,814**Issued: **Oct. 4, 2011**Appl. No.: **12/322,858**Filed: **Feb. 5, 2009**

(\*) Notice: This patent is subject to a terminal disclaimer.

**Related U.S. Patent Documents**

Reissue of:

(64) Patent No.: **6,321,335**Issued: **Nov. 20, 2001**Appl. No.: **09/183,493**Filed: **Oct. 30, 1998**(51) **Int. Cl.**  
**G06F 13/14** (2006.01)(52) **U.S. Cl.**USPC ..... **726/34**; 455/347; 455/349; 713/183;  
726/28(58) **Field of Classification Search**

None

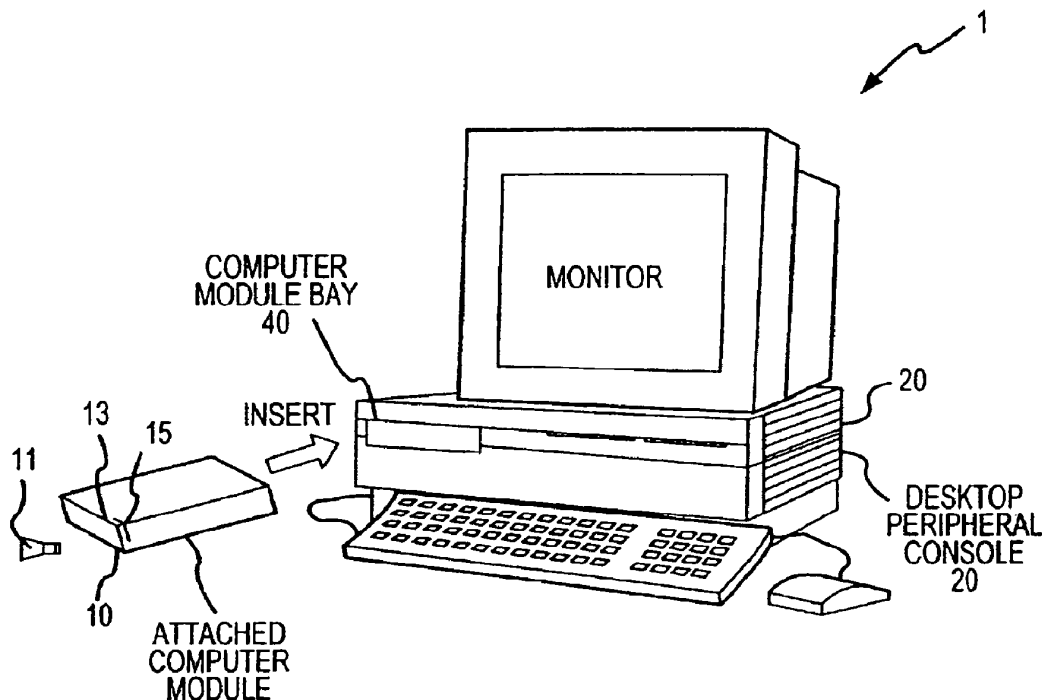
See application file for complete search history.

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To view the complete listing of prior art documents cited during the proceeding for Reexamination Control Number 95/001,776, please refer to the USPTO's public Patent Application Information Retrieval (PAIR) system under the Display References tab.

*Primary Examiner* — Majid A. Banankhah(57) **ABSTRACT**

A method and device for securing a removable Attached Computer Module ("ACM") 10. ACM 10 inserts into a Computer Module Bay ("CMB") 40 within a peripheral console to form a functional computer such as a desktop computer or portable computer. The present ACM 10 includes a locking system, which includes hardware and software 600, 700, to prevent accidental removal or theft of the ACM from the peripheral console. While ACM is in transit, further security is necessary against illegal or unauthorized use. If ACM contains confidential data, a high security method is needed to safeguard against theft.



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**INTER PARTES  
REEXAMINATION CERTIFICATE  
ISSUED UNDER 35 U.S.C. 316**

5

THE PATENT IS HEREBY AMENDED AS  
INDICATED BELOW.

AS A RESULT OF REEXAMINATION, IT HAS BEEN  
DETERMINED THAT:

10

The patentability of claims ~~24-39~~, ~~41~~ and ~~43-53~~ is  
confirmed.

Claims ~~1-23~~ were previously cancelled.

Claims ~~40~~ and ~~42~~ are cancelled.

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\* \* \* \* \*



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 (12) **Reissued Patent**  
 Chu

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 (45) **Date of Reissued Patent:** **\*Jan. 17, 2012**

(54) **PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE**

(75) Inventor: **William W. Y. Chu**, Los Altos, CA (US)

(73) Assignee: **ACQIS LLC**, McKinney, TX (US)

(\*) Notice: This patent is subject to a terminal disclaimer.

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**H04L 9/00** (2006.01)

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 726/28

(58) **Field of Classification Search** ..... 713/164,  
 713/172, 189, 190, 193, 194; 711/164; 726/9,  
 726/18, 28, 34; 710/301  
 See application file for complete search history.

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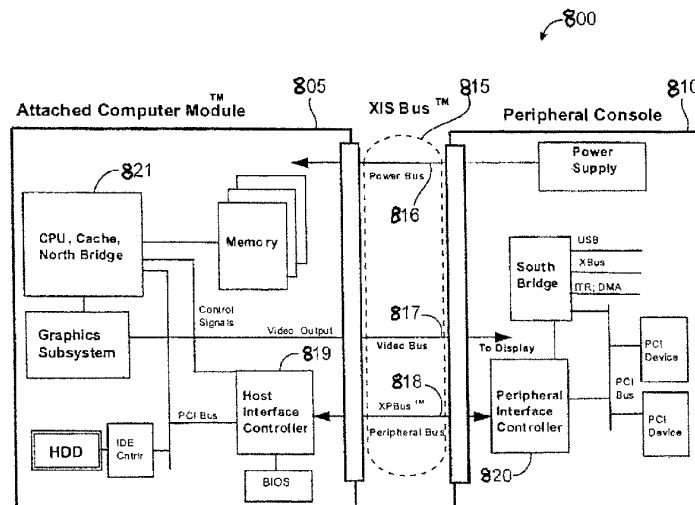
*Primary Examiner* — Beemnet Dada

(74) *Attorney, Agent, or Firm* — Cooley LLP

(57) **ABSTRACT**

A method and device for securing a removable Attached Computer Module ("ACM") 10. ACM 10 inserts into a Computer Module Bay ("CMB") 40 within a peripheral console to form a functional computer such as a desktop computer or portable computer. The present ACM 10 includes a locking system, which includes hardware and software 600, 700, to prevent accidental removal or theft of the ACM from the peripheral console. While ACM is in transit, further security is necessary against illegal or unauthorized use. If ACM contains confidential data, a high security method is needed to safeguard against theft.

**43 Claims, 15 Drawing Sheets**



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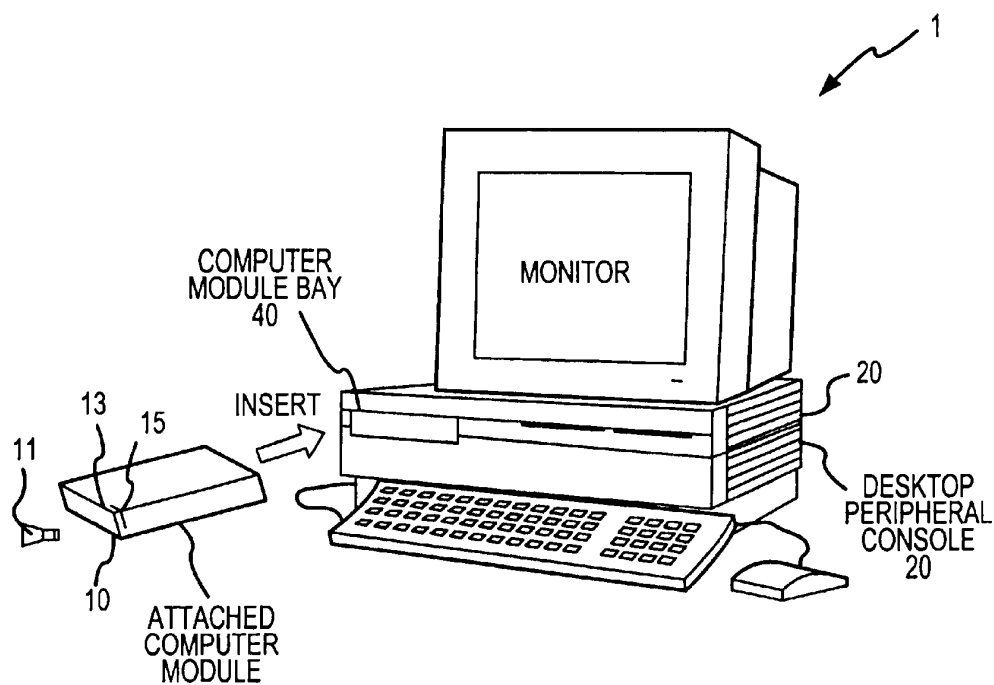


FIG.1

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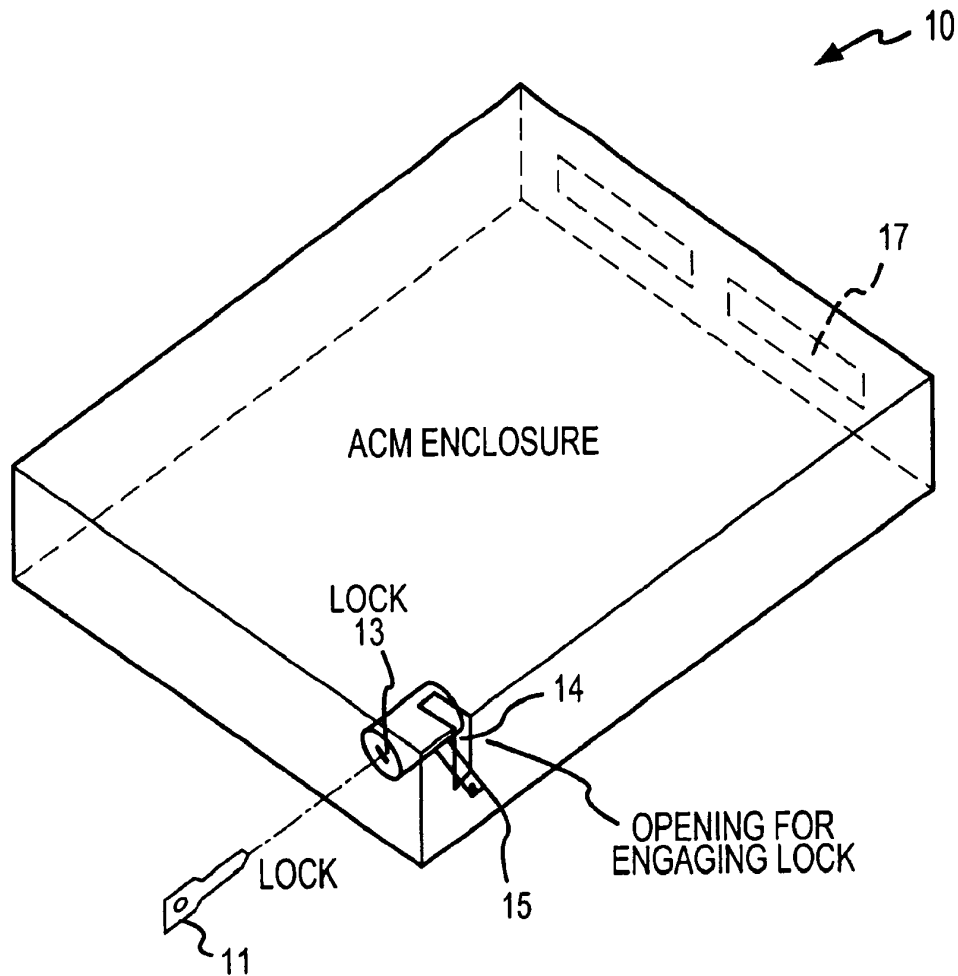


FIG.2

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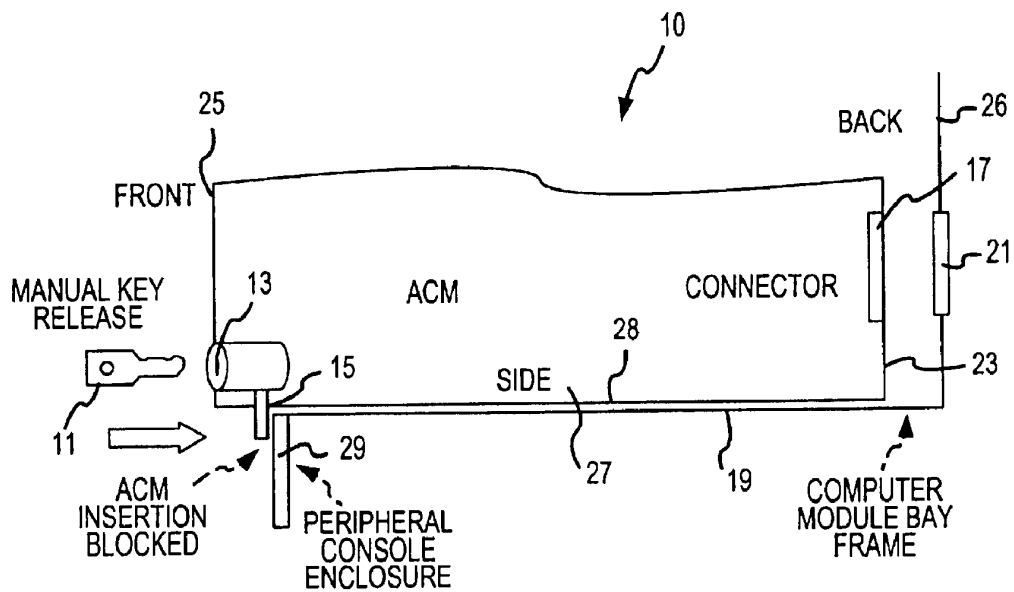


FIG.3

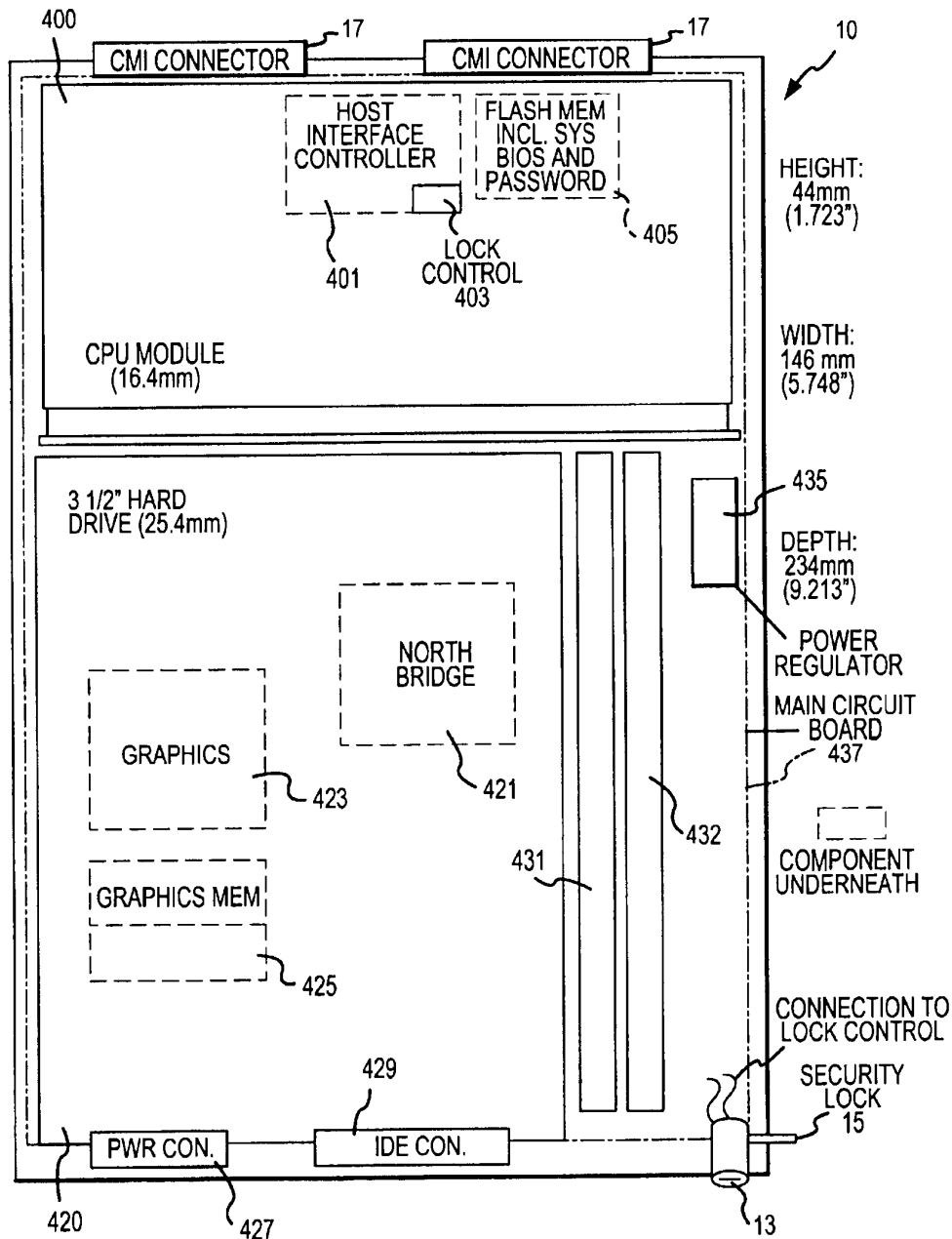


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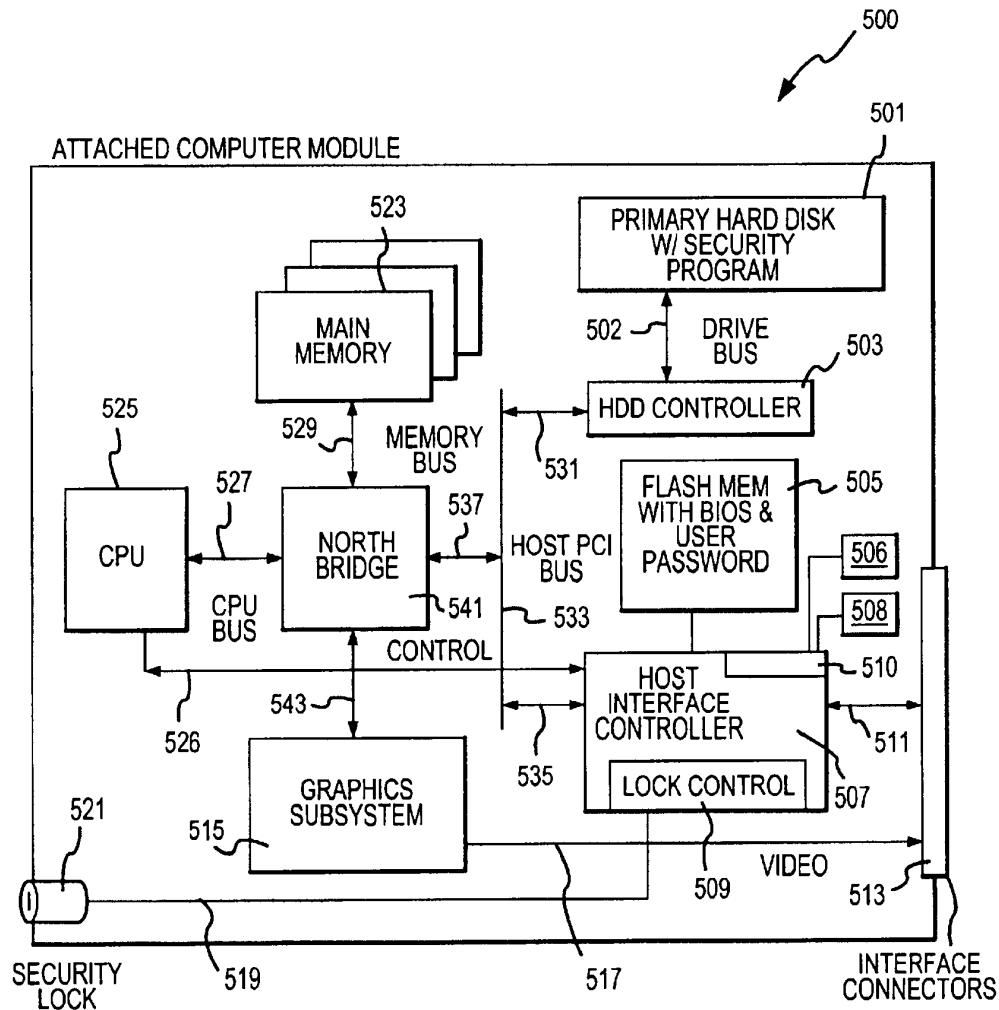


FIG.5

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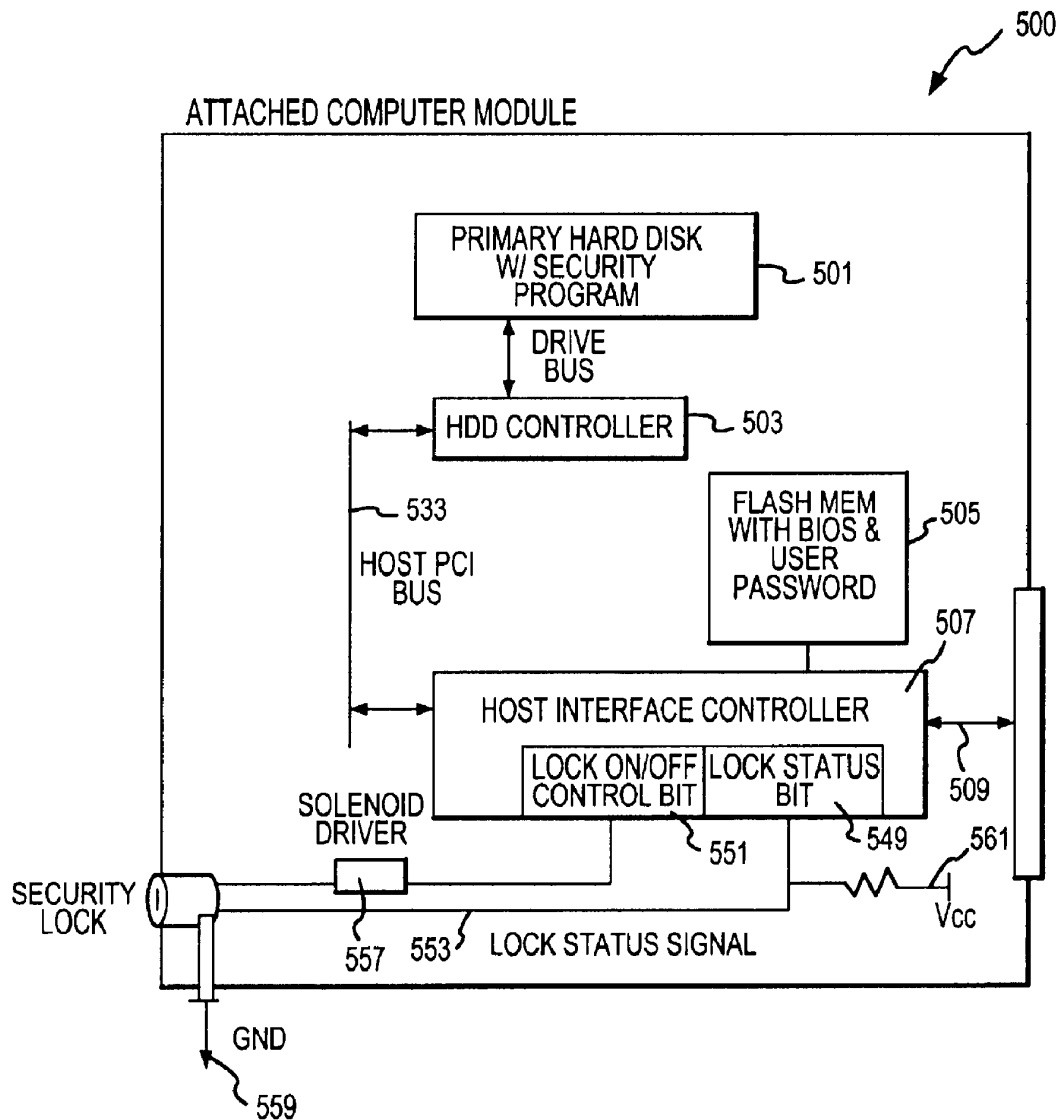


FIG.5A

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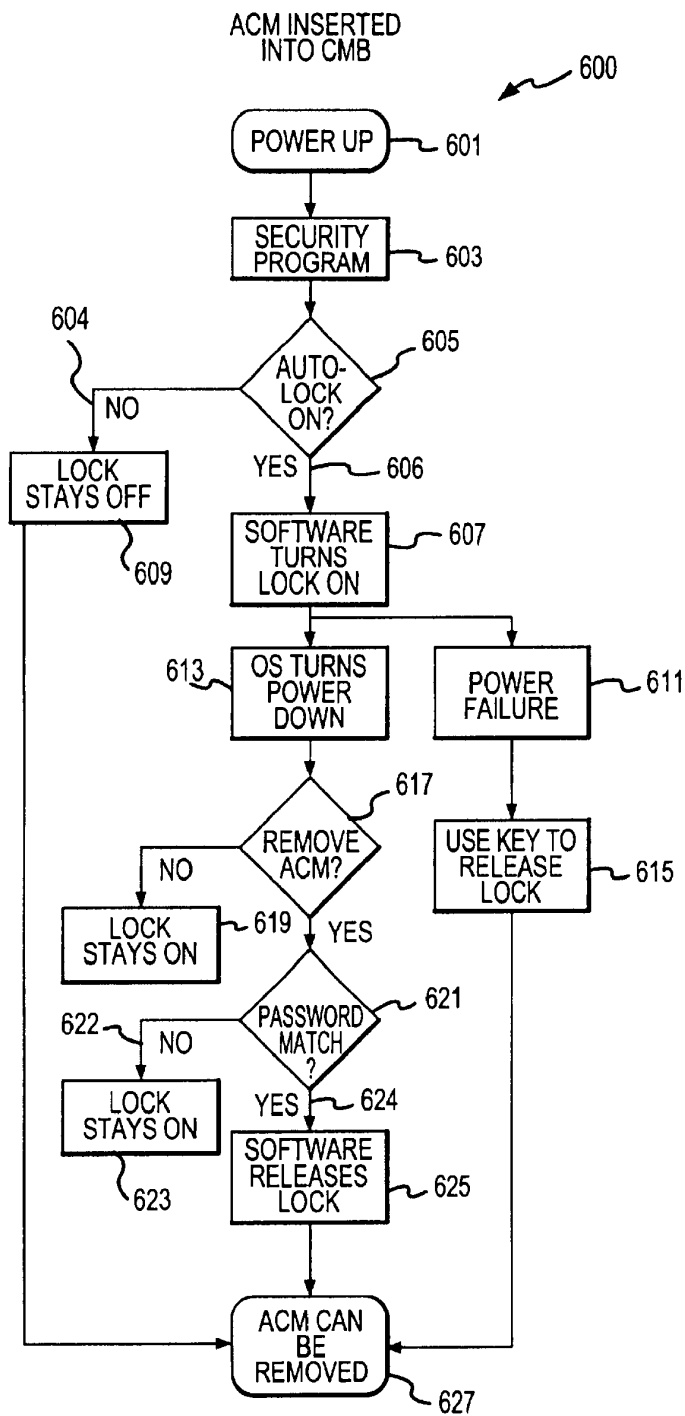


FIG.6

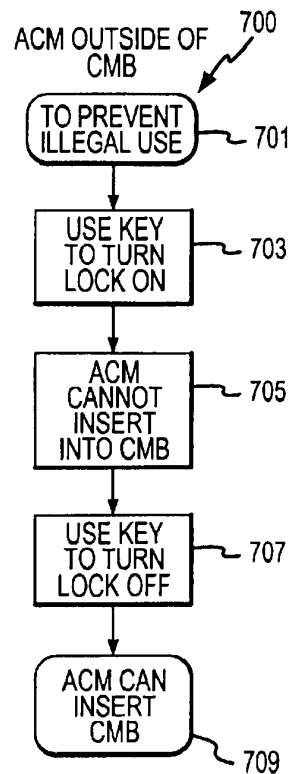


FIG.7

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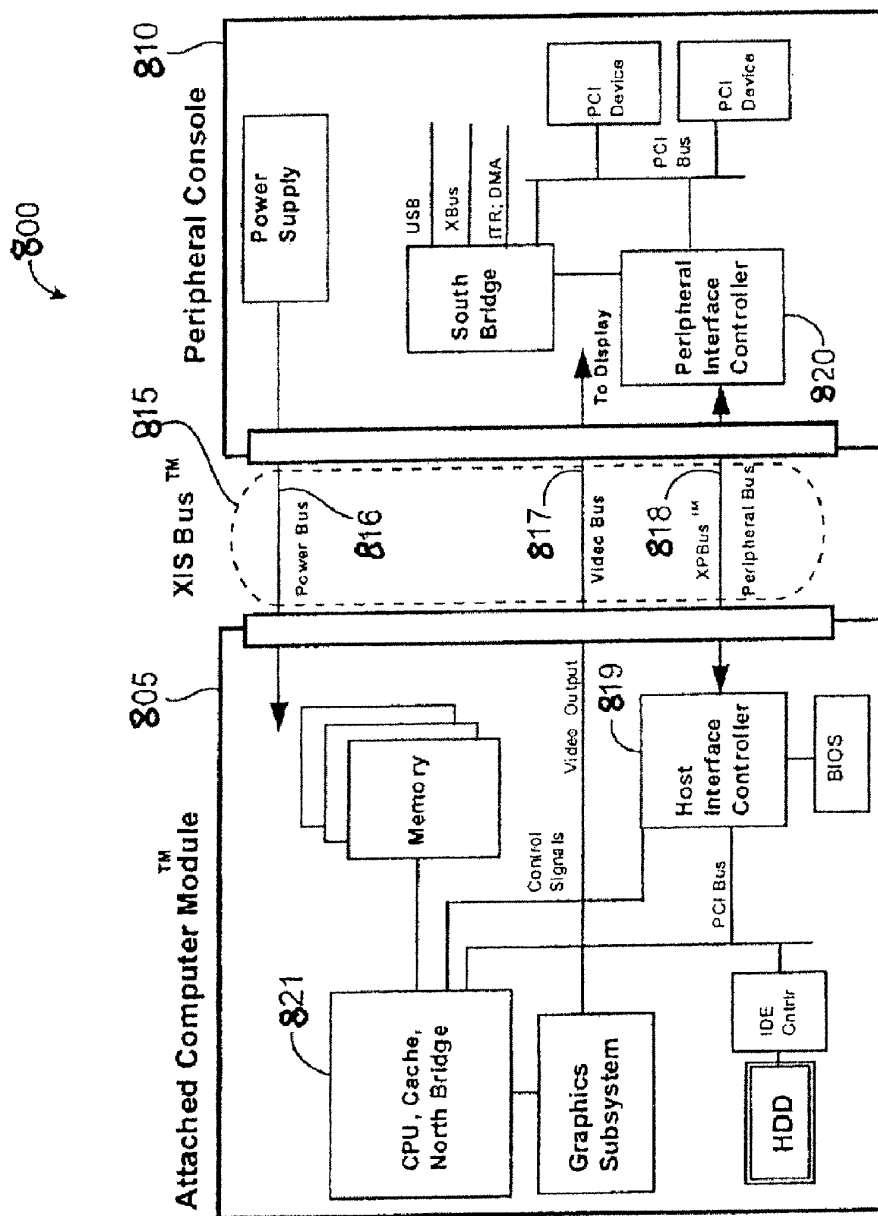


FIG. 8

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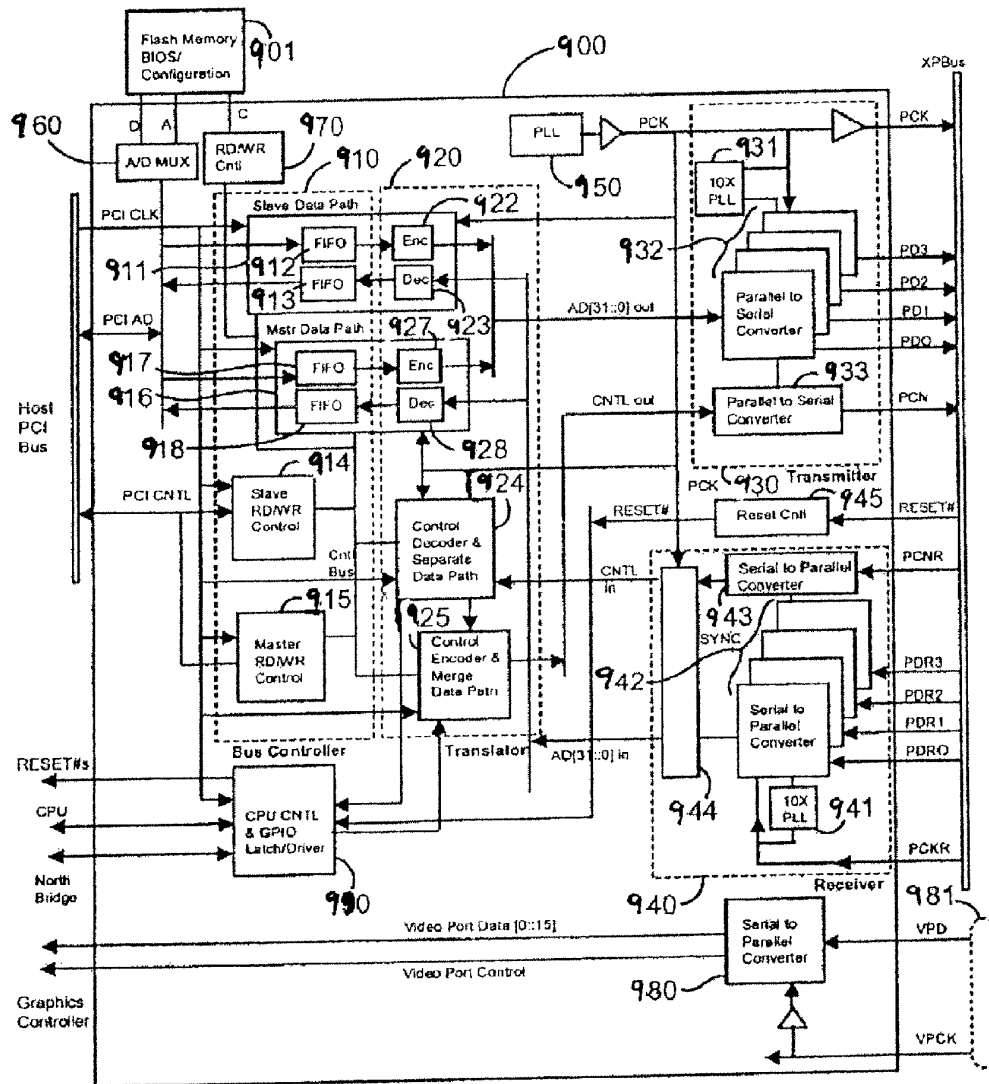


FIG. 9



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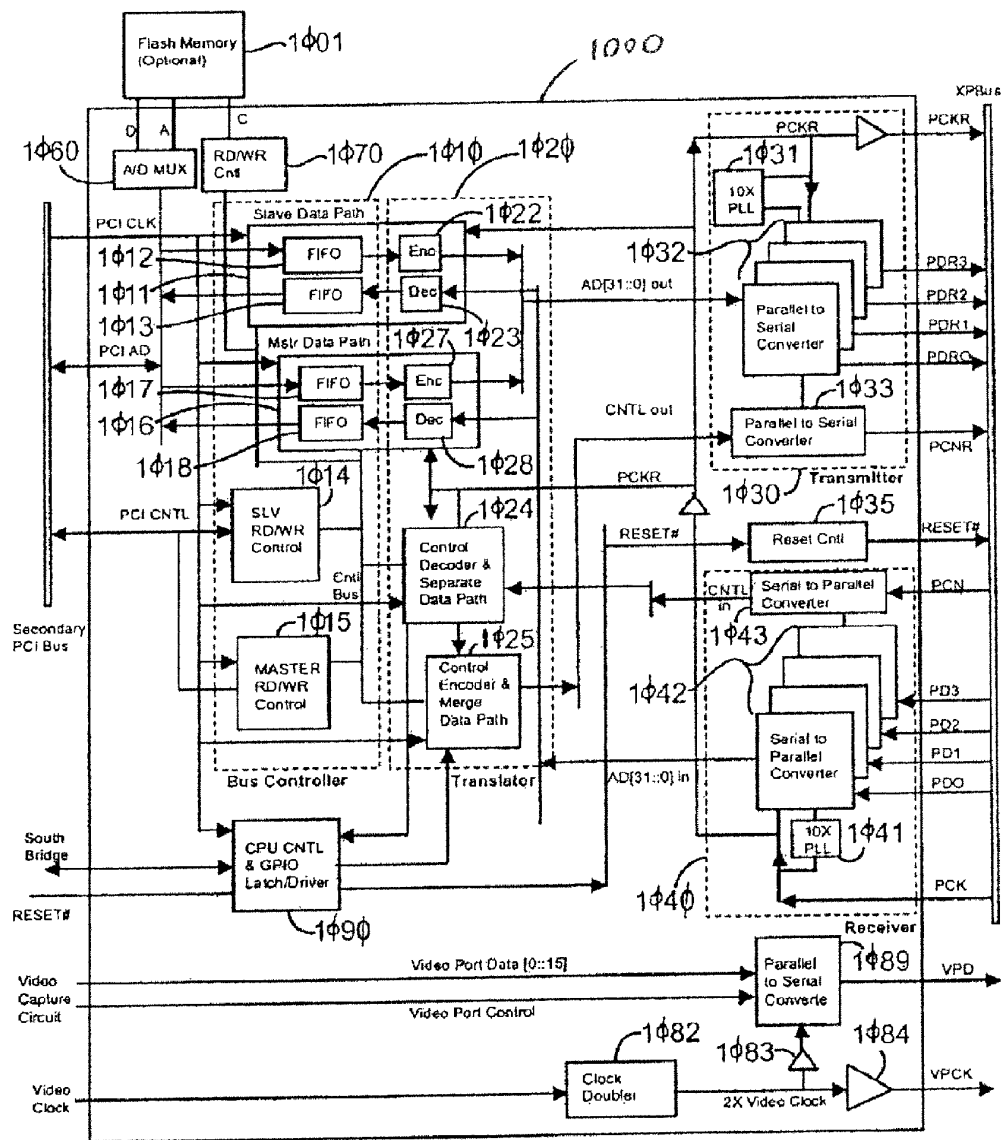


FIG. 10

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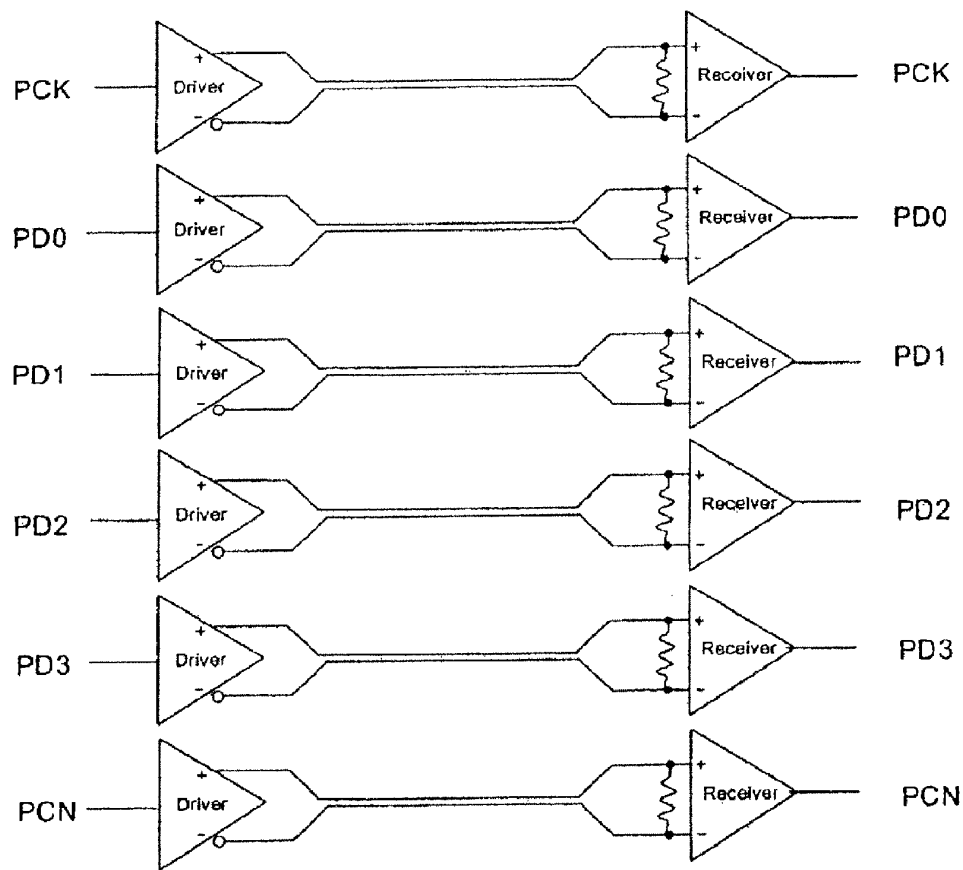


FIG. 11

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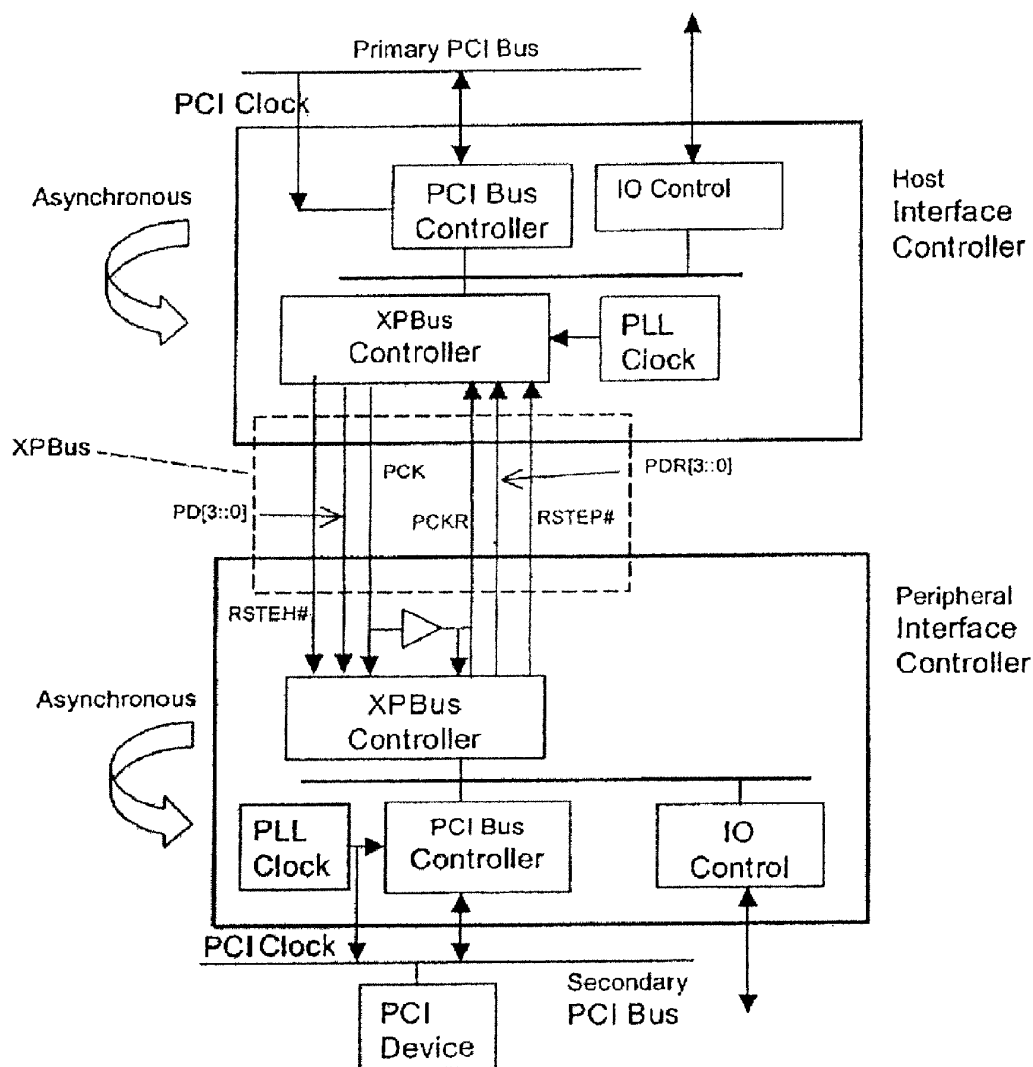


FIG. 12

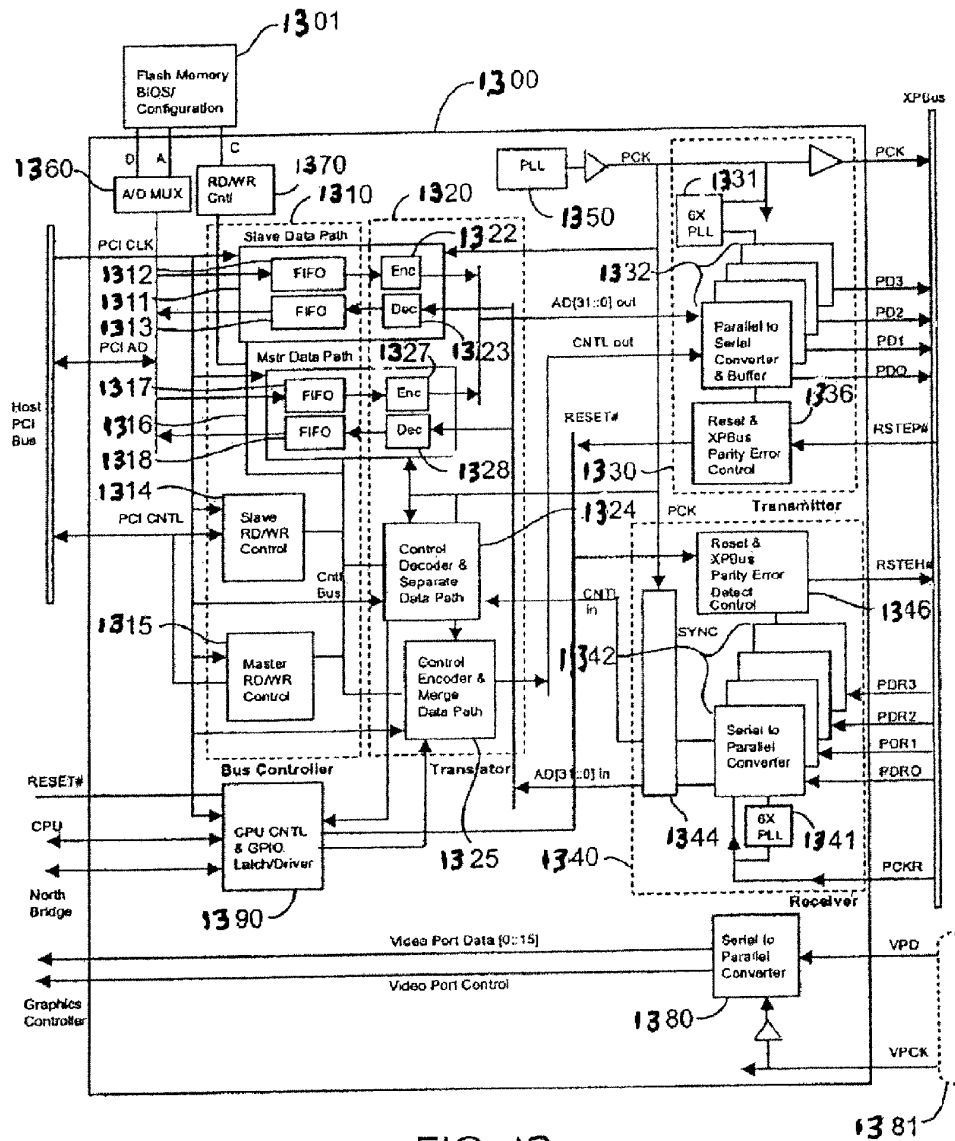


FIG. 13

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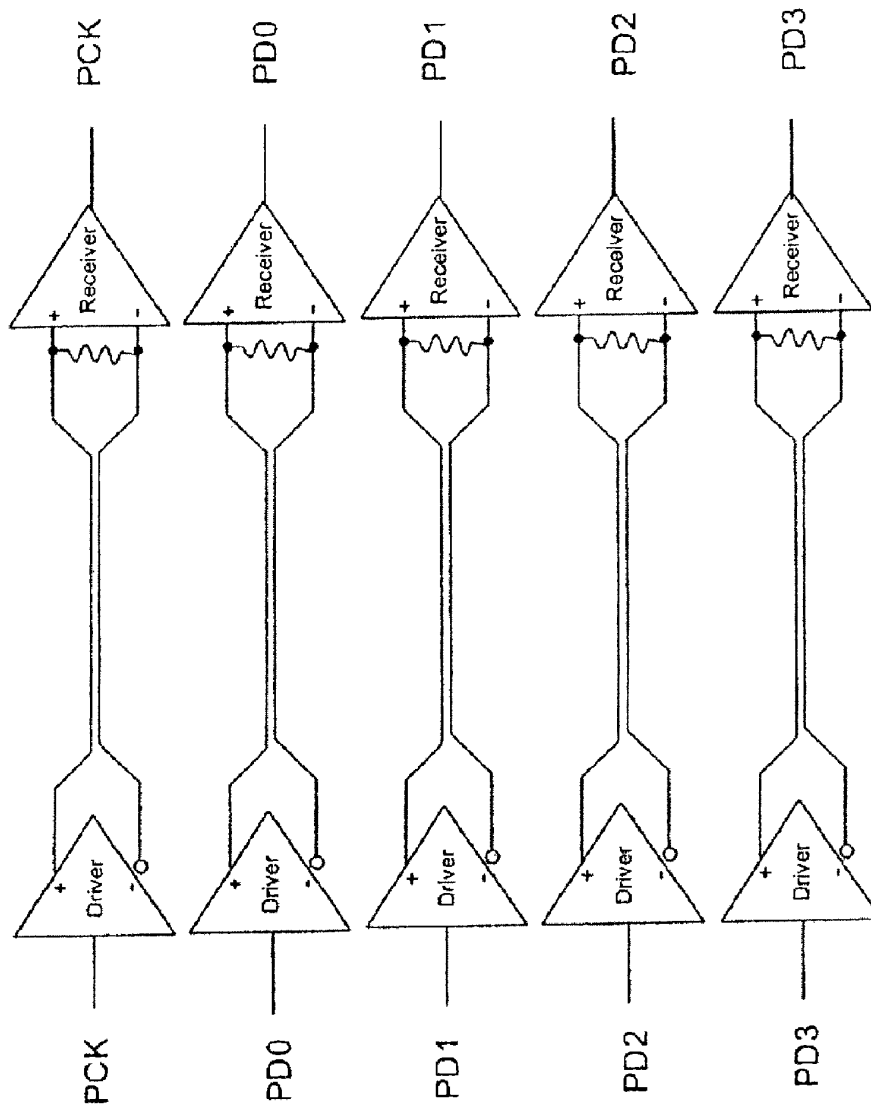


FIG. 14

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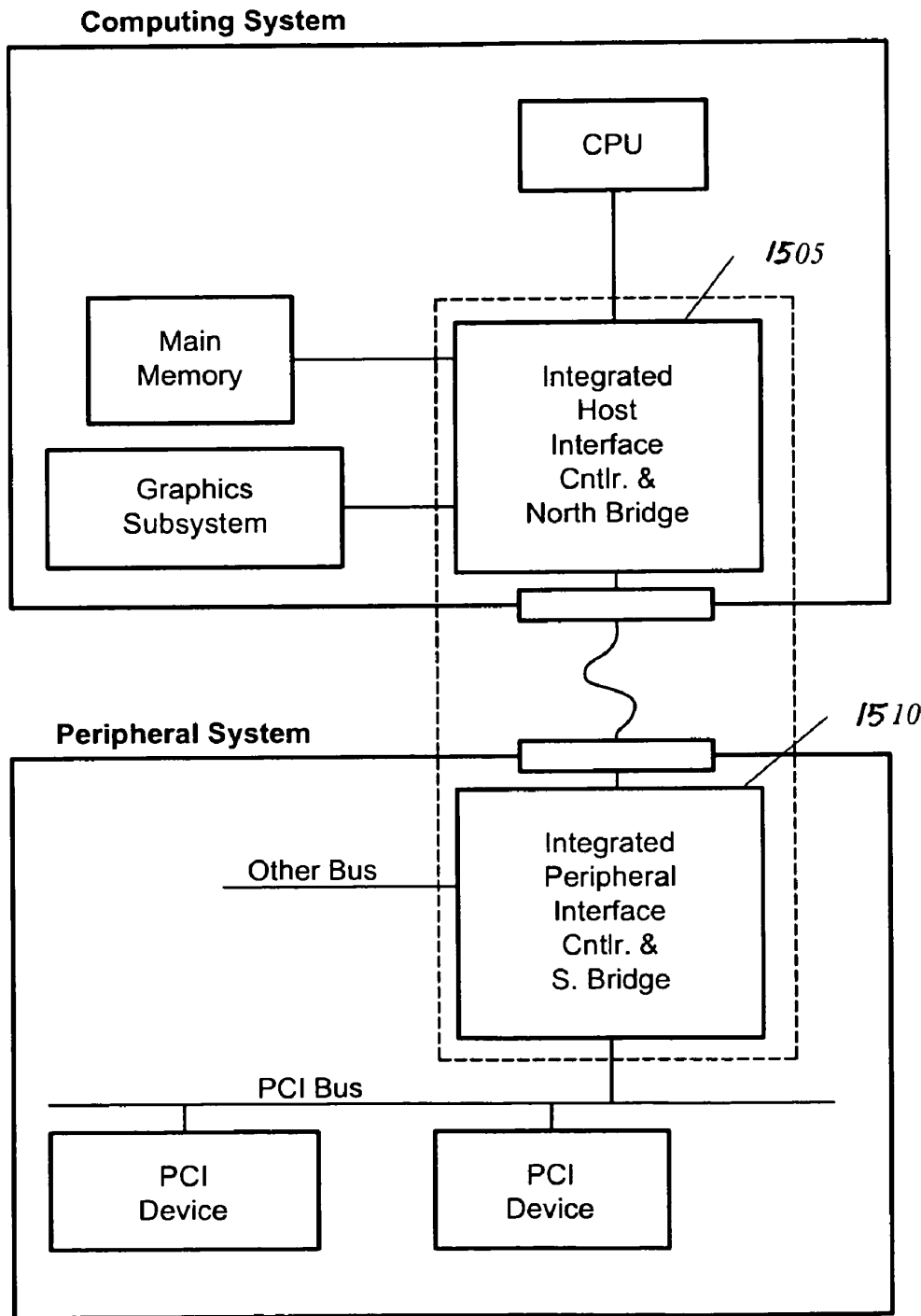


FIGURE 15



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PASSWORD PROTECTED MODULAR  
COMPUTER METHOD AND DEVICE

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

CROSS REFERENCE TO RELATED  
APPLICATIONS

*Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,321,335. The reissue applications are U.S. application Ser. Nos. 10/963,825 (a parent reissue application), 11/474,256 (which is a continuation reissue of the parent reissue application), 11/517,601 (which is a continuation reissue of the parent reissue application), 12/577,074 (the present application, which is a continuation reissue of the parent reissue application), and 12/322,858 (which is a continuation reissue of U.S. application Ser. No. 11/517,601).*

*This application is a continuation reissue of U.S. application Ser. No. 10/963,825, which is a reissue of U.S. Pat. No. 6,321,335, which are incorporated herein by reference.*

The following two commonly-owned copending applications, including this one, are being filed concurrently and the other one is hereby incorporated by reference in their entirety for all purposes:

1. U.S. patent application Ser. No. 09/183,816, William W. Y. Chu, entitled, "Modular Computer Security Method and Device", and
2. U.S. patent application Ser. No. 09/183,493, William W. Y. Chu, entitled, "Password Protected Modular Computer Method and Device".

## BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box using password protection techniques. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to a server as well as other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive such as memory in the giga-bit range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 20 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can

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be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have poor display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals that are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it

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is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have proprietary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

Thus what is needed are computer systems that provide reduced user investment in redundant computer components and provide a variable level of performance based upon computer configuration.

## SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module using a password in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a Computer Module Bay (CMB) within a peripheral console to form a functional computer.

In a specific embodiment, the present invention provides a computer module. The computer module has an enclosure that is insertable into a console. The module also has a central processing unit (i.e., integrated circuit chip) in the enclosure. The module has a hard disk drive in the enclosure, where the hard disk drive is coupled to the central processing unit. The module further has a programmable memory device in the enclosure, where the programmable memory device can be configurable to store a password for preventing a possibility of unauthorized use of the hard disk drive and/or other module elements. The stored password can be any suitable key strokes that a user can change from time to time. In a further embodiment, the present invention provides a permanent password or user identification code stored in flash memory, which also can be in the processing unit, or other integrated circuit element. The permanent password or user identification code is designed to provide a permanent "finger print" on the attached computer module.

In a specific embodiment, the present invention provides a variety of methods. In one embodiment, the present invention provides a method for operating a computer system such as a modular computer system and others. The method includes inserting an attached computer module ("ACM") into a bay of a modular computer system. The ACM has a microprocessor unit (e.g., microcontroller, microprocessor) coupled to a mass memory storage device (e.g., hard disk). The method also includes applying power to the computer system and the ACM to execute a security program, which is stored in the mass memory storage device. The method also includes prompting for a user password from a user on a display (e.g., flat panel, CRT). In a further embodiment, the present method includes a step of reading a permanent password or user identification code stored in flash memory, or other integrated circuit element. The permanent password or user identification code provides a permanent finger print on the attached computer module. The present invention includes a variety of these methods that can be implemented in computer codes, for example, as well as hardware.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to

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prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified side-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention;

FIG. 5 is a simplified block diagram of a security system for a computer module according to an embodiment of the present invention; and

FIGS. 6 and 7 show simplified flow diagrams of security methods according to embodiments of the present invention.

FIG. 8 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 9 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention.

FIG. 10 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 11 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 12 is a block diagram of another embodiment of the HIC and PIC of the present invention and the interface therebetween.

FIG. 13 is a detailed block diagram of another embodiment of the HIC of the present invention.

FIG. 14 is a schematic diagram of the signal lines PCK and PD0 to PD3.

FIG. 15 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

## DESCRIPTION OF SPECIFIC EMBODIMENTS

## I. System Hardware

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 1 includes an attached computer module (i.e., ACM) 10, a desktop console 20, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, ACM 10 includes computer components, as will be described below, including a central

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processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) **40** is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM **10**. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending patent application Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998, commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking system includes at least a key **11**. The key **11** mates with key hole **13** in a lock, which provides a mechanical latch **15** in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the Fig. below.

FIG. 2 is a simplified diagram of a computer module **10** according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous Fig. for easy reading. The computer module **10** includes key **11**, which is insertable into keyhole **13** of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening **14**, which allows the latch to move into and out of the ACM. The ACM also has openings **17** in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. 3 is a simplified side-view diagram of a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. As shown, the ACM module inserts into the computer module bay frame **19**, which is in the console. A side **27** and a bottom **19** of ACM slide and fit firmly into the computer module bay frame, which has at least a bottom portion **19** and back portion **26**. A backside **23** of the ACM faces backside **26** of the frame. ACM also has a front-side or face **25** that houses the lock and exposes the keyhole **13** to a user. The key **11** is insertable from the race into the keyhole.

As the ACM inserts into the frame, connector **17** couples and inserts into connector **21**. Connector **17** electrically and mechanically interface elements of the ACM to the console through connector **21**. Latch **14** should be moved away from the bottom side **19** of the module bay frame before inserting the ACM into the frame. Once the ACM is inserted fully into the frame, latch **15** is placed in a closed or lock position, where it keeps the ACM firmly in place. That is, latch **15** biases against a backside portion **29** of the ACM enclosure to hold the ACM in place, where the connector **17** firmly

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engages, electrically and mechanically, with connector **21**. To remove the ACM, latch **15** is moved away or opened from the back side portion of the ACM enclosure. ACM is manually pulled out of the computer module bay frame, where connector **17** disengages with connector **21**. As shown, the key **11** is used to selectively move the latch in the open or locked position to secure the ACM into the frame module.

In most embodiments, the ACM includes an enclosure such as the one described with the following components, which should not be limiting:

- 1) A CPU with cache memory;
- 2) Core logic device or means;
- 3) Main memory;
- 4) A single primary Hard Disk Drive ("HDD") that has a security program;
- 5) Flash memory with system BIOS and programmable user password;
- 6) Operating System, application software, data files on primary HDD;
- 7) An interface device and connectors to peripheral console;
- 8) A software controllable mechanical lock, lock control means, and other accessories.

The ACM connects to a peripheral console with power supply, a display device, an input device, and other elements. Some details of these elements with the present security system are described in more detail below.

FIG. 4 is a simplified layout diagram of a security system for a computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module **10**, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module **400**, and a second portion, which includes a hard drive module **420**. A common printed circuit board **437** houses these modules and the like. Among other features, the ACM includes the central processing unit module **400** with a cache memory **405**, which is coupled to a north bridge unit **421**, and a host interface controller **401**. The host interface controller includes a lock control **403**. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors **17**. Here, the CPU module is spatially located near connector **17**.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller **401** is coupled to BIOS/flash memory **405**. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control **403** to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.



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The second portion of the attached computer module has the hard drive module **420**. Among other elements, the hard drive module includes north bridge **421**, graphics accelerator **423**, graphics memory **425**, a power controller **427**, an IDE controller **429**, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus **431**, **432**. A power regulator **435** is disposed near the PCI bus.

In a specific embodiment, north bridge unit **421** often couples to a computer memory, to the graphics accelerator **423**, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator **423** typically couples to a graphics memory **423**, and other elements. IDE controller **429** generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, 1394, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **420** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Wash. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **420** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE. Among other features, the computer system includes an ACM with security protection. The ACM connects to the console, which has at least the following elements, which should not be limiting.

- 1) Connection to input devices, e.g. keyboard or mouse;
- 2) Connection to display devices, e.g. Monitor;
- 3) Add-on means, e.g. PCI add-on slots;
- 4) Removable storage media subsystem, e.g. Floppy drive, CDROM drive;
- 5) Communication device, e.g. LAN or modem;
- 6) An interface device and connectors to ACM;
- 7) A computer module bay with a notch in the frame for ACM's lock; and
- 8) Power supply and other accessories.

As noted, the computer module bay is an opening in a peripheral console that receives the ACM. The computer module bay provides mechanical support and protection to ACM. The module bay also includes, among other elements, a variety of thermal components for heat dissipation, a frame that provides connector alignment, and a lock engagement, which secures the ACM to the console. The bay also has a printed circuit board to mount and mate the connector from the ACM to the console. The connector provides an interface between the ACM and other accessories.

FIG. 5 is a simplified block diagram **500** of a security system for a computer module according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram **500** has a variety of features such as those noted above, as well as

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others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram is an attached computer module **500**. The module **500** has a central processing unit, which communicates to a north bridge **541**, by way of a CPU bus **527**. The north bridge couples to main memory **523** via memory bus **529**. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem **515** via bus **[542]** **543**. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal **517** to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2½ inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines **502** and **531**. The hard disk drive controller couples to the north bridge by way of the host PCI bus, which connects bus **537** to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device **505** with a BIOS. The flash memory device **505** also has codes for a user password that can be stored in the device. The flash memory device generally permits the **5** storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 4 Meg. or greater of memory, or 16 Meg. or greater of memory. A host interface controller **507** [communications] communicates to the north bridge via bus **535** and host PCI bus. The host interface controller also has a lock control **509**, which couples to a lock. The lock is attached to the module and has a manual override to the lock on the host interface controller in some embodiments. Host interface controller **507** communicates to the console using bus **511**, which couples to [connection] connector **513**.

In one aspect of the present invention the security system uses a combination of electrical and mechanical locking mechanisms. Referring to FIG. 5A, for example, the present system provides a lock status mechanism in the host interface controller **509**. The lock status of the lock is determined by checking a lock status bit **549**, which is in the host interface controller. The lock status bit is determined by a signal **553**, which is dependent upon the position of the lock. Here, the position of the lock is closed in the ground **559** position, where the latch couples to a ground plane in the module and/or system. Alternatively, the signal of the lock is at Vcc, for example, which is open. Alternatively, the signal can be ground in the open position and Vcc in the closed position, depending upon the application. Other signal schemes can also be used depending upon the application.

Once the status is determined, the host interface controller turns the lock via solenoid **557** in a lock on or lock off position, which is provided through the control bit **551**, for example. The control bit is in a register of the host interface controller in the present example. By way of the signal schemes noted and the control bit, it is possible to place the

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lock in the lock or unlock position in an electronic manner. Once the status of the lock is determined, the host interface controller can either lock or unlock the latch on the module using a variety of prompts, for example.

In a preferred embodiment, the present invention uses a password protection scheme to electronically prevent unauthorized access to the computer module. The present password protection scheme uses a combination of software, which is a portion of the security program, and a user password, which can be stored in the flash memory device **505**. By way of the flash memory device, the password does not become erased by way of power failure or the lock. The password is substantially fixed in code, which cannot be easily erased. Should the user desire to change the password, it can readily be changed by erasing the code, which is stored in flash memory and a new code (i.e., password) is written into the flash memory. An example of a flash memory device can include a Intel Flash 28F800F3 series flash, which is available in 8 Mbit and 16 Mbit designs. Other types of flash devices can also be used, however. Details of a password protection method are further explained below by way of the FIGS.

In a specific embodiment, the present invention also includes a real-time clock **510** in the ACM, but is not limited. The real-time clock can be implemented using a reference oscillator 14.31818 MHz **508** that couples to a real-time clock circuit. The real-time clock circuit can be in the host interface controller. An energy source **506** such as a battery can be used to keep the real-time clock circuit running even when the ACM has been removed from the console. The real-time clock can be used by a security program to perform a variety of functions. As merely an example, these functions include: (1) fixed time period in which the ACM can be used, e.g., ACM cannot be used at night; (2) programmed ACM to be used after certain date, e.g., high security procedure during owner's vacation or non use period; (3) other uses similar to a programmable time lock. Further details of the present real-time clock are described in the application listed under Ser. No. 09/183,816 noted above.

In still a further embodiment, the present invention also includes a permanent password or user identification code to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present password and user identification can be quite important for electronic commerce applications and the like. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program, which is described below in more detail.

## II. SECURITY DETECTION PROGRAMS

FIGS. 6 and 7 show simplified flow diagrams **600**, **700** of security methods according to embodiments of the present invention. These diagrams are merely illustrations and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and

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alternatives. Referring to FIG. 6, which considers an example for when the ACM is inserted into the computer module bay in the console, ACM has already been inserted into the console and is firmly engaged in an electrical and mechanical manner. A computer system is powered up **601**, which provides selected signals to the microprocessor. The microprocessor oversees the operation of the computer system. The microprocessor searches the memory in, for example, the hard disk drive and execute a security program, step **603**.

The security program runs through a sequence of steps before allowing a user to operate the present system with the ACM. Among other processes, the security program determines if an "Auto-lock" is ON. If so, the security program goes via branch **606** to step **607**. Alternatively, the security program goes to step **609**, which determines that the lock stays OFF and loops to step **627**, which indicates that the ACM can be removed physically from the console. In step **607**, the security program turns a switch or switching means that turns ON a lock, which can be electrical, mechanical, or a combination of electrical and mechanical.

In a specific embodiment, the security program turns OFF the power of the ACM and console. Here, the security program directs the OS to turn the power OFF, step **613**. In an embodiment where power failure occurs (step **611**), a key is used to release a latch in the ACM on the lock **615**, where the ACM can be removed, step **627**. From step **613**, the security program determines if the ACM is to be removed, step **617**. If not, the lock stays ON, step **619**. Alternatively, the security detection program determines if the password (or other security code) matches with the designated password, step **621**. If not, the lock stays ON, step **623**. Alternatively, the security program releases the lock **625**, which frees the ACM. Next, the ACM can be removed, step **627**.

In an alternative embodiment, the present invention provides a security system for the ACM, which is outside the console or computer module bay. See, FIG. 7, for example. As shown, the security system is implemented to prevent illegal or unauthorized use (step **701**) of the ACM, which has not been used in the console. Here, a key turns ON a lock (step **703**). The lock moves a latch in the ACM to a specific spatial location that physically blocks the passage of the ACM into the computer module bay. Accordingly, the ACM cannot insert (step **705**) into the computer module bay.

In an alternative aspect, the key can be used to turn the lock OFF, step **707**. Here, the key moves the latch in a selected spatial location that allows the ACM to be inserted into the computer bay module. In the OFF position, the ACM inserts into the computer module bay, step **709**. Once the ACM is in the bay, a user can begin operating the ACM through the console. In one embodiment, the computer console including the ACM goes through the sequence of steps in the above FIG., but is not limited.

In a specific embodiment, the present invention implements the sequences above using computer software. In other aspects, computer hardware can also be used and is preferably in some applications. The computer hardware can include a mechanical lock, which is built into the ACM. An example of such mechanical lock is shown above, but can also be others. In other aspects, the lock can be controlled or accessed electronically by way of computer software. Here, the key can be used to as a manual override if the ACM or computer fails.

The lock is used to prevent theft and accidental removal inside CMB. The current invention locates the lock inside the ACM to allow a user to keep a single key as ACM is moved from console to console at different locations. When ACM is in transit, the lock can be engaged using the key so that the latch extends outside ACM's enclosure. The extended latch

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prevents ACM from being inserted into any CMB. This prevents any illegal use of ACM by someone other than the user.

In one aspect of the invention, the user password is programmable. The password can be programmable by way of the security program. The password can be stored in a flash memory device within the ACM. Accordingly, the user of the ACM and the console would need to have the user password in order to access the ACM. In the present aspect, the combination of a security program and user password can provide the user a wide variety of security functions as follows:

- 1) Auto-lock capability when ACM is inserted into CMB;
- 2) Access privilege of program and data;
- 3) Password matching for ACM removal; and
- 4) Automatic HDD lock out if tempering is detected.

In still a further embodiment, the present invention also includes a method for reading a permanent password or user identification aide to identify the computer module. In one embodiment, the permanent password or user code is stored in a flash memory device. Alternatively, the permanent password or user code is stored in the central processing unit. The password or user code can be placed in the device upon manufacture of such device. Alternatively, the password or user code can be placed in the device by a one time programming techniques using, for example, fuses or the like. The present password or user code provides a permanent "finger print" on the device, which is generally hardware. The permanent finger print can be used for identification purposes for allowing the user of the hardware to access the hardware itself, as well as other systems. These other systems include local and wide area networks. Alternatively, the systems can also include one or more servers. The present method allows a third party confirm the user by way of the permanent password or user code. The present password and user identification can be quite important for electronic commerce applications and the like, which verify the user code or password. In one or more embodiments, the permanent password or user code can be combined with the password on flash memory for the security program.

Two PCI or PCI-like buses are interfaced using a non-PCI or non-PCI-like channel. PCI control signals are encoded into control bits, and the control bits, rather than the control signals that they represent, and are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using low voltage differential signal ("LVDS") channels for the interface. An LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel. Therefore, an LVDS channel is advantageously used for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

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In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

FIG. 8 is a block diagram of one embodiment of a computer system 800 using the interface of the present invention. Computer system 800 includes an attached computer module (ACM) 805 and a peripheral console 810. The ACM 805 and the peripheral console 810 are interfaced through an exchange interface system (XIS) bus 815. The XIS bus 815 includes power bus 816, video bus 817 and peripheral bus (XPBus) 818, which is also herein referred to as an interface channel. The power bus 816 transmits power between ACM 805 and peripheral console 810. In a preferred embodiment power bus 816 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 817 transmits video signals between the ACM 805 and the peripheral console 810. In a preferred embodiment, the video bus 817 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 818 is coupled to host interface controller (HIC) 819 and to peripheral interface controller (PIC) 820, which is also sometimes referred to as a bay interface controller.

FIG. 9 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in FIG. 9, HIC 900 comprises bus controller 910, translator 920, transmitter 930, receiver 940, a PLL 950, an address/data multiplexer (A/D MUX) 960, a read/write controller (RD/WR Cntl) 970, a video serial to parallel converter 980 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 990.

HIC 900 is coupled to an optional flash memory BIOS configuration unit 901. Flash memory unit 901 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 960 and RD/WR Control 970, which control the programming, read, and write of flash memory unit 901.

Bus controller 910 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 910 includes a slave (target) unit 911 and a master unit 916. Both slave unit 911 and master unit 916 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 916 as well as the two FIFOs in the slave unit 911 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 911 includes encoder 922 and decoder 923, while master unit 916 includes encoder 927 and decoder 928. The FIFOs 912, 913, 917 and 918 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 9 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 912 and 917 before they are encoded by encoders 922 and 927. Encoders 922 and 927 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal



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on the XDBus. Similarly, address and data information from the receivers is decoded by decoders 923 and 928 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 913 and 918 prior to being transferred to the host PCI bus. FIFOs 912, 913, 917 and 918 allow bus controller 910 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller 910 also comprises slave read/write control (RD/WR Cntl) 914 and master read/write control (RD/WR Cntl) 915. RD/WR controls 914 and 915 are involved in the transfer of PCI control signals between bus controller 910 and the host PCI bus.

Bus controller 910 is coupled to translator 920. Translator 920 comprises encoders 922 and 927, decoders 923 and 928, control decoder & separate data path unit 924 and control encoder & merge data path unit 925. As discussed above encoders 922 and 927 are part of slave data unit 911 and master data unit 916, respectively, receive PCI address and data information from FIFOs 912 and 917, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmission on the XDBus. Similarly, decoders 923 and 928 are part of slave data unit 911 and master data unit 916, respectively, and format address and data information from receiver 940 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 925 receives PCI control signals from the slave RD/WR control 914 and master RD/WR control 915. Additionally, control encoder & merge data path unit 925 receives control signals from CPU CNTL & GPIO latch/driver 990, which is coupled to the CPU and north bridge (not shown in FIG. 9). Control encoder & merge data path unit 925 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 930, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XDBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand, is a data bit that represents a control signal. Control decoder & separate data path unit 924 receives control bits from receiver 940 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XDBus. Control decoder & separate data path unit 924 separates the control bits it receives from receiver 940 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals, all of which meet the relevant timing constraints.

Transmitter 930 receives multiplexed parallel address/data (A/D) bits and control bits from translator 920 on the AD[31:0] out and the CNTL out lines, respectively. Transmitter 930 also receives a clock signal from PLL 950. PLL 950 takes a reference input clock and generates PCK that drives the XDBus. PCK is asynchronous with the PCI clock signal and operates at 66 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XDBus may be used to interface two PCI or PCI-like buses operating at 66 MHz rather than 33 MHz or having 64 rather than 32 multiplexed address/data lines.

The multiplexed parallel AID bits and some control bits input to transmitter 930 are serialized by parallel to serial converters 932 of transmitter 930 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the

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XDBus. Other control bits are serialized by parallel to serial converter 933 into 10 bit packets and send out on control line PCN of the XDBus.

FIG. 10 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1000 is nearly identical to HIC 900 in its function, except that HIC 900 interfaces the host PCI bus to the XDBus while PIC 1000 interfaces the secondary PCI bus to the XDBus. Similarly, the components in PIC 1000 serve the same function as their corresponding components in HIC 900. Reference numbers for components in PIC 1000 have been selected such that a component in PIC 1000 and its corresponding component in HIC 900 have reference numbers that have the same two least significant digits. Thus for example, the bus controller in PIC 1000 is referenced as bus controller 1010 while the bus controller in HIC 900 is referenced as bus controller 910. As many of the elements in PIC 1000 serve the same functions as those served by their corresponding elements in HIC 900 and as the functions of the corresponding elements in HIC 900 have been described in detail above, the function of elements of PIC 1000 having corresponding elements in HIC 900 will not be further described herein. Reference may be made to the above description of FIG. 9 for an understanding of the functions of the elements of PIC 1000 having corresponding elements in HIC 900.

As suggested above, there are also differences between HIC 900 and PIC 1000. Some of the differences between HIC 900 and PIC 1000 include the following. First, receiver 1040 in PIC 1000, unlike receiver 940 in HIC 900, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 900 synchronizes the PCKR clock to the PCK clock locally generated by PLL 950. PIC 1000 does not locally generate a PCK clock and, therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 900. Another difference between PIC 1000 and HIC 900 is the fact that PIC 1000 contains a video parallel to serial converter 1089 whereas HIC 900 contains a video serial to parallel converter 980. Video parallel to serial converter 1089 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0:15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. 10) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1000, unlike HIC 900, contains a clock doubler 1082 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1082 through buffer 1083 and is sent to serial to parallel converter 980 through buffer 1084. Additionally, reset control unit 1035 in PIC 1000 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1090 and transmits the reset signal on the RESET# line to the HIC 900 whereas reset control unit 945 of HIC 900 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 990 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1000 to the HIC 900.

Like HIC 900, PIC 1000 handles the PCI bus control signals and control bits from the XDBus representing PCI control signals in the following ways:

1. PIC 1000 buffers clocked control signals from the secondary PCI bus, encodes them and sends the encoded control bits to the XDBus;
2. PIC 1000 manages the signal locally; and

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3. PIC 1000 receives control bits from XPBus, translates them into PCI control signals and sends the PCI control signals to the secondary PCI bus.

PIC 1000 also supports a reference arbiter on the secondary PCI Bus to manage the PCI signals REQ# and GNT#.

FIG. 11 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 11, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 11 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e. PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 11, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a pair of physical lines together transmit a signal in a bit line or bit channel in an LVDS or IEEE 1394 interface.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

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FIG. 12 is a block diagram of another embodiment of the HIC and PIC of the present invention and the interface therebetween. One important difference is the fact that the XPBus of FIG. 12 does not have control lines PCN and PCNR. Another difference lies in the fact that the XPBus of FIG. 12 has two dedicated reset lines RSTEH# and RSTEP# instead of one. RSTEH# and RSTEP# are unidirectional reset and error condition signal lines that transmit a reset and error condition signal from the host PCI to the peripheral PCI and from the peripheral PCI to host PCI, respectively.

In one embodiment, each of reset lines RSTEH#, RSTEP#, and RESET# (previously discussed) is preferably a non-differential signal line of one physical line. In other embodiments, one or more of the above lines may be a differential signal line having more than one physical line.

FIG. 13 shows a detailed block diagram of the HIC shown in FIG. 12. HIC 1300 shown in FIG. 13 is, other than for a few differences, identical to HIC 900 shown in FIG. 9. Accordingly, reference numbers for components in HIC 1300 have been selected such that a component in HIC 1300 and its corresponding component in HIC 900 have reference numbers that have the same two least significant digits. One of the differences between HIC 1300 and HIC 900 is the fact that, unlike HIC 900, HIC 1300 does not have a parallel to serial converter or a serial to parallel converter dedicated exclusively to CNTL out and CNTL in signals, respectively. This is due to the fact that XPBus for HIC 1300 does not contain a PCN or PCNR line. Another difference between HIC 1300 and HIC 900 is the fact that HIC 1300, unlike HIC 900, has two reset lines, RSTEP# and RSTEH#, instead of one reset line. Reset line RSTEP# is coupled to Reset & XPBus Parity Error Control Unit 1336 which receives, on the reset line RSTEP#, a reset signal and a parity error signal generated by the PIC, sends a reset signal to the CPU CNTL & GPIO latch/driver 1390, and controls retransmission of bits from the parallel to serial converters 1332. Reset & XPBus Parity Error Detection and Control Unit 1346 takes bits from serial to parallel converters 1342, performs a parity check to detect any transmission error, and sends reset and parity error signals to the PIC on the reset line RSTEH#. The reset and parity error signals may be distinguished by different signal patterns and/or different signal durations. In the two reset line system, the reset and error parity signals are transmitted on the same line, and it is possible to send a parity error confirmation signal on one line while receiving a reset signal on the other line. Because HIC 1300 provides for parity error detection, the parallel to serial converters 1332 include buffers. The buffers in parallel to serial converters 1332 store previously transmitted bits (e.g., those transmitted within the previous two clock cycles) for retransmission if transmission error is detected and a parity error signal is received on line RSTEP#. It is to be noted that parallel to serial converters 932 do not contain buffers such as those contained in parallel to serial converters 1332 for purposes of retransmission since HIC 900 does not provide for parity error signal detection. Yet another difference between HIC 900 and HIC 1300 is the fact that in HIC 1300 clock multipliers 1331 and 1341 multiply the PCK and PCKR clocks, respectively, by a factor of 6 rather than 10 because the XPBus coupled to HIC 1300 transmits six bit packets instead of ten bit packets during each XPBus clock cycle. Sending a smaller number of bits per XPBus clock cycle provides the benefit of improving synchronization between the data latching clock output by clock multipliers 1331 and 1341 and the XPBus clocks, PCK and PCKR. In another embodiment, one may send 5 or some other number of bits per XPBus clock cycle. As mentioned above, the remaining elements in HIC 1300 are identical to those in HIC 900 and reference to

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the description of the elements in HIC 900 may be made to understand the function of the corresponding elements in HIC 1300.

FIG. 14 is a schematic diagram of the lines PCK and PD0 to PD3. These lines are unidirectional LVDS lines for transmitting signals from HIC 1300 to the PIC of FIG. 12. Another set of lines, namely PCKR and PDR0 to PDR3, are used to transmit clock signals and bits from the PIC of FIG. 12 to HIC 1300. The lines used for transmitting information from the PIC to HIC 1300 have the same structure as those shown in FIG. 14, except that they transmit information in the opposite direction from that shown in FIG. 14. In other words they transmit information from the PIC to the HIC.

In the embodiment shown in FIG. 8, HIC 819 is coupled to an integrated unit 821 that includes a CPU, a cache and a north bridge. In yet another embodiment, such as that shown in FIG. 15, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1505 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1510 includes a PIC and a south bridge.

The above embodiments are described generally in terms of hardware and software. It will be recognized, however, that the functionality of the hardware can be further combined or even separated. The functionality of the software can also be further combined or even separated. Hardware can be replaced, at times, with software. Software can be replaced, at times, with hardware. Accordingly, the present embodiments should not be construed as limiting the scope of the claims here. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

1. A computer [module, said module] system comprising:
  - a console comprising
    - a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and
    - an interface controller coupled to said first LVDS channel; and
  - a computer module comprising
    - an enclosure, said enclosure being insertable into [a] said console;
    - a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;
    - an integrated interface controller and bridge unit to communicate encoded address and data of Peripheral Component Interconnect ("PCI") bus transaction, said integrated interface controller and bridge unit directly coupled to said central processing unit without any intervening PCI bus;
    - a second LVDS channel extending directly from said integrated interface controller and bridge unit to convey said encoded address and data of PCI bus transaction, said second LVDS channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions;
    - a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit; and
    - a programmable memory device in said enclosure, said programmable memory device being configurable to

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store a password for preventing a possibility of unauthorized use of said hard disk drive.

[2. The computer module of claim 1 further comprising a host interface controller for providing a status of a locking device in said enclosure.]

[3. The computer module of claim 1 further comprising a mechanical locking device that is coupled to said programmable memory device.]

[4. The computer module of claim 1 further comprising a host interface controller coupled to a mechanical locking device, said host interface controller being coupled to said programmable memory device.]

5. The computer [module] system of claim 1 wherein said programmable memory device comprises a flash memory device.

[6. The computer module of claim 1 wherein said programmable memory device comprises a flash memory device having at least 8 Mbits of cells and greater.]

[7. The computer module of claim 1 further comprising a security program in a main memory.]

[8. The computer module of claim 7 wherein said security program comprises a code for storing a password on said programmable memory device.]

[9. The computer module of claim 8 wherein said security program comprises a code for checking a time from said real-time clock circuit.]

[10. The computer module of claim 1 further comprising a host interface controller coupled to a solenoid that drives a mechanical lock in a first position to a second position.]

[11. The computer module of claim 10 wherein said solenoid also drives said mechanical lock from said second position to said first position.]

[12. The computer module of claim 1 further comprising a real-time clock circuit coupled to said central processing unit.]

[13. The computer module of claim 12 further comprising a battery coupled to a host interface controller that includes said real-time clock.]

14. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console of a modular computer system, said console comprising a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, multiple serial bit channels to transmit encoded address and data of Peripheral Component Interconnect ("PCI") bus transaction in opposite directions, said ACM comprising

a microprocessor unit coupled to a mass memory storage device including a plurality of application software program files;

an integrated interface controller and bridge unit directly coupled to said microprocessor unit without any intervening PCI bus; and

a second LVDS channel extending directly from said integrated interface controller and bridge unit, said second LVDS channel comprising at least two unidirectional, serial bit channels to transmit data in opposite directions;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and prompting for a user password from a user on a display.

[15. The method of claim 14 wherein said ACM comprises an enclosure that houses said microprocessor unit and said mass memory storage device.]



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[16. The method of claim 14 further comprising providing a user password to said security program.]

17. The method of claim 14 [further comprising] wherein said mass memory storage device comprises a flash memory device [for storing a desired password for said ACM].

[18. The method of claim 17 wherein said flash memory device maintains said desired password when power is removed from said ACM.]

[19. The method of claim 18 wherein said flash memory device is coupled to a host interface controller that is coupled to said microprocessor based unit.]

[20. The method of claim 14 wherein said mass memory storage device comprises a code directed to comparing said user password with a desired password.]

[21. The method of claim 14 further comprising identifying a permanent password or user code on said attached computer module.]

[22. The method of claim 21 wherein said permanent password or user code is stored in said microprocessor unit.]

[23. The method of claim 21 wherein said permanent password or user code is stored in a flash memory device coupled to said microprocessor unit.]

24. A computer system comprising:

a console comprising a LAN communication device and a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, multiple serial bit channels to transmit encoded address and data of Peripheral Component Interconnect ("PCI") bus transaction in opposite directions;

a computer module comprising an enclosure insertable into said console to form a functional computer;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing a possibility of unauthorized use of said hard disk drive;

an integrated interface controller and bridge unit in said enclosure, said integrated interface controller and bridge unit directly coupled to said central processing unit without any intervening PCI bus; and

a second LVDS channel extending directly from said integrated interface controller and bridge unit, said second LVDS channel comprising at least two unidirectional, serial bit channels to transmit data in opposite directions;

wherein said integrated interface controller and bridge unit is configured to communicate to said console through said second LVDS channel and an interface connector.

25. The computer system of claim 24 further comprising a graphics accelerator in said enclosure.

26. The computer system of claim 24 wherein said first LVDS channel is configured to transmit said encoded address and data of PCI bus transaction in 10-bit packets.

27. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a modular computer system housed in a console, said console comprising a LAN communication device and a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, multiple serial bit channels to transmit encoded address and data

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of Peripheral Component Interconnect ("PCI") bus transaction in opposite directions, said ACM comprising

a graphics subsystem;

a microprocessor unit coupled to a mass memory storage device;

a peripheral bridge coupled to said microprocessor unit without any intervening PCI bus; and

a second LVDS channel extending directly from said peripheral bridge, said second LVDS channel comprising at least two unidirectional, serial bit channels to transmit data in opposite directions;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and

prompting for a user password from a user on a display.

28. The method of claim 27, further comprising transmitting said encoded address and data of PCI bus transaction in 10-bit packets through said first LVDS channel.

29. The method of claim 27 wherein said mass memory storage device comprises a flash memory device.

30. The method of claim 27 further comprising executing said security program to prevent unauthorized use of said mass memory storage device based on said user password.

31. The method of claim 27 further comprising executing said security program to manage an access privilege to data based on said user password.

32. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a modular computer system housed in a console, said console comprising an add-on card slot and a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, multiple serial bit channels to transmit encoded address and data of Peripheral Component Interconnect ("PCI") bus transaction in opposite directions, said ACM comprising a microprocessor unit coupled to a mass memory storage device comprising a plurality of application software program files;

an enclosure;

an integrated interface controller and bridge unit directly coupled to said microprocessor unit without any intervening PCI bus; and

a second LVDS channel extending directly from said integrated interface controller and bridge unit, said second LVDS channel comprising at least two unidirectional, serial bit channels to transmit data in opposite directions;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and

prompting for a user password from a user on a display, wherein data in said mass memory storage device is accessed by said microprocessor unit through said integrated interface controller and bridge unit.

33. The method of claim 32, further comprising transmitting said encoded address and data of PCI bus transaction in 10-bit packets through said first LVDS channel.

34. The method of claim 32 wherein said mass memory storage device comprises a flash memory.

35. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console of a modular computer system, said console comprising a LAN communication device, a removable storage media subsystem, and a first low

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voltage differential signal ("LVDS") channel comprising two unidirectional, serial channels to transmit encoded address and data of Peripheral Component Interconnect ("PCI") bus transaction in 10-bit packets, said ACM comprising

a microprocessor unit coupled to a mass memory storage device;

a peripheral bridge directly coupled to said microprocessor unit without any intervening PCI bus; and

a second LVDS channel extending directly from said peripheral bridge, said second LVDS channel comprising two unidirectional, serial bit channels to transmit data in opposite directions;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and

prompting for a user password from a user on a display.

36. The method of claim 35 wherein said mass memory storage device comprises a flash memory.

37. The method of claim 35 wherein said mass memory storage device comprises a hard disk drive.

38. A method for operating a computer system, said method comprising:

inserting an attached computer module ("ACM") into a bay of a console of a modular computer system, said console comprising a LAN communication device and a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, multiple serial bit channels to transmit encoded Peripheral Component Interconnect ("PCI") bus transaction address and data in opposite directions, said ACM comprising

a microprocessor unit coupled to a mass memory storage device;

a peripheral bridge directly coupled to said microprocessor unit without any intervening PCI bus; and

a second LVDS channel extending directly from said peripheral bridge, said second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

applying power to said computer system and said ACM to execute a security program, said security program being stored in said mass memory storage device; and

prompting for a user password from a user on a display.

39. The method of claim 38 wherein said mass memory storage device comprises a flash memory.

40. The method of claim 38 wherein said mass memory storage device comprises a hard disk drive.

41. A computer module, said module comprising:

an enclosure, said enclosure being insertable into a console of a modular computer system, said console comprising a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

a peripheral bridge to communicate address and data of Peripheral Component Interconnect ("PCI") bus transaction in an encoded, serial form, said peripheral bridge directly coupled to said central processing unit without any intervening PCI bus;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a second LVDS channel extending directly from said peripheral bridge to convey said address and data of PCI bus transaction in said encoded, serial form, said

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second LVDS channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing a possibility of unauthorized use of said hard disk drive.

42. The computer module of claim 41 wherein said second LVDS channel is configured to transmit data in 10-bit packets.

43. The computer module of claim 41 wherein said first LVDS channel couples to said second LVDS channel upon insertion of said computer module into said console.

44. A computer module, said module comprising:

an enclosure, said enclosure being insertable into a console of a modular computer system, said console comprising a first low voltage differential signal ("LVDS") channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a central processing unit in said enclosure, said central processing unit comprising a microprocessor based integrated circuit chip;

an integrated interface controller and bridge unit coupled to said central processing unit without any intervening Peripheral Component Interconnect ("PCI") bus;

a hard disk drive in said enclosure, said hard disk drive being coupled to said central processing unit;

a second LVDS channel extending directly from said integrated interface controller and bridge unit, said second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a programmable memory device in said enclosure, said programmable memory device being configurable to store a password for preventing a possibility of unauthorized use of said hard disk drive,

wherein said first LVDS channel couples to said second LVDS channel upon insertion of said computer module into said console.

45. The computer module of claim 44 wherein said console further comprises a power supply to supply power to said computer module upon insertion.

46. The computer module of claim 44 wherein said second LVDS channel is configured to transmit encoded address and data of PCI bus transaction in 10-bit packets.

47. The computer system of claim 1 wherein said integrated interface controller and bridge unit is configured to output said encoded address and data of PCI bus transaction as 10-bit packets.

48. The computer system of claim 47 wherein said hard disk drive is coupled to said central processing unit through said integrated interface controller and bridge unit.

49. The computer system of claim 26 wherein said integrated interface controller and bridge unit is configured to output a serial bit stream that is conveyed over said second LVDS channel as data packets.

50. The computer system of claim 49 wherein said serial bit stream comprises information of Universal Serial Bus protocol.

51. The computer system of claim 49 wherein said hard disk drive is coupled to said central processing unit through said integrated interface controller and bridge unit.

52. The computer module of claim 42 wherein said peripheral bridge is configured to output an encoded serial bit stream comprising said address and data of PCI bus transaction.

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53. The computer module of claim 52 wherein said encoded serial bit stream comprises information to permit decoding to create a PCI bus transaction.

54. The computer module of claim 53 wherein said hard disk drive is coupled to said central processing unit through said peripheral bridge.

55. The computer module of claim 54 wherein said peripheral bridge comprises a north bridge.

56. The computer module of claim 42 wherein said peripheral bridge comprises an interface controller to output said address and data of PCI bus transaction in said encoded, serial form, and said second LVDS channel extends directly from said interface controller.

57. The computer module of claim 56 wherein said interface controller is integrated with the peripheral bridge to form a single integrated unit.

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58. The computer module of claim 57 wherein said interface controller is directly coupled to said central processing unit without any intervening PCI bus.

59. The computer module of claim 44 wherein said integrated interface controller and bridge unit is configured to output an encoded serial bit stream that is conveyed over said second LVDS channel.

60. The computer module of claim 59 wherein said encoded serial bit stream is conveyed over said second LVDS channel as 10-bit packets.

61. The computer module of claim 59 wherein said hard disk drive is coupled to said central processing unit through said integrated interface controller and bridge unit.

62. The computer module of claim 59 wherein said encoded serial bit stream comprises information of Universal Serial Bus protocol.

\* \* \* \* \*





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(54) **DATA SECURITY METHOD AND DEVICE  
FOR COMPUTER MODULES**

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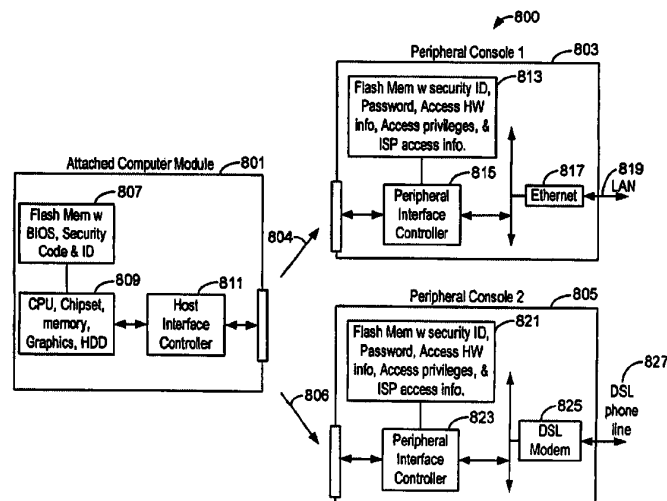
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(57) **ABSTRACT**

A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.

**53 Claims, 14 Drawing Sheets**



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"Exhibit 2, Disclosure of Asserted Claims and Infringement Contentions for Defendant ClearCube Technology, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 163 pages.

"Exhibit 3, Disclosure of Asserted Claims and Infringement Contentions for Defendant Dell Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 184 pages.

"Exhibit 4, Disclosure of Asserted Claims and Infringement Contentions for Defendant Fujitsu America, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 210 pages.

"Exhibit 7, Disclosure of Asserted Claims and Infringement Contentions for Defendant NEC Corp. of America," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 166 pages.

"Exhibit 9, Disclosure of Asserted Claims and Infringement Contentions for Defendant Super Micro Computer, Inc.," submitted by the Plaintiff in the U.S. District Court for the Eastern District of Texas, Case No. 6:09-cv-148-LED, served on Sep. 14, 2009, 220 pages.

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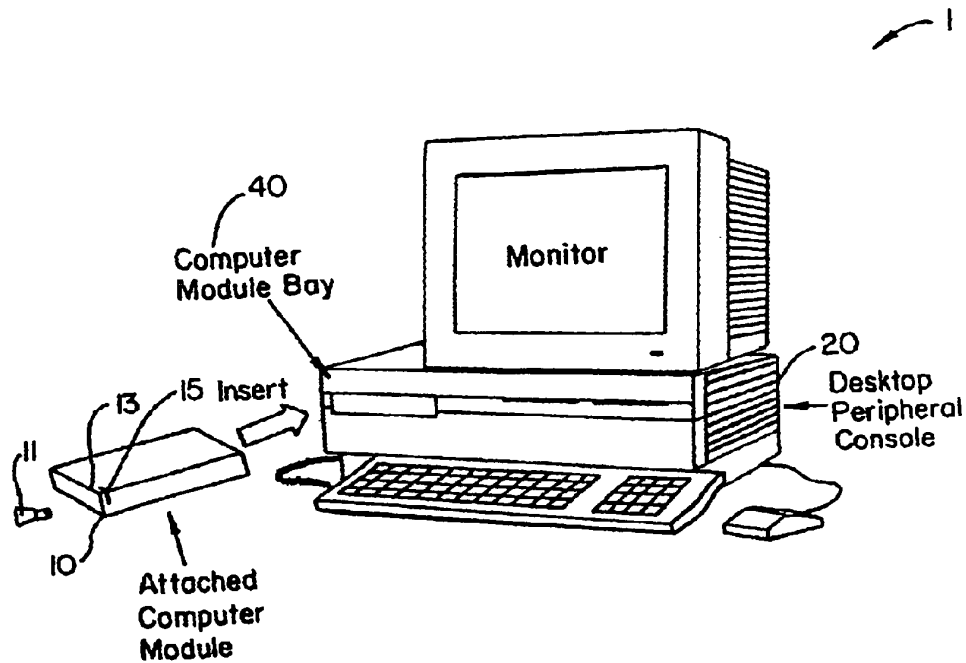


FIG. 1



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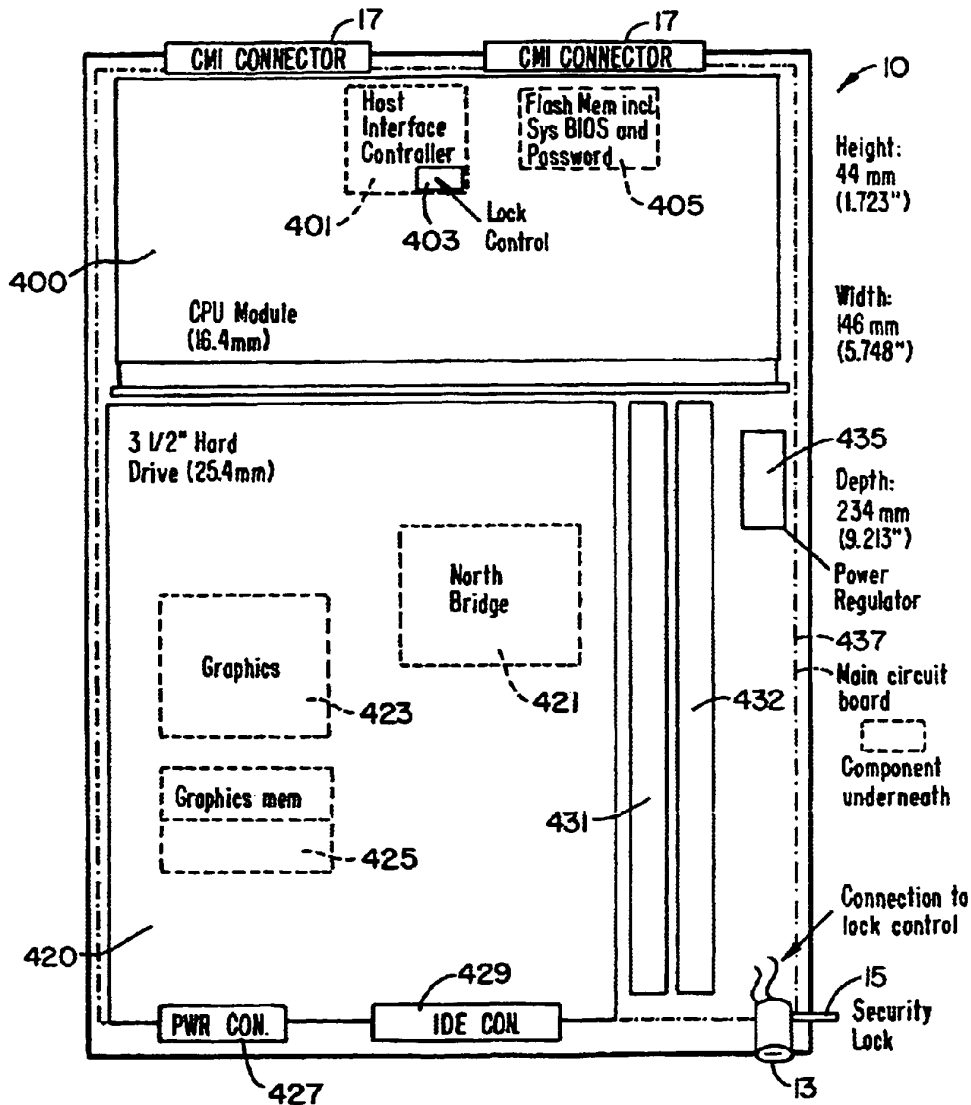


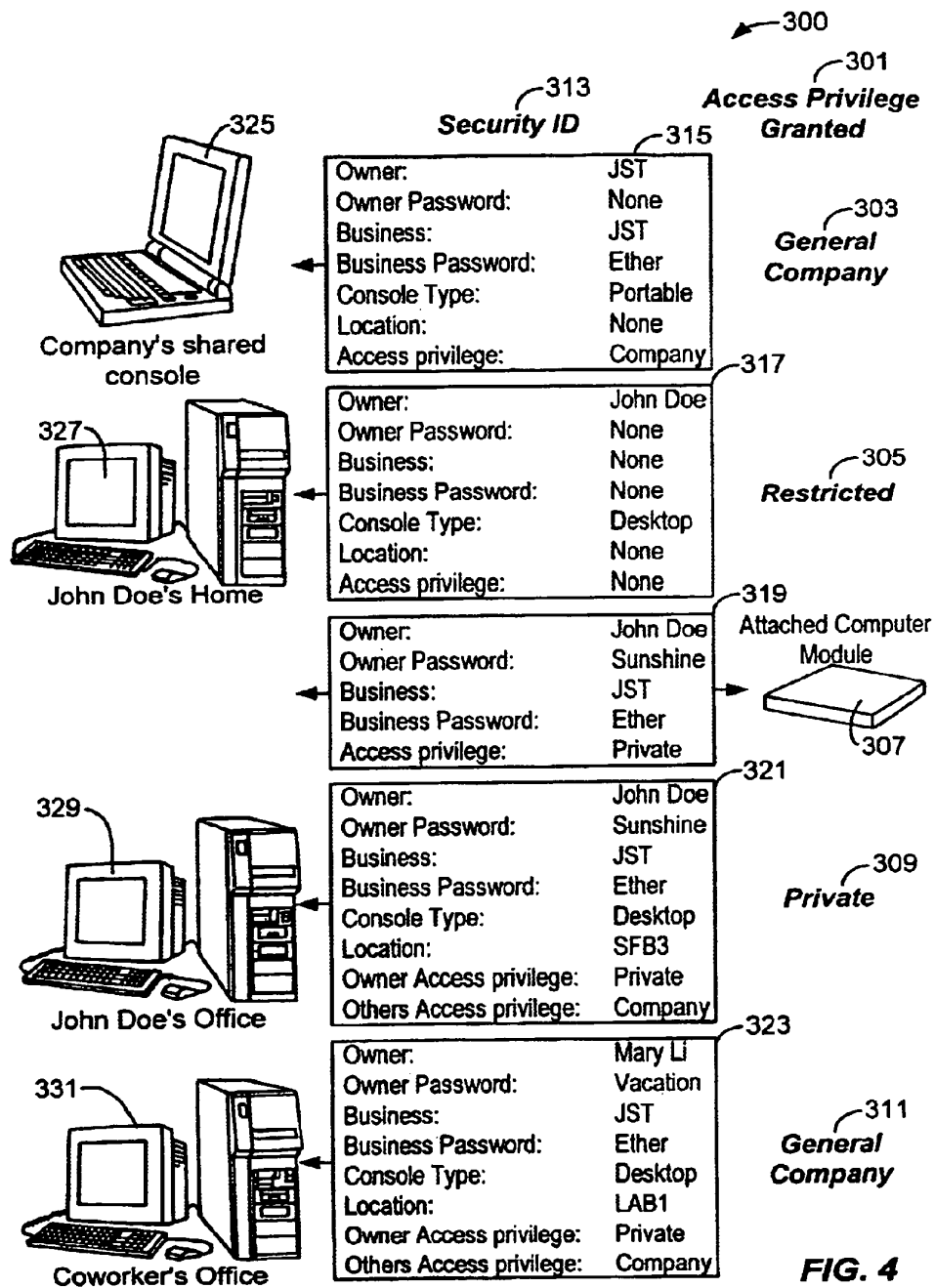
FIG. 3

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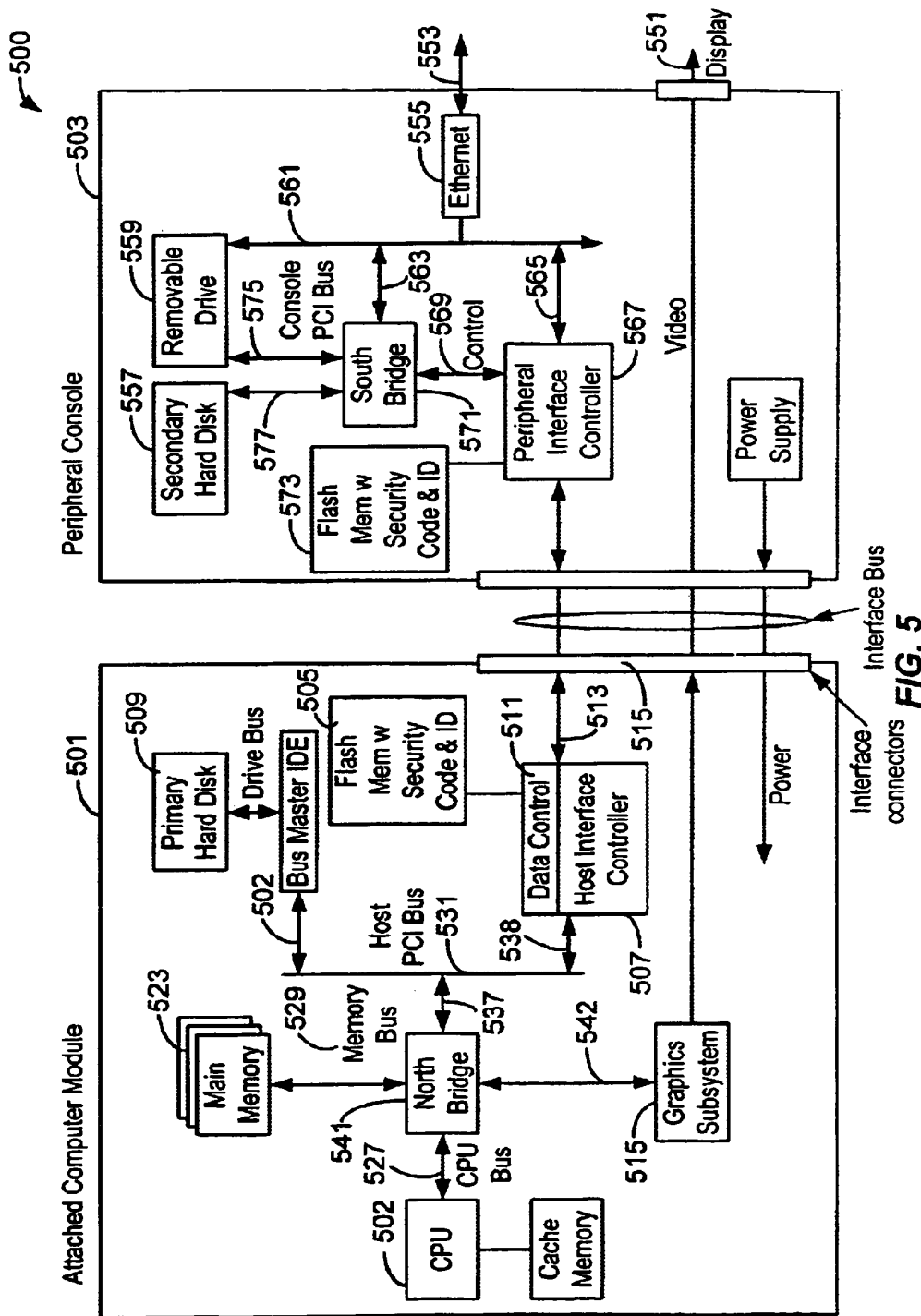


FIG. 5

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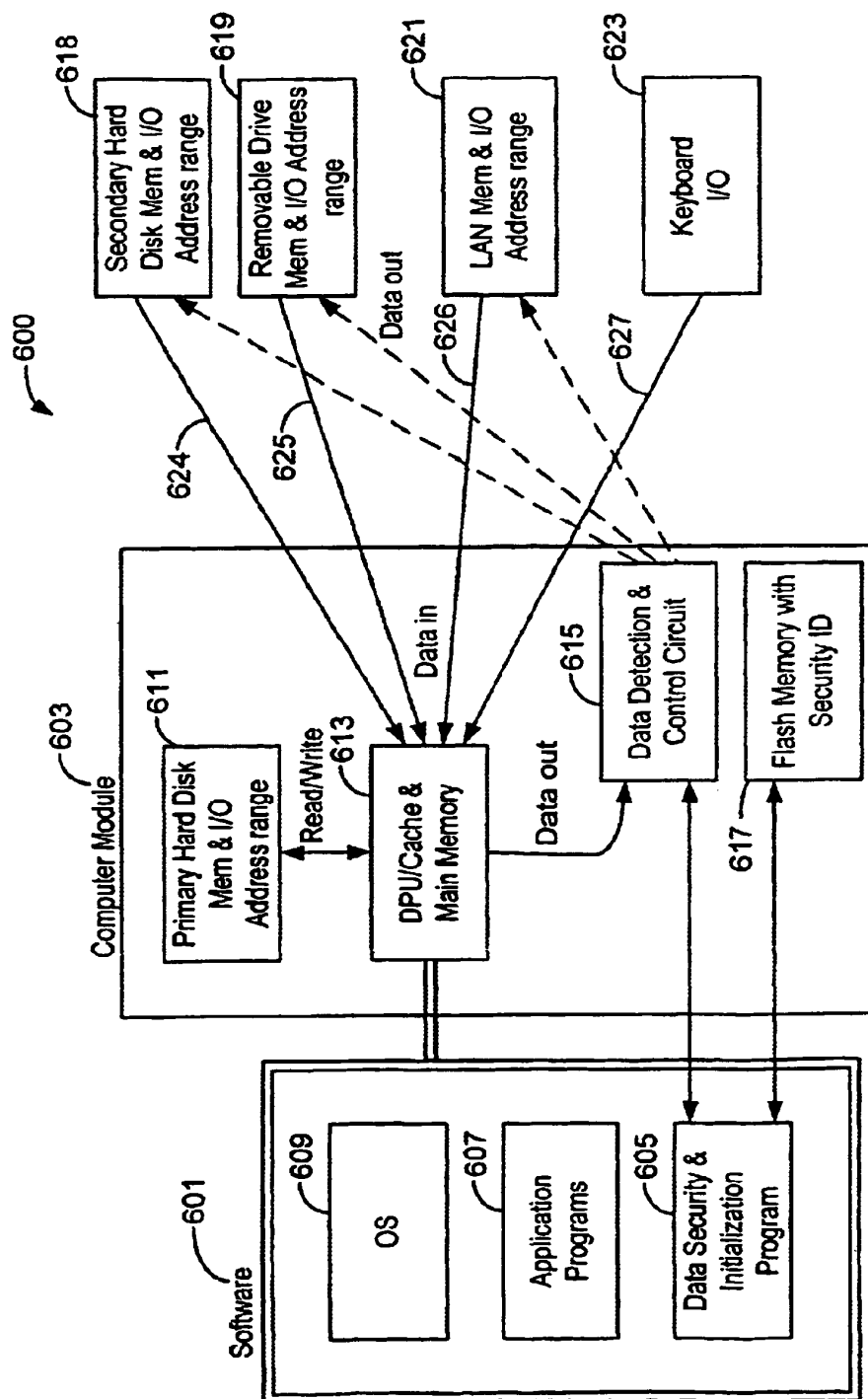


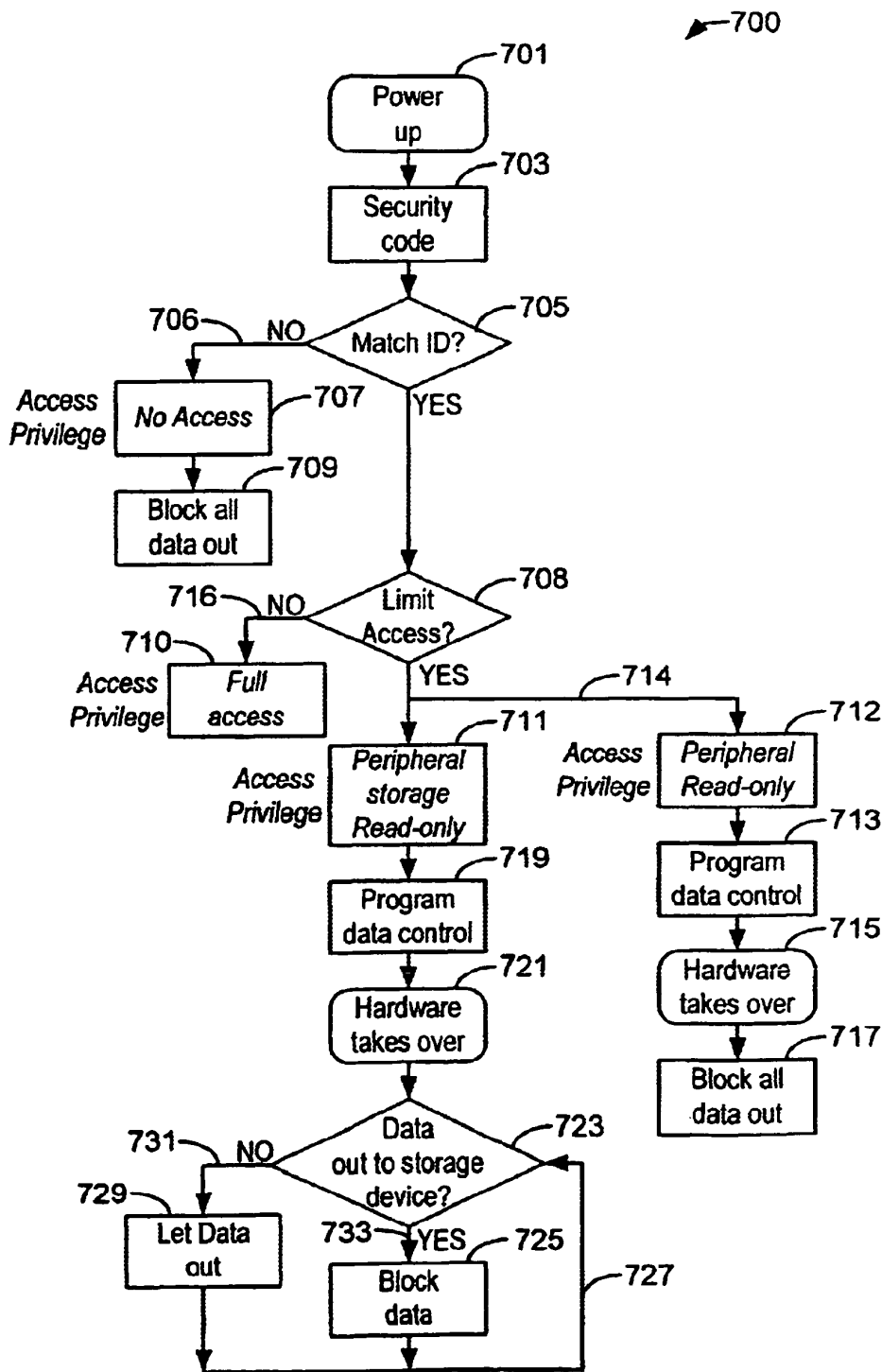
FIG. 6

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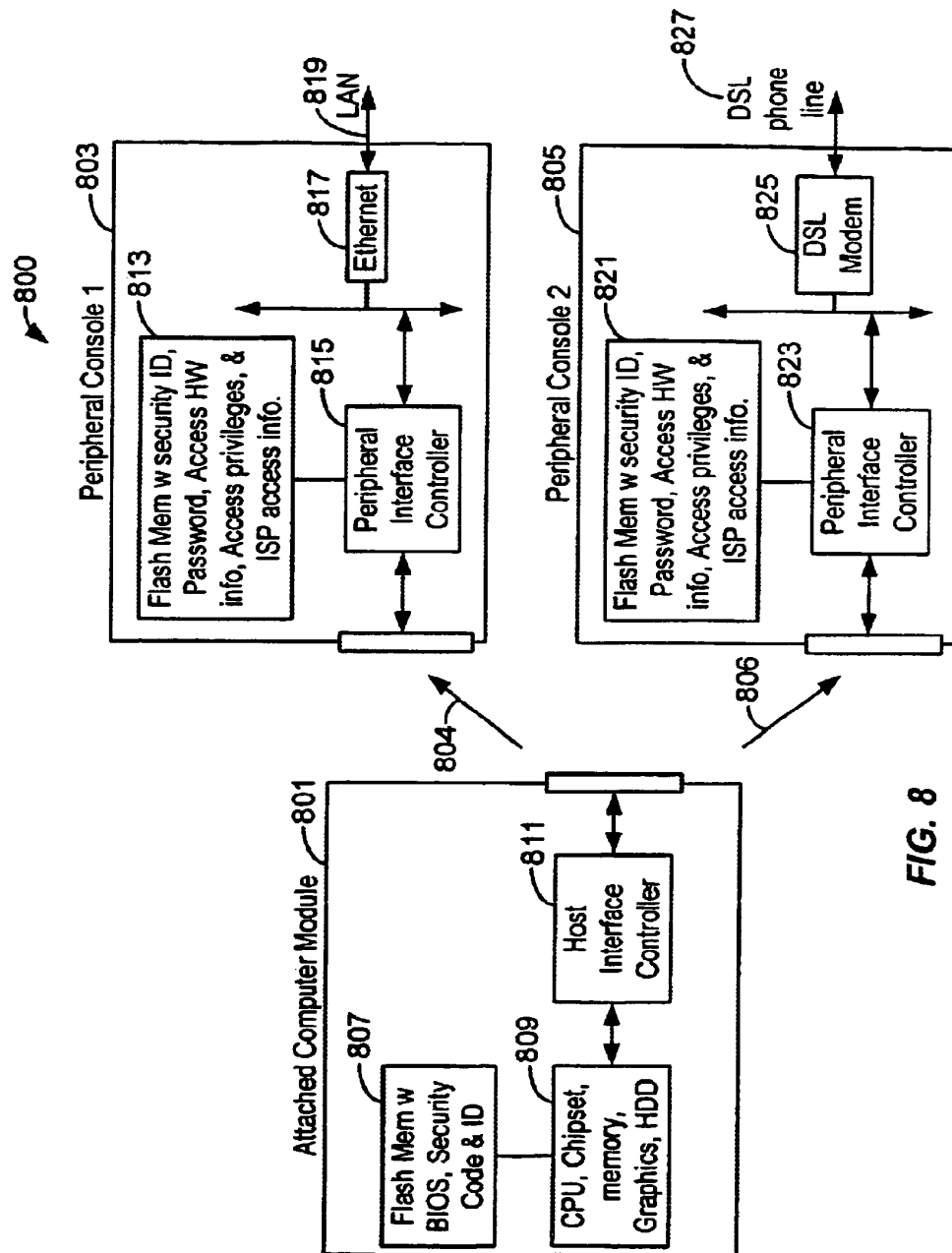


FIG. 8

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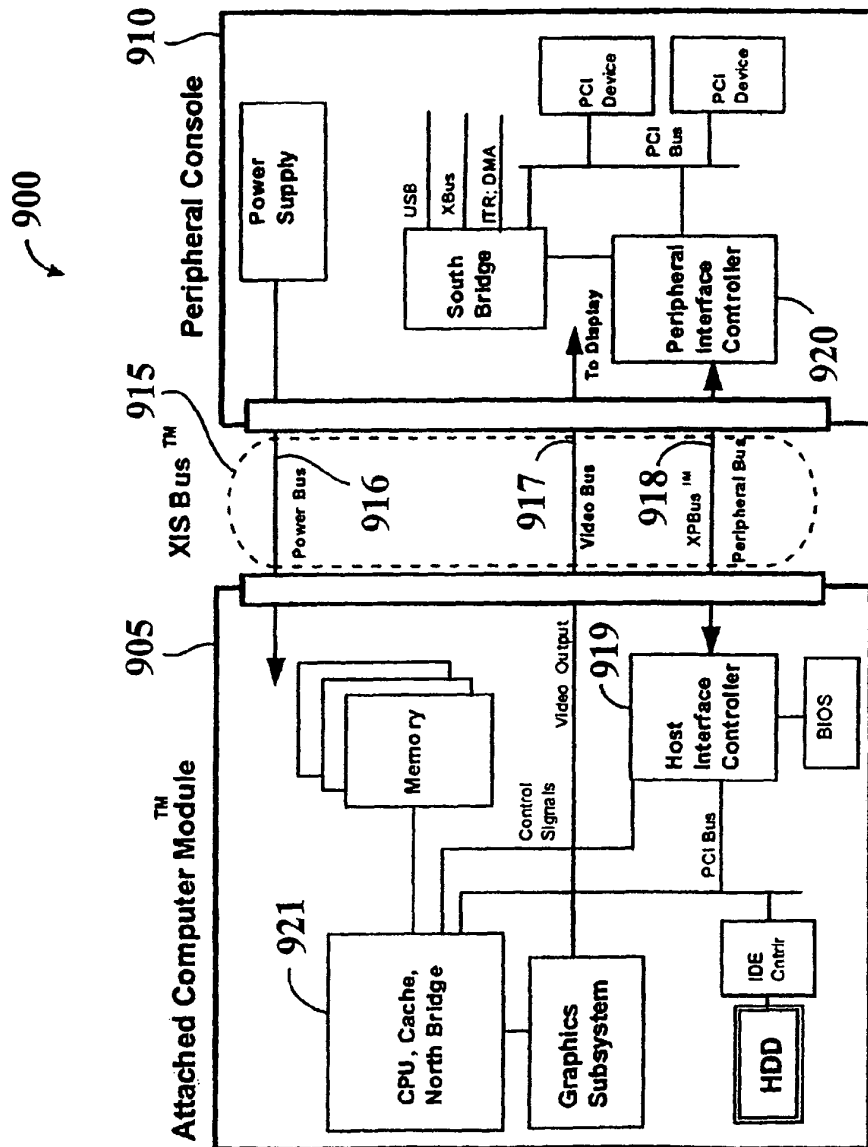


FIG. 9

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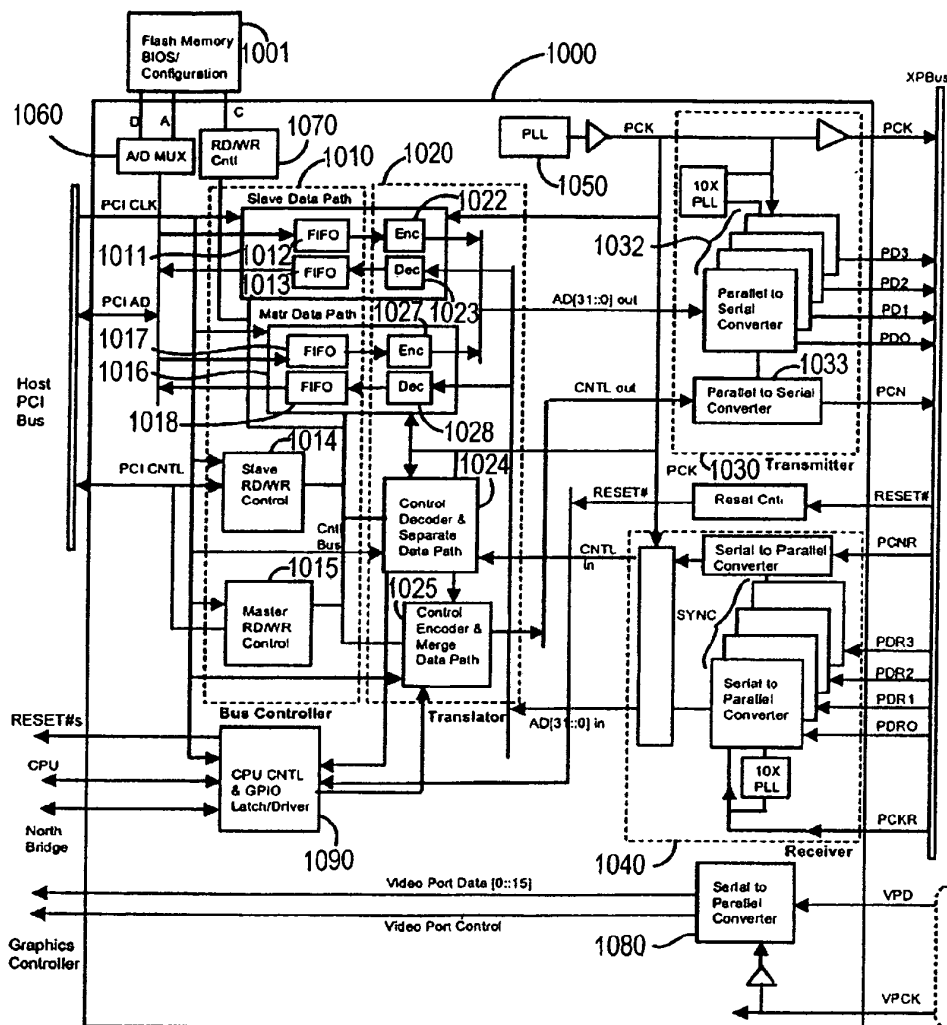


FIG. 10



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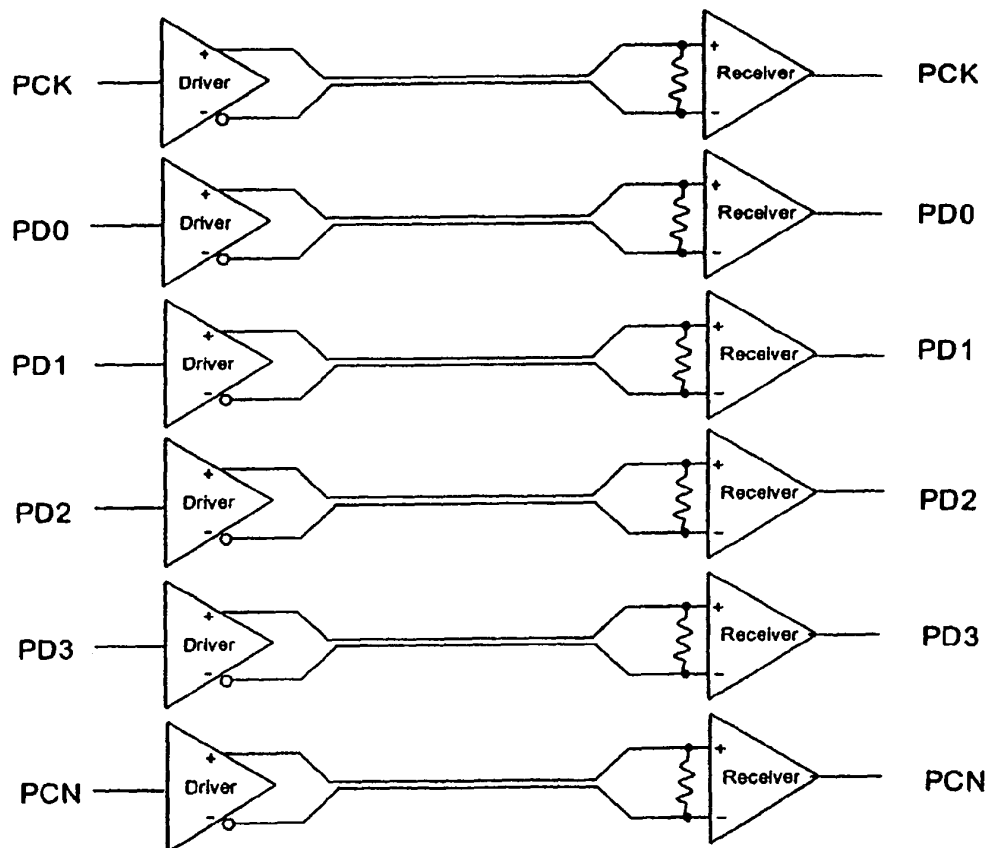


FIG. 11

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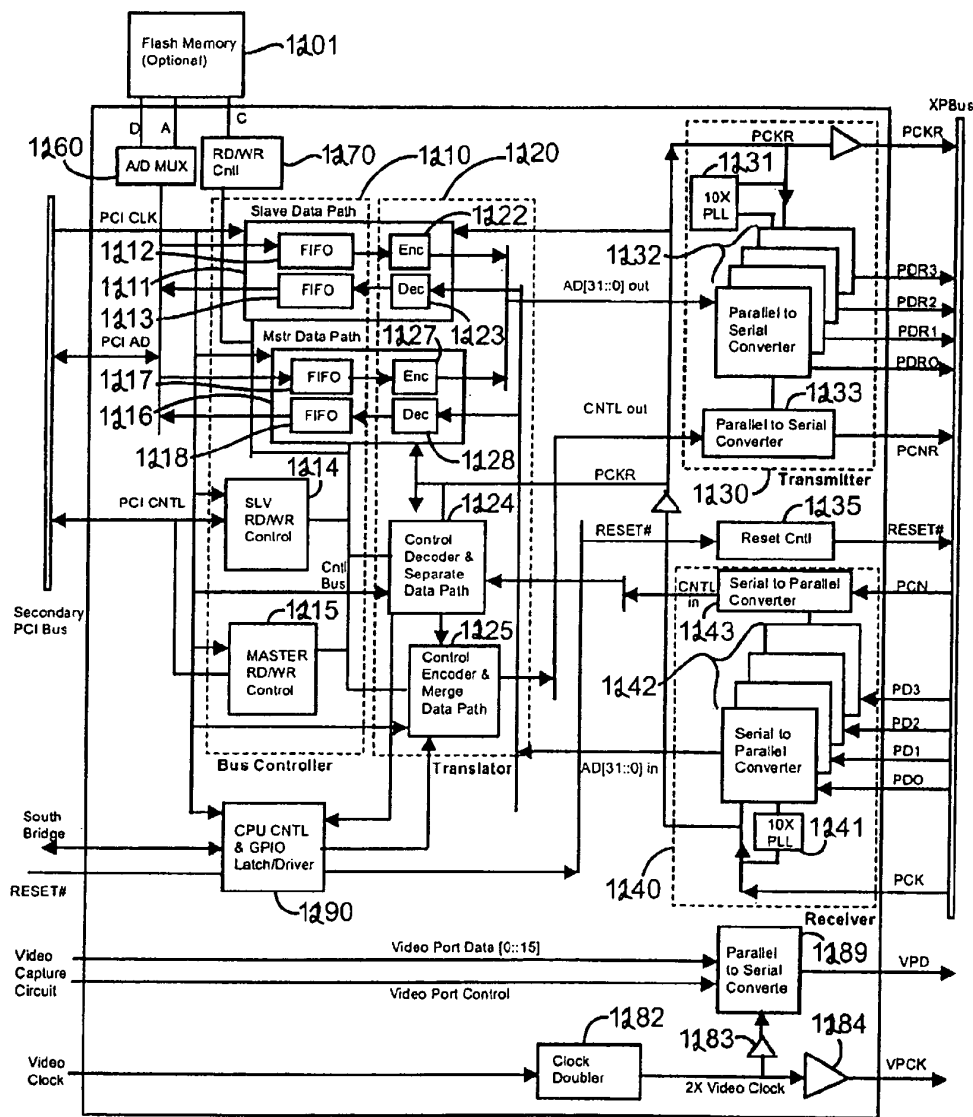


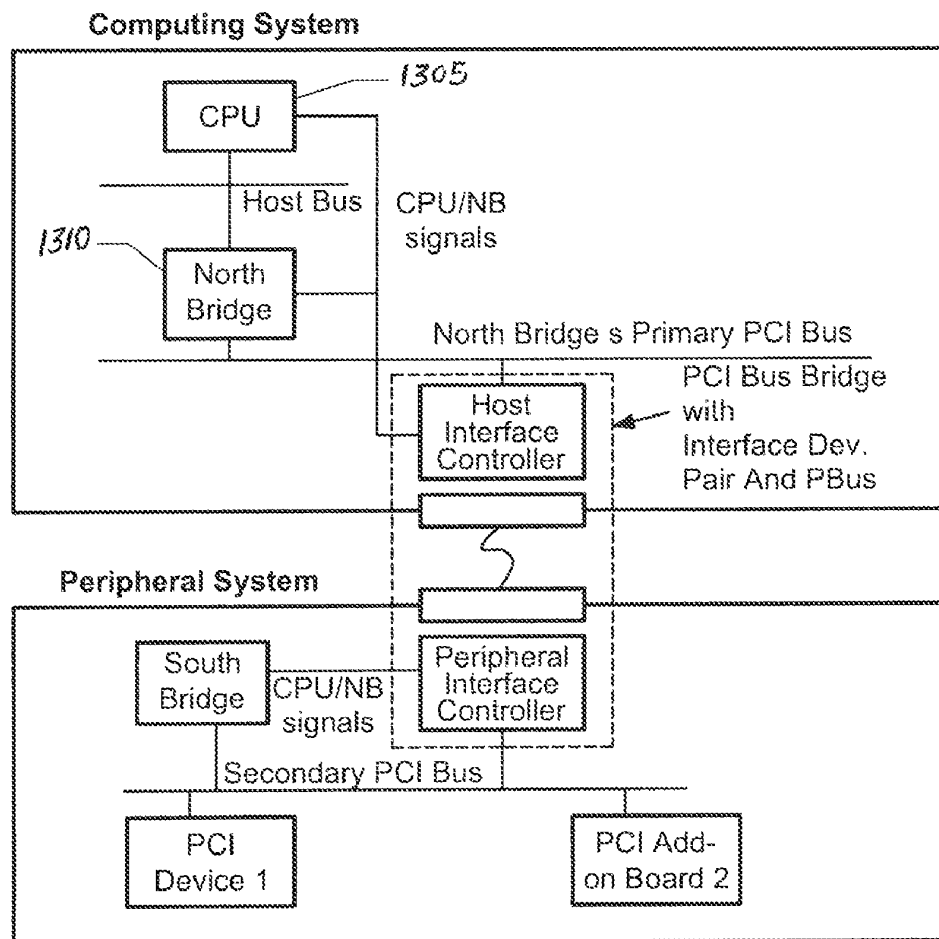
FIG. 12

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**FIGURE 13**

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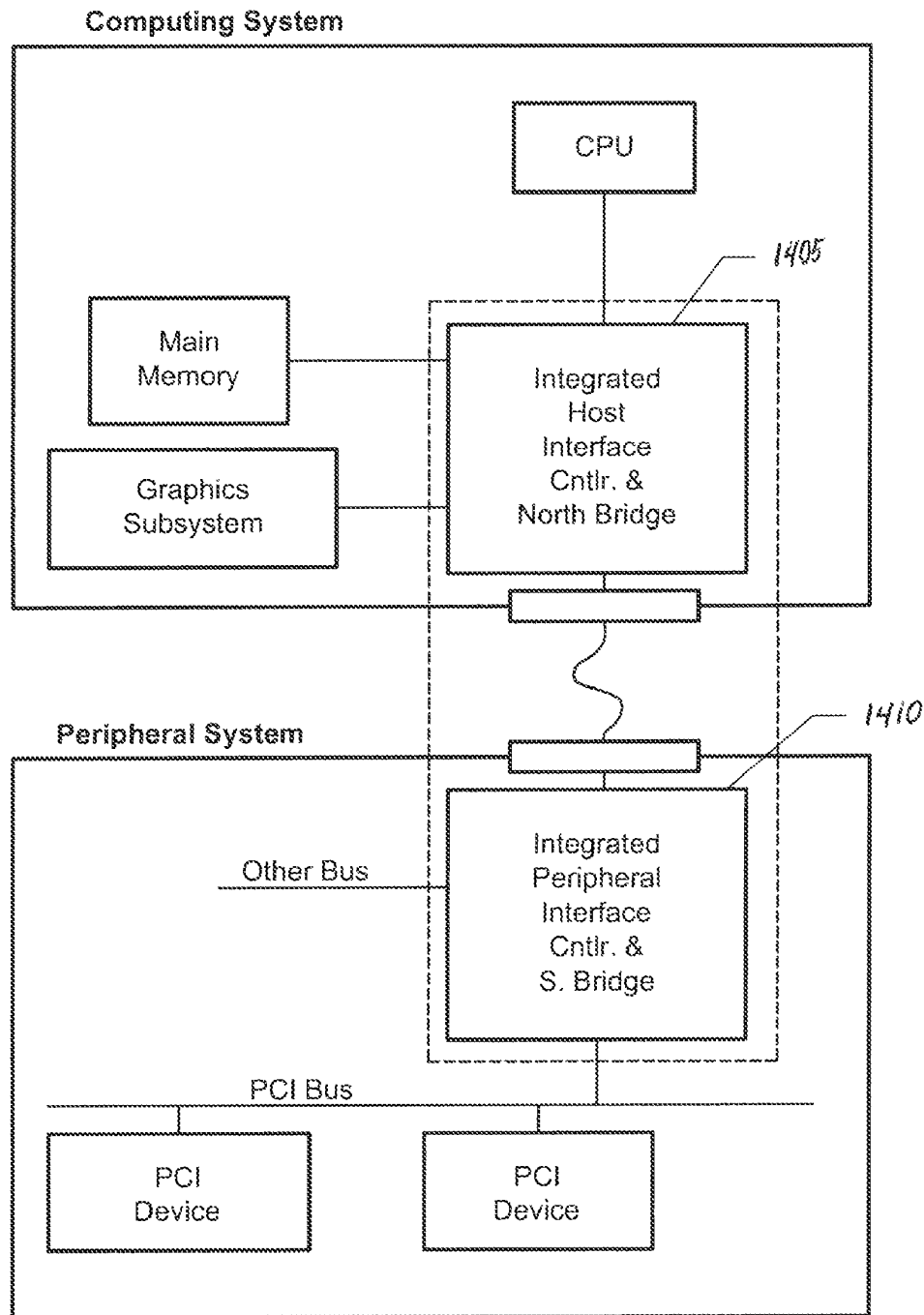


FIGURE 14

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## DATA SECURITY METHOD AND DEVICE FOR COMPUTER MODULES

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

*Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,643,777. The reissue applications are U.S. application Ser. Nos. 11/056,604 (a parent reissue application and now U.S. Pat. No. Re. 41,092), 11/545,056 (the present application, which is a continuation reissue of the parent reissue application), and 12/561,138 (which is a continuation reissue of the parent reissue application).*

*This application is a continuation reissue of U.S. application Ser. No. 11/056,604, which is a reissue of U.S. Pat. No. 6,643,777, which are incorporated herein by reference.*

### BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive including memory in the giga-byte range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 19 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many

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limitations. These computing devices have expensive display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals the are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have proprietary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

To date, most personal computers provide data file security through software only. A wide variety of removable storage media are available for a personal computer. These removable

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media do not provide any access security protection in hardware. Data encryption program often must be used for protection. Such program is cumbersome to handle for the user requiring extra cost and time. Data encryption is more commonly used for communication over an unprotected network or the Internet. Having a large number of frequently used files managed by encryption software is not practical. Without software security program, any file can be read and copied illegally from a hard disk drive on a PC or any removable media.

PC architecture generally allows freedom of data flow between memory and peripheral devices within the allowed memory and I/O address spaces. In conventional PC architecture, a peripheral bus, i.e. PCI bus, is used to control all data transactions among peripheral devices. PCI bus allows any device to be a bus master and perform data transaction with another device. Also when a software program is in control, it can move data between any two devices. There is no hardware or protocol security mechanism on a standard peripheral bus such as PCI Bus to detect or block data transactions. Operating system may have individual files read or write protected. These types of special security feature require significant additional user interaction to control. This is too cumbersome for a typical user to manage. There is no mechanism in current PCs to allow access to the primary hard disk drive and yet prevent copying of its content. The conventional PC is a single machine that does not have a mechanism to perform security ID matching in hardware.

Thus, what is needed are computer systems that provide improved security features to prevent illegal or unauthorized access to information.

## SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a computer module bay (CMB) within a peripheral console to form a functional computer. A security program reads an identification number in a security memory device to determine a security level of the ACM according to one embodiment.

In a specific embodiment, the present invention provides a system for secured information transactions. The system has a console (e.g., computer housing) comprising a peripheral controller housed in the console; and a security memory device (e.g., flash memory device) coupled to the peripheral controller. The system also has an attached computer module (i.e., a removable module with memory and microprocessor) coupled to the console. The attached computer module has a host interface controller housed within the attached computer module to interface to the security memory device through the peripheral controller.

In an alternative embodiment, the present invention provides a security protection method for a computer module. The method includes steps or acts of inserting the computer module into a console. Once the module has been inserted, the method initiates a security program in the module to read a security identification of the console and to read a security identification of the computer module. Based upon a relationship of the console identification and the computer module identification, a predetermined security status is determined from, for example, a look up table or the like. The method then

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selects the predetermined security status, which can be one of many. The method then operates the computer module based upon the security status.

In a further alternative embodiment, the present invention provides a method for identifying a user for a computer module. The method includes inserting a computer module into a console; and initiating a security program in memory of the computer module. The method prompts a plurality of input fields corresponding to respective input information on a user interface to be provided by a user of the computer module. Next, the method inputs the input information into the user interface of the computer module. The input information includes a user (e.g., owner) name, a user (e.g., owner) password, a business name, a business password, and a location.

Still further, the present invention provides a system for secured information transactions, e.g., data security, electronic commerce, private communications. The system includes a console comprising a peripheral controller housed in the console. A user identification input device (e.g., keyboard, retinal reader, finger print reader, voice recognition unit) is coupled to the peripheral controller. The user identification input device is provided for user identification data of the user. The system has an attached computer module coupled to the console. The attached computer module has a security memory device (e.g., flash memory device) stored with the user identification data.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified top-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified illustration of security systems according to embodiments of the present invention;

FIG. 5 is a simplified diagram of a computer module in a console according to an embodiment of the present invention;

FIG. 6 is a simplified diagram of a security method for a module according to an embodiment of the present invention; and

FIG. 7 is a simplified diagram of a method according to an embodiment of the present invention.

FIG. 8 is a simplified diagram of a system 800 according to an alternative embodiment of the present application.

FIG. 9 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 10 is a detailed block diagram of one embodiment of the host interface controller of the present invention.



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FIG. 11 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 12 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 13 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 14 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

#### DESCRIPTION OF THE SPECIFIC EMBODIMENTS

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 1 includes an attached computer module (i.e., ACM) 10, a desktop console 20, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, ACM 10 includes computer components, as will be described below, including a central processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 40 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM 10. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending U.S. patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998 commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking system includes at least a key 11. The key 11 mates with key hole 13 in a lock, which provides a mechanical latch 15 in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the FIG. below.

FIG. 2 is, a simplified diagram of a computer module 10 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. The computer module 10 includes key 11, which is insertable into keyhole 13 of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening 14, which allows the latch to move into and out of the ACM. The ACM also has

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openings 17 in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. 3 is a simplified top-view diagram 10 of a computer module for computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 10, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 400, and a second portion, which includes a hard drive module 420. A common printed circuit board 437 houses these modules and the like. Among other features, the ACM includes the central processing unit module 400 with a cache memory 405, which is coupled to a north bridge unit 421, and a host interface controller 401. The host interface controller includes a lock control 403. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 17. Here, the CPU module is spatially located near connector 17.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 401 is coupled to BIOS/flash memory 405. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 403 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 420. Among other elements, the hard drive module includes north bridge 421, graphics accelerator 423, graphics memory 425, a power controller 427, an IDE controller 429, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus 431, 432. A power regulator 435 is disposed near the PCI bus.

In a specific embodiment, north bridge unit 421 often couples to a computer memory, to the graphics accelerator 423, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator 423 typically couples to a graphics memory 423, and other elements. IDE controller 429 generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, USB, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit 420 typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT,

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MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module 420 includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit 240 may also support other interfaces than IDE.

In a specific embodiment, the present invention provides a file and data protection security system and method for a removable computer module or ACM. ACM contains the primary hard disk drive (HDD) where the operating system, application programs, and data files reside. The security system is used to prevent illegal access and copying of any file residing on the HDD inside ACM. An ACM is a self-contained computing device that can be armed with security software and hardware to protect its owner's private files and data. ACM docks with a computer bay in a wide variety of peripheral consoles. The combined ACM and peripheral console function as a personal computer. A computer module interface bus connects ACM and peripheral device. In some embodiments, all ACM data passes through computer module interface (CMI) bus to reach any device in the peripheral console, i.e. floppy drive, removable media, secondary hard disk drive, modem, and others. CMI bus data transfer is controlled by a pair of interface controllers on either side of the bus. This partitioning of a personal computer offer a way of protecting against illegal access of data residing within ACM by guarding data transaction through the computer module interface bus.

In a specific embodiment, a secured ACM has an enclosure that includes the following components:

- 1) ACPU,
- 2) Main memory,
- 3) A primary Hard Disk Drive (HDD),
- 4) Operating System, application software, data files on primary HDD,
- 5) Interface circuitry and connectors to peripheral console,
- 6) Flash memory used for storing security code and ID,
- 7) Data detection and control circuitry to manage data flow to peripheral console,
- 8) Circuit board connecting the above components, and others.

A peripheral console includes some of the following elements:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. CRT monitor, or integrated LCD display,
- 3) Removable storage media subsystem, e.g. Floppy drive, CDROM drive,
- 4) Communication device, e.g. LAN or modem,
- 5) Computer Module Bay, interface device and connectors to ACM,
- 6) Flash memory with security ID,
- 7) Power supply or battery system, and other devices.

The Computer Module Bay (CMB) is an opening in a peripheral console that receives ACM. CMB provides mechanical protection and electrical connection to ACM. The Computer Module Interface bus is made up of 3 bus components: video bus, peripheral data bus, and power bus. Video Bus consists of video output of graphics devices, i.e. analog RGB and control signals for monitor, or digital video signals to drive flat panel displays. Power bus supplies the power for ACM. Peripheral data bus is a high speed, compressed,

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peripheral bridge bus managed by a Host Interface Controller in ACM and a peripheral Interface Controller in peripheral console. In some embodiments, all peripheral data transaction passes through the interface controllers.

The implementation of the secured ACM generally includes the following elements:

- 1) A programmable Flash memory controlled by the Peripheral Interface Controller containing the security ID for the peripheral console,
- 2) A programmable Flash memory controlled by the Host Interface Controller containing hardware specific security code and ID for the computer module,
- 3) A data detection and control circuitry within Host Interface Controller to detect and manage data going out of ACM, and
- 4) A low level hardware dependent security code to perform security ID matching, hardware programming to manage data flow,
- 5) A high-level security program to manage user interface, program security ID, program security level, and other functions.

The hardware and software implementation allow more flexibility in the level of security protection offered to an ACM owner. Some examples of security levels are:

- 1) No access—Security IDs do not match according to owner's requirement. The Host Interface Controller blocks all peripheral data traffic between ACM and peripheral console except for keyboard and mouse,
- 2) Peripheral Read-only—No files can be written to any peripheral devices. All peripheral devices in peripheral console are managed as Read-only devices. The primary hard disk drive in ACM can be accessed freely,
- 3) Limited access—Certain peripheral devices are allowed read/write access, i.e. modem, and other devices are Read-only, i.e. removable media devices,
- 4) Full access—No restriction, and others.

Upon power up, the low level security code is executed to compare security ID between the respective flash memory between ACM and peripheral console. Typical security ID can include:

- 1) User ID
- 2) User password
- 3) User Access privilege
- 4) Business ID
- 5) Business password
- 6) Equipment ID
- 7) Equipment access privilege, and any other security IDs.

The user through the security program can activate different levels of password protection, which can be stored in a look up table. The company through the security program can control different levels of access privilege of a user, a business group, or equipment. The security code then program the security level allowed by the access privilege determined by the security ID matching result. For example, if an unidentified peripheral console is detected upon power up by the low level security code, e.g. a home unit, the access privilege can set to Peripheral Read-only. With Read-only access privilege for all peripheral devices in peripheral console, the data detection and control circuitry is programmed to monitor all data traffic going to the peripheral console. Any memory block transfer to peripheral console will be detected and blocked. Under this mode, a user can use the computer with free access to the primary HDD in ACM. Any files can be read from other storage media in the peripheral console. But no files from the primary HDD can be copied to another media.

The data detection circuitry separately monitors peripheral bus operation type and memory address range being

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accessed. A specific address range for memory accesses and for I/O accesses can be programmed for the data detection circuitry to flag a match. A data blocking circuitry is triggered by the detection circuitry when a match occurs, and blank out the data that is being sent to the peripheral console. For the security system to be effective, a [temper] tamper resistant enclosure must be used to prevent removal of the hard disk drive and the flash memory inside ACM. Further details are shown throughout the present specification and more particularly below.

FIG. 4 is a simplified illustration of security systems 300 according to embodiments of the present invention. This illustration is merely an example, which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The systems show various examples of ways to implement the present invention. Here, a user relies upon certain consoles to access information. A company's shared portable console 325 can access general company information 303. Selected security identification information 315 is entered into the shared console to access the information via a network. The information generally includes owner, owner password, business, business password, console type, location, and access privilege information, which is displayed on a user display. The owner is generally the user name. Owner password is the user password. The business is the business unit name and business password is the business unit password. The console type can be portable for laptops, notebooks, and the like. Alternatively, the console type can be a desktop. The location generally specifies the desktop location or address for a networked system. Alternatively, the location can also be a home location. Access privilege can be categorized into many different levels. For example, the user can access general company information, but not information directed to other business units. The user can also be limited to access his/her private information, which is company related. Many other types of information can be restricted or accessed depending upon the embodiment.

Other types of access can be granted depending upon the consoles. For example, various consoles include, among others, a console at a user's home, e.g., "John Doe's," a console in the user's office 329, a console in a co-worker's office 331, which the user can access. The access from John Doe's home console uses security identification 317 and provides restricted access 305. The user's use of the module 307 can be from a variety of consoles and is accessed using security identification 319. Here, access privilege is private, which allows the user to access private personal information or private company information that the user has created. The user's access from his office relies upon security identification 321, which grants access to private information and general company information. The co-worker's console can also be used with security identification 323, which allows the user to access general company information but not private information of John Doe, for example. Depending upon the console used by the user, the security system can provide partial or full access to information on servers via network as well as an attached computer module. Information can also be limited to read only for certain information sources such as a server, a hard drive, a floppy drive, and others.

In a specific embodiment, the present invention also provides a security feature for the ACM 307. Here, the user of the ACM can be granted access to information in the ACM if the correct security identification information 319 is provided to the combination of ACM and console. Once the correct information is provided, the user can access the information on the

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hard drive of the ACM, which can be for private use. Other levels of access and security can also be provided depending upon the application.

FIG. 5 is a simplified diagram 500 of a computer module in a console according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 500 includes an attached computer module 501 and a peripheral console 503, as well as other elements as desired. These elements have a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram 500 illustrates attached computer module 501. The module 501 has a central processing unit 502, which communicates to a north bridge 541, by way of a CPU bus 527. The north bridge couples to main memory 523 via memory bus 529. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 515 via bus 542. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive 509 that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2 1/2 inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines 502 and 531. The hard disk drive controller couples to the north bridge by way of the host PCI bus 531, which connects bus 537 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device 505 with a BIOS. The flash memory device 505 also has codes for a user password that can be stored in the device. The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 512 kilobits or greater of memory, or 1 megabits or greater of memory. The flash memory device can store a security identification number or the like. The flash memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The flash memory generally has at least 128 kilobits storage cells or more. The flash memory can be any product such as a W29C020 product made by a company called Winbond of Taiwan, but can also be others. The flash memory cell and user identification will be more fully described below in reference to the FIGS. A host interface controller 507 communicates to the north bridge via bus 535 and host PCI bus. The host interface controller also has a data control 511. Host interface controller 507 communicates to the console using bus 513, which couples to connection 515.

Peripheral console 503 includes a variety of elements to interface to the module 501, display 551, and network 553. The console forms around south bridge 571, which couples to



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bus **563**, which couples to bus **561**. Bus **561** is in communication with network card **555**, which is a local area network for Ethernet, for example. South bridge also couples through control **569** to peripheral interface controller **567**, which also communicates to bus **561**. Peripheral interface controller also couples to host interface controller through connection **515** and bus **513**. The peripheral console has a primary removable drive **559** connected to south bridge through bus **575**. South bridge also couples to secondary hard disk through bus **577**.

In a specific embodiment, the peripheral console also has a serial EEPROM memory device **575**, which is coupled to the peripheral interface controller. The memory device can store a security identification number or the like. The memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The memory generally has at least 16 kilobits of storage cells or more. Preferably, the memory device is a 16 kilobit device or 64 megabit device or greater, depending upon the application. The memory can be any product such as a X24320 product made by a company called Xicor, but can also be others. The memory cell and user identification will be more fully described below in reference to the FIGS.

FIG. **6** is a simplified diagram of a security method **600** for a module according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method shows an example of how the present security method can be implemented. The present method uses a combination of software **601** and hardware **603**, which is in the computer module. A plurality of external devices can be accessed depending upon the embodiment. These external devices include a secondary hard drive **618**, a removable drive **619**, a network (e.g., LAN, modem) device **621**, and others. A keyboard **623** is also shown, which can act locally.

The software **601** includes an operating system **609**, application programs **607**, and a data security and initialization program **605**. Other programs can also exist. Additionally, some of these programs may not exist. Preferably, the data security and initialization program exists. This data security and initialization program is initiated once the attached computer module is inserted into the console. The program interface and oversees a variety of hardware features, which will be used to control access to the external devices, for example. Of course, the particular configuration of the software will depend upon the application.

Hardware features can be implemented using a primary hard disk **611** coupled to a CPU/cache combination, which includes a main memory. The main memory is often a volatile memory such as dynamic random access memory. Data from any one of the external devices can enter the CPU/cache combination. For example, the secondary hard disk memory and I/O address range data is transferred **624** to the CPU/cache combination. The removable drive memory and I/O address range data can also transfer **625** to the CPU/cache combination. The LAN memory and I/O address range data can also transfer **626** to the CPU/cache combination. Keyboard data can also transfer **627** to the CPU/cache combination. To write data from the module into any one of these external elements, the data security program interfaces with the data detection and control circuit to determine if such data should be transferred to any one of the external elements. As noted, the external elements include, among others, secondary hard disk, and removable drive. Here, the data security program checks the security identification number with other numbers to determine the security access level. There are

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many other ways that the present invention can be implemented. These methods are described more fully below.

FIG. **7** is a simplified diagram **700** of a method according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method begins at power up, which is step **701**. The present method reads a security code, which has been entered by a user, for example, in step **703**. The security code can be a string of characters, including numbers and letters. The security code is preferably a mixture of numbers and letters, which are at least about 6 characters in length, but is not limited.

The present method reads (step **703**) the security code, which has been entered. Next, the security code is compared with a stored code, which is in flash memory or the like (step **705**). If the compared code matches with the stored code, the method resumes to step **708**. Alternatively, the method goes to step **707** via branch **706** where no access is granted. When no access is granted, all data are blocked out from the user that attempts to log onto the system. Alternatively, the method determines if a certain level of access is granted, step **708**. Depending upon the embodiment, the present method can grant full access, step **710**, via branch **716**. The present method allows full access based upon information stored in the flash memory device. Alternatively, the method can allow the user to access a limited amount of information.

Here, the present method allows for at least one or more than two levels of access. In a specific embodiment, the present method allows for the user of the module to access peripheral storage (step **711**). The access privilege is read-only. The user can read information on the peripheral storage including hard disks and the like. Once the user accesses the storage, the method data control, step **719**, takes over, where the hardware prevents the user from accessing other information, step **721**. In a specific embodiment, the method can allow information to be removed from the peripheral storage. If the method allows for data to be removed, step **723**, the method goes through branch **731** to let data out, which can occur through the module. Alternatively, the method goes to block data (step **725**) via branch **733**. Depending upon the embodiment, the method returns to the decision block, step **723**. Alternatively, the method traverses branch **714** to a peripheral read-only process, step **712**. The read-only process programs data control, step **713**. Next, the hardware takes over (step **715**). The method blocks all data from being accessed by the user, step **717**.

FIG. **8** is a simplified diagram of a system **800** according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The system **800** includes an attached computer module **801**, which can be inserted into one of a plurality of console devices to create a "plug and play" operation. For example, the console device can be peripheral console **801** or peripheral console **805**. Each peripheral console can have similar or different connection characteristics. Peripheral console **803** couples to a local area network using Ethernet **817**. Peripheral console **805** couples to a DSL line **827** through a DSL modem **825**. Other consoles can also be included to use other types of networks such as ADSL, Cable Modem, wireless, Token Ring, and the like.

As shown, the attached computer module has elements such as a memory region **807**, which stores BIOS information, a security code, and a security identification number on a flash memory device or the like. The memory region

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couples to a central processing region 809, which can include CPU, chipset, cache memory, graphics, and a hard disk drive, as well as other features. The central processing region couples to a host interface controller, which interfaces the attached computer module to one of the peripheral consoles. Any of the above information can also be included in the attached computer module.

Each peripheral console also has a variety of elements. These elements include a region 813, 821, which has a flash memory device with a security identification number, a password, access information, access privileges, internet service provider access information, as well as other features, which were previously noted. The peripheral console also has an interface controller 815, 823, which couples region 813, 821, respectively to a networking device 817, 825. The networking device can be an Ethernet card 817, which allows communication to the local area network 819. Alternatively, the networking device can be a DSL modem 825, which allows communication to a DSL (or ADSL) phone line. Other types of networking device can also be used, depending upon the application.

Each console provides a selected connection based upon set of predefined factors. These factors include communication hardware information so that software in attached computer module can read and allow a connection to a network. Here, access information can be provided to the user. Information about connection information will also be included. This connection information includes telephone numbers, account numbers, passwords (local), or a company password. The console and module combination will take care of charges, etc. based upon time bases. Module will have credit card information, but will have security. In a specific embodiment, the module inserts into the console. The module then asks the console which hardware will be used. If the hardware is an Ethernet connect, the module configures connection information to access the Ethernet connection. Alternatively, if the hardware requires a DSL connection, the module configures connection information to access the DSL connection. Other configuration information such as company server information, password, can also be provided.

*Embodiments in accordance with the present invention may interface two PCI or PCI-like buses using a non-PCI or non-PCI-like channel. In accordance with embodiments of the present invention, PCI control signals are encoded into control bits and the control bits, rather than the control signals that they represent, are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.*

*The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using low voltage differential signal (LVDS) channels for the interface. An LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel, which is used in the prior art to interface two PCI buses. Therefore, the present invention advantageously uses an LVDS channel for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. An interface having a smaller number of signal channels and, therefore, a*

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*smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.*

*In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operate. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the host interface controller (HIC) to the peripheral interface controller (PIC) while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.*

*FIG. 9 is a block diagram of one embodiment of a computer system 900 using the interface of the present invention. Computer system 900 includes an ACM 905 and a peripheral console 910, which are described in greater detail in the application of William W. Y. Chu for "Personal Computer Peripheral Console With Attached Computer Module" filed concurrently with the present application on Sep. 8, 1998, now U.S. Pat. No. 6,216,185, and incorporated herein by reference. The ACM 905 and the peripheral console 910 are interfaced through an exchange interface system (XIS) bus 915. The XIS bus 915 includes power bus 916, video bus 917 and peripheral bus (XPBus) 918, which is also herein referred to as an interface channel. The power bus 916 transmits power between ACM 905 and peripheral console 910. In a preferred embodiment power bus 916 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 917 transmits video signals between the ACM 905 and the peripheral console 910. In a preferred embodiment, the video bus 917 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-Video) signals. The XPBus 918 is coupled to host interface controller (HIC) 919 and to peripheral interface controller (PIC) 920, which is also sometimes referred to as a bay interface controller. In the embodiment shown in FIG. 9, HIC 919 is coupled to an integrated unit 921 that includes a CPU, a cache and a north bridge.*

*FIG. 10 is a detailed block diagram of one embodiment of the host interface controller (HIC) of the present invention. As shown in FIG. 10, HIC 1000 comprises bus controller 1010, translator 1020, transmitter 1030, receiver 1040, a PLL 1050, an address/data multiplexer (A/D MUX) 1060, a read/write controller (RD/WR Cntl) 1070, a video serial to parallel converter 1080 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1090.*

*HIC 1000 is coupled to an optional flash memory BIOS configuration unit 1001. Flash memory unit 1001 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1060 and RD/WR Control 1070, which control the programming, read, and write of flash memory unit 1001.*

*Bus controller 1010 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1010 includes a slave (target) unit 1011 and a master unit 1016. Both slave unit 1011 and master unit 1016 each include two first in first out (FIFO) buffers, which are preferably*

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asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1016 as well as the two FIFOs in the slave unit 1011 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1011 includes encoder 1022 and decoder 1023, while master unit 1016 includes encoder 1027 and decoder 1028. The FIFOs 1012, 1013, 1017 and 1018 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 10 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1023 and 1028 to a form more suitable for transmission on the host PCI bus. Thereafter the decoded data and address information is passed through FIFOs 1013 and 1018 prior to being transferred to the host PCI bus. FIFOs 1012, 1013, 1017 and 1018, allow bus controller 1010 to handle posted and delayed PCI transactions and to provide deep buffering to store PCI transactions.

Bus controller 1010 also comprises slave read/write control (RD/WR Cntl) 1014 and master read/write control (RD/WR Cntl) 1015. RD/WR controls 1014 and 1015 are involved in the transfer of PCI control signals between bus controller 1010 and the host PCI bus.

Bus controller 1010 is coupled to translator 1020. Translator 1020 comprises encoders 1022 and 1027, decoders 1023 and 1028, control decoder & separate data path unit 1024 and control encoder & merge data path unit 1025. As discussed above encoders 1022 and 1027 are part of slave data unit 1011 and master data unit 1016, respectively, receive PCI address and data information from FIFOs 1012 and 1017, respectively, and encode the PCI address and data information into a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, decoders 1023 and 1028 are part of slave data unit 1011 and master data unit 1016, respectively, and format address and data information from receiver 1040 into a form more suitable for transmission on the host PCI bus. Control encoder & merge data path unit 1025 receives PCI control signals from the slave RD/WR control 1014 and master RD/WR control 1015. Additionally, control encoder & merge data path unit 1025 receives control signals from CPU CNTL & GPIO latch/driver 1090, which is coupled to the CPU and north bridge (not shown in FIG. 10). Control encoder & merge data path unit 1025 encodes PCI control signals as well as CPU control signals and north bridge signals into control bits, merges these encoded control bits and transmits the merged control bits to transmitter 1030, which then transmits the control bits on the data lines PD0 to PD3 and control line PCN of the XPBus. Examples of control signals include PCI control signals and CPU control signals. A specific example of a control signal is FRAME# used in PCI buses. A control bit, on the other hand is a data bit that represents a control signal. Control decoder & separate data path unit 1024 receives control bits from receiver 1040 which receives control bits on data lines PDR0 to PDR3 and control line PCNR of the XPBus. Control decoder & separate data path unit 1024 separates the control bits it receives from receiver 1040 into PCI control signals, CPU control signals and north bridge signals, and decodes the control bits into PCI control signals, CPU control signals, and north bridge signals all of which meet the relevant timing constraints.

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Transmitter 1030 receives multiplexed parallel address/data (A/D) bits and control bits from translator 1020 on the AD[31::0] out and the CNTL out lines, respectively. Transmitter 1030 also receives a clock signal from PLL 1050. PLL 1050 takes a reference input clock and generates PCK that drives the XPBus. PCK is asynchronous with the PCI clock signal and operates at 66 MHz, twice the speed of the PCI clock of 33 MHz. The higher speed is intended to accommodate at least some possible increases in the operating speed of future PCI buses. As a result of the higher speed, the XPBus may be used to interface two PCI or PCI-like buses operating at 66 MHz rather than 33 MHz or having 64 rather than 32 multiplexed address/data lines.

The multiplexed parallel A/D bits and some control bits input to transmitter 1030 are serialized by parallel to serial converters 1032 of transmitter 1030 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1033 into 10 bit packets and send out on control line PCN of the XPBus.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 11, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel which may consist of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a bit line or bit channel in an LVDS or IEEE 1394 interface consists of a pair of physical lines which together transmit a signal.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIG. 12 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 1200 is nearly identical to HIC 600 in its function, except that HIC 600 interfaces the host PCI bus to the XPBus while PIC 1200 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 1200 serve the same function as their corresponding components in HIC 600. Reference numbers for components in PIC 1200 have been selected such that a component in PIC 1200 and its corresponding component in HIC 600 have reference numbers that differ by 500 and have the same two least significant digits. Thus for example, the bus controller in PIC 1200 is referenced as bus controller 1210 while the bus controller in HIC 600 is referenced as bus controller 610. As many of the elements in PIC 1200 serve the same functions as those served by their corresponding elements in HIC 600 and as the functions of the corresponding elements in HIC 600 have been described in detail above, the function of elements of PIC 1200 having corresponding elements in HIC 600 will not be further described herein. Reference may be made to the



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above description of FIG. 6 for an understanding of the functions of the elements of PIC 1200 having corresponding elements in HIC 600.

As suggested above, there are also differences between HIC 600 and PIC 1200. Some of the differences between HIC 600 and PIC 1100 include the following. First, receiver 1240 in PIC 1200, unlike receiver 640 in HIC 600, does not contain a synchronization unit. As mentioned above, the synchronization unit in HIC 600 synchronizes the PCKR clock to the PCK clock locally generated by PLL 650. PIC 1100 does not locally generate a PCK clock and therefore, it does not have a locally generated PCK clock with which to synchronize the PCK clock signal that it receives from HIC 600. Another difference between PIC 1200 and HIC 600 is the fact that PIC 1200 contains a video parallel to serial converter 1289 whereas HIC 600 contains a video serial to parallel converter 680. Video parallel to serial converter 1289 receives 16 bit parallel video capture data and video control signals on the Video Port Data [0::15] and Video Port Control lines, respectively, from the video capture circuit (not shown in FIG. 12) and converts them to a serial video data stream that is transmitted on the VPD line to the HIC. The video capture circuit may be any type of video capture circuit that outputs a 16 bit parallel video capture data and video control signals. Another difference lies in the fact that PIC 1200, unlike HIC 600, contains a clock doubler 1282 to double the video clock rate of the video clock signal that it receives. The doubled video clock rate is fed into video parallel to serial converter 1282 through buffer 1283 and is sent to serial to parallel converter 680 through buffer 1284. Additionally, reset control unit 1235 in PIC 1200 receives a reset signal from the CPU CNTL & GPIO latch/driver unit 1190 and transmits the reset signal on the RESET# line to the HIC 600 whereas reset control unit 645 of HIC 600 receives the reset signal and forwards it to its CPU CNTL & GPIO latch/driver unit 690 because, in the above embodiment, the reset signal RESET# is unidirectionally sent from the PIC 1200 to the HIC 600.

The XPBUS which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBUS, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

In the embodiment shown in FIG. 9, HIC 919 is coupled to an integrated unit 921 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 13, the CPU 1305 and north bridge 1310 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 14, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated HIC and north bridge unit 1405 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1410 includes a PIC and a south bridge.

Although the functionality above has been generally described in terms of a specific sequence of steps, other steps can also be used. Here, the steps can be implemented in a combination of hardware, firmware, and software. Either of these can be further combined or even separated. Depending

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upon the embodiment, the functionality can be implemented in a number of different ways without departing from the spirit and scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

[1. A security protection method for a computer module, said method comprising:

inserting the computer module into a console;  
initiating a security program in said module to read a security identification of said console and to read a security identification of said computer module;  
determining of a predetermined security status based upon a relationship of said console identification and said computer module identification;  
selecting said predetermined security status; and  
operating said computer module based upon said security status.]

[2. The method of claim 1 wherein said predetermined security status disables a network access to the computer module.]

[3. The method of claim 1 wherein said predetermined security status disables a secondary storage of information from said computer module to substantially prevent information to be transferred from a memory of the computer module to said secondary storage.]

[4. The method of claim 1 wherein said security program is provided in a system BIOS.]

[5. The method of claim 1 wherein said step of initiating reads said security identification of said computer module from a flash memory device.]

[6. The method of claim 1 wherein said step of initiating reads said security identification of said console from a flash memory device.]

[7. The method of claim 1 wherein said console is selected from a desktop home computing device, an office desktop computing device, a mobile computing device, a television set-top computing device, and a co-worker's computing device.]

[8. A system for secured information transactions, the system comprising:

a console comprising a peripheral controller housed in the console;  
a user identification input device coupled to the peripheral controller, the user identification input device being provided for user identification data; and  
an attached computer module coupled to the console, the attached computer module comprising a security memory device stored with the user identification data.]

[9. The system of claim 8 wherein the user identification input device is a finger print reader.]

[10. The system of claim 8 wherein the user identification input device is a voice processing device.]

[11. A method for operating a module computer into one of a plurality of network systems, the method comprising:

providing a computer module, the module comprising a connection program;  
inserting the computer module into a computer console, the computer console having access to a network;  
receiving connection information from the computer console;

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configuring the connection program to adapt to the connection information; and  
establish a connection between the computer module and a server coupled to the network.】

【12. The method of claim 11 wherein the connection information comprises a connection protocol for providing the connection.】

【13. The method of claim 12 wherein the connection protocol is selected from TCP/IP, or mobile IP.】

14. A system for secured information transactions, the system comprising:

a console comprising a network controller housed in the console;

a user identification input device coupled to the network controller; and

an attached computer module coupled to the console, the attached computer module comprising

a central processing unit,

a device stored with a user identification data,

a security program providing password protection for access to the computer module based on the user identification data,

an integrated interface controller and bridge unit to communicate an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit directly coupled to the central processing unit, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction,

wherein the low voltage differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

15. The system of claim 14 wherein the encoded serial bit stream comprises 10 bit packets.

16. The system of claim 14 wherein the integrated interface controller and bridge unit is coupled to the central processing unit without any intervening PCI bus.

17. The system of claim 16 wherein the integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with the north bridge, and the low voltage differential signal channel extends from the interface controller to convey the encoded serial bit stream of PCI bus transaction.

18. The system of claim 16 further comprising a peripheral component coupled to the central processing unit through the low voltage differential signal channel.

19. The system of claim 16 wherein the attached computer module further comprises a main memory coupled to the central processing unit through the integrated interface controller and bridge unit.

20. The system of claim 16 wherein the integrated interface controller and bridge unit is configured to output encoded PCI address and data bits in serial form that are conveyed over the low voltage differential signal channel.

21. The system of claim 16 wherein the encoded serial bit stream of PCI bus transaction comprises information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

22. The system of claim 16 wherein the low voltage differential signal channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

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23. The system of claim 16 wherein the network controller comprises an Ethernet controller.

24. A method comprising:

providing a computer module, the module comprising

a central processing unit,

a connection program,

an integrated interface controller and bridge unit to output an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction, the integrated interface controller and bridge unit coupled to the central processing unit without any intervening PCI bus, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial bit stream of PCI bus transaction;

inserting the computer module into a computer console, the computer console having access to a network;

receiving connection information from the computer console;

configuring the connection program to adapt to the connection information; and

establishing a connection between the computer module and a server coupled to the network,

wherein the low voltage differential signal channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

25. The method of claim 24 wherein the connection between the computer module and the server comprises an Ethernet connection.

26. The method of claim 24 wherein the connection protocol is TCP/IP.

27. The method of claim 24 further comprising conveying, over the low voltage differential signal channel, the encoded serial bit stream of PCI bus transaction as 10 bit packets.

28. The method of claim 27 wherein conveying the encoded serial bit stream of PCI bus transaction comprises conveying information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

29. A system of connecting a computer module to a network, the system comprising:

a console having access to a network;

a computer module inserted into the console and powered by the console, the computer module comprising

a central processing unit,

a peripheral bridge coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, the peripheral bridge comprising an interface controller to communicate an encoded serial bit stream of address and data bits of PCI bus transaction,

a low voltage differential signal channel extending from the interface controller to convey the encoded serial bit stream of PCI bus transaction, and

a connection program receiving connection information from the console, configuring the connection program to adapt to the connection information, and establishing a connection between the computer module and a server coupled to the network,

wherein the low voltage differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

30. The system of claim 29 wherein the encoded serial bit stream comprises 10 bit packets.

31. The system of claim 29 wherein the interface controller is integrated with the peripheral bridge as a single integrated unit.

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32. The system of claim 31 wherein the peripheral bridge comprises a north bridge.

33. The system of claim 32 further comprising a south bridge coupled to the north bridge through the low voltage differential signal channel.

34. The system of claim 31 wherein the interface controller is coupled to the central processing unit without any intervening PCI bus.

35. The system of claim 31 wherein each of the unidirectional serial bit channels corresponds to a point-to-point link.

36. A system for secured information transactions, the system comprising:

a console comprising a network communication controller housed in the console;

a user identification input device coupled to the console, the user identification input device being provided for user identification data; and

an attached computer module coupled to the console, the attached computer module comprising

a central processing unit,

a security program,

a peripheral bridge directly coupled to the central processing unit, the peripheral bridge comprising an interface controller, the peripheral bridge and the interface controller configured as a single integrated unit, and

a low voltage differential signal channel that comprises two sets of unidirectional serial bit channels in opposite directions which transmit data in 10 bit packets, the low voltage differential signal channel coupled to the interface controller;

wherein said security program receives the user identification data from the console, determines a predetermined security status, and operating said computer module based upon said security status.

37. The system of claim 36 wherein the data packets comprise an encoded bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction.

38. The system of claim 37 wherein the interface controller is configured to transmit and receive encoded PCI address and data bits over the low voltage differential signal channel.

39. The system of claim 38 wherein the interface controller is coupled to the central processing unit without any intervening PCI bus.

40. The system of claim 38 wherein the peripheral bridge comprises a north bridge.

41. The system of claim 40 further comprising a south bridge coupled to the north bridge.

42. The system of claim 41 wherein the south bridge is coupled to the north bridge through the low voltage differential signal channel.

43. The system of claim 38 wherein the low voltage differential signal channel comprises two sets of unidirectional, multiple serial bit channels to convey data in opposite directions, and each of the unidirectional, multiple serial bit channels corresponds to a point-to-point link.

44. A system for secured information transactions, the system comprising:

a computer console comprising

a network communication controller housed in the console,

a low voltage differential signal (LVDS) channel comprising two sets of multiple unidirectional serial channels that transmit encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction in opposite directions, and

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a user identification input device coupled to the console, the user identification input device being provided for user identification data; and

an attached computer module that inserts into the console in a "plug and play" operation, the attached computer module comprising

a security program providing password protection for data content within said attached computer module,

a security memory device stored with the user identification data, and

an interface controller coupled to the console through serial bit based lines;

wherein the interface controller transfers data between the computer module and the console in Universal Serial Bus (USB) protocol.

45. The system of claim 44 wherein said attached computer module inserts into the console and is powered by the console to form a functional computer.

46. The system of claim 44 wherein the attached computer module has a tamper resistant enclosure.

47. The system of claim 44 wherein the security memory device comprises of flash memory.

48. The system of claim 44 wherein the console further comprises an integrated interface controller and bridge unit to transmit and receive encoded serial bits of PCI bus transaction over the LVDS channel.

49. The system of claim 48 wherein the encoded serial bits of PCI bus transaction comprise information to permit decoding to create a PCI bus transaction.

50. A system for secured information transactions, the system comprising:

a console comprising a network communication controller housed in the console;

a user input device coupled to the console, the user input device being provided for user identification data; and

an attached computer module inserted into the console, the attached computer module comprising

a central processing unit,

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, the peripheral bridge comprising an integrated interface controller to communicate an encoded serial bit stream of address and data bits of PCI bus transaction,

a low voltage differential signal channel extending from the integrated interface controller to convey the encoded serial bit stream of PCI bus transaction, and a mass storage unit storing a security program and user identification data;

wherein the security program receives the user identification data from the input device, matches the stored user identification data and permits external access to the computer module,

wherein the low voltage differential signal channel comprises two sets of unidirectional serial bit channels which transmit data in opposite directions, and each of the unidirectional serial bit channels corresponds to a point-to-point link.

51. The system of claim 50 wherein the security program further determines a predetermined security status, and controls different levels of access privilege to said attached computer module.

52. The system of claim 50 wherein the encoded serial bit stream comprises 10 bit packets.

53. The system of claim 50 wherein the peripheral bridge comprises a north bridge.

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54. The system of claim 50 wherein the integrated interface controller is coupled to the central processing unit without any intervening PCI bus, and the integrated interface controller is configured to output encoded address and data bits of PCI bus transaction in serial form that are conveyed over the low voltage differential signal channel.

55. The system of claim 50 wherein the low voltage differential signal channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

56. A system comprising:

a console housing a network controller and a low voltage differential signal serial channel for communicating encoded address and data bits of Peripheral Component Interconnect (PCI) bus transaction;

a user identification input device coupled to the console; and

an attached computer module coupled to the console, the attached computer module comprising

a device stored with a user identification data,

a security program providing protection for access to the computer module based on the user identification data, and

an interface controller coupled to the console for communicating data in a serial bit stream,

wherein the low voltage differential signal serial channel further comprises two sets of unidirectional serial bit channels which transmit data in opposite directions.

57. The system of claim 56 wherein the encoded address and data bits of PCI bus transaction comprise 10 bit data packets.

58. The system of claim 56 wherein the computer module further comprises a flash memory mass storage device.

59. The system of claim 56 wherein the serial bit stream transmits data packets in Universal Serial Bus (USB) protocol.

60. A system for secured information transactions, the system comprising:

a console comprising a peripheral controller housed in the console;

a user identification input device coupled to the peripheral controller, the user identification input device being provided for user identification data; and

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an attached computer module coupled to the console, the attached computer module comprising

a security memory device stored with the user identification data,

a central processing unit,

an integrated interface controller and bridge unit to communicate an encoded serial stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction as 10 bit packets, the integrated interface controller and bridge unit directly coupled to the central processing unit, and

a low voltage differential signal channel coupled to the integrated interface controller and bridge unit to convey the encoded serial stream of PCI bus transaction, the low voltage differential signal channel comprising two sets of unidirectional serial bit channels which transmit data in opposite directions.

61. The system of claim 60 wherein the integrated interface controller and bridge unit is coupled to the central processing unit without any intervening PCI bus.

62. The system of claim 61 wherein the integrated interface controller and bridge unit comprises a north bridge and an interface controller integrated with the north bridge, and the low voltage differential signal channel extends from the interface controller to convey the encoded serial stream of PCI bus transaction.

63. The system of claim 61 wherein the attached computer module further comprises a main memory coupled to the central processing unit through the integrated interface controller and bridge unit.

64. The system of claim 61 wherein the integrated interface controller and bridge unit is configured to output encoded PCI address and data bits in serial form that are conveyed over the low voltage differential signal channel.

65. The system of claim 61 wherein the encoded serial stream of PCI bus transaction comprises information to permit decoding to create a PCI bus transaction across the low voltage differential signal channel.

66. The system of claim 61 wherein the low voltage differential signal channel comprises a first plurality of unidirectional, differential signal pairs to convey data in a first direction and a second plurality of unidirectional, differential signal pairs to convey data in a second, opposite direction.

\* \* \* \* \*





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 (12) **Reissued Patent**  
**Chu**

(10) **Patent Number:** **US RE44,468 E**  
 (45) **Date of Reissued Patent:** **\*Aug. 27, 2013**

(54) **DATA SECURITY METHOD AND DEVICE  
FOR COMPUTER MODULES**

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(73) Assignee: **Acqis LLC**, McKinney, TX (US)

(\*) Notice: This patent is subject to a terminal disclaimer.

(21) Appl. No.: **13/562,210**

(22) Filed: **Jul. 30, 2012**

**Related U.S. Patent Documents**

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(64) Patent No.: **6,643,777**  
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U.S. Applications:

(63) Continuation of application No. 13/294,108, filed on Nov. 10, 2011, now Pat. No. Re. 43,602, which is a continuation of application No. 12/561,138, filed on Sep. 16, 2009, now Pat. No. Re. 42,984, which is a continuation of application No. 11/056,604, filed on Feb. 10, 2005, now Pat. No. Re. 41,092.

(51) **Int. Cl.**  
**G06F 12/00** (2006.01)

(52) **U.S. Cl.**  
 USPC ..... **726/16; 726/20**

(58) **Field of Classification Search**  
 USPC ..... 726/2-9, 16-21, 34, 36; 713/182-183,  
 713/192-194; 710/1, 7, 8, 15, 20, 22, 100  
 See application file for complete search history.

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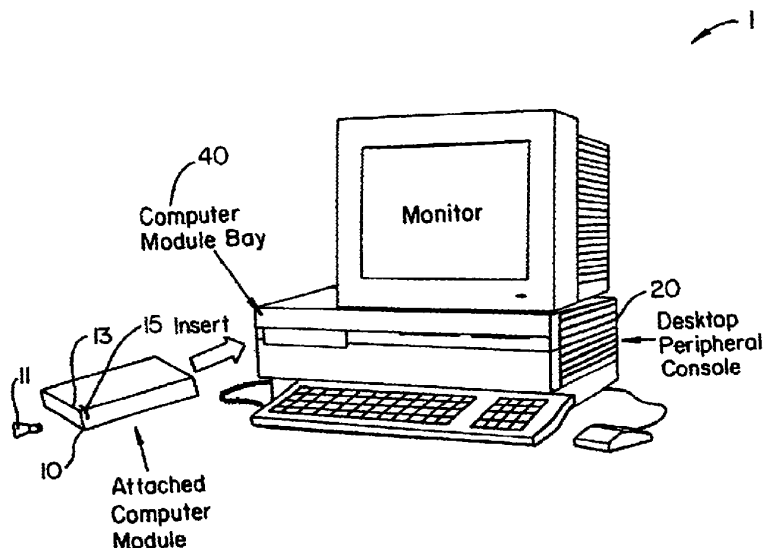
*Primary Examiner* — Hosuk Song

(74) *Attorney, Agent, or Firm* — Cooley LLP

(57) **ABSTRACT**

A security method for an attached computer module in a computer system. The security method reads a security identification number in an attached computer module and compares it to a security identification number in a console, which houses the attached computer module. Based upon a relationship between these numbers, a security status is selected. The security status determines the security level of operating the computer system.

**36 Claims, 24 Drawing Sheets**



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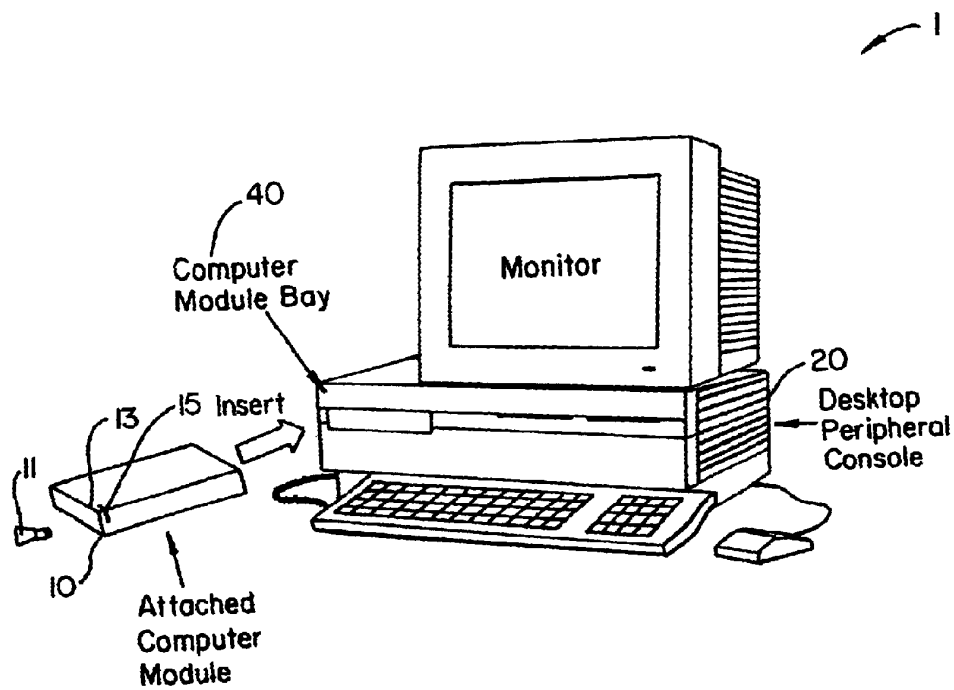


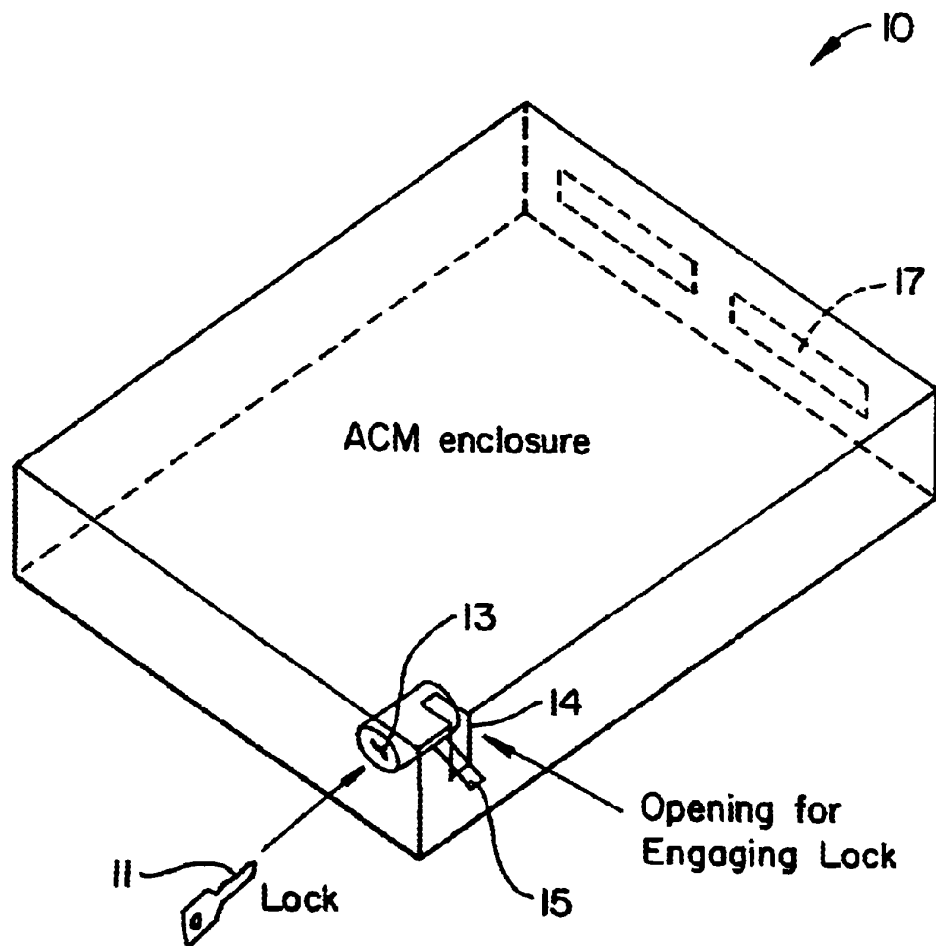
FIG. 1

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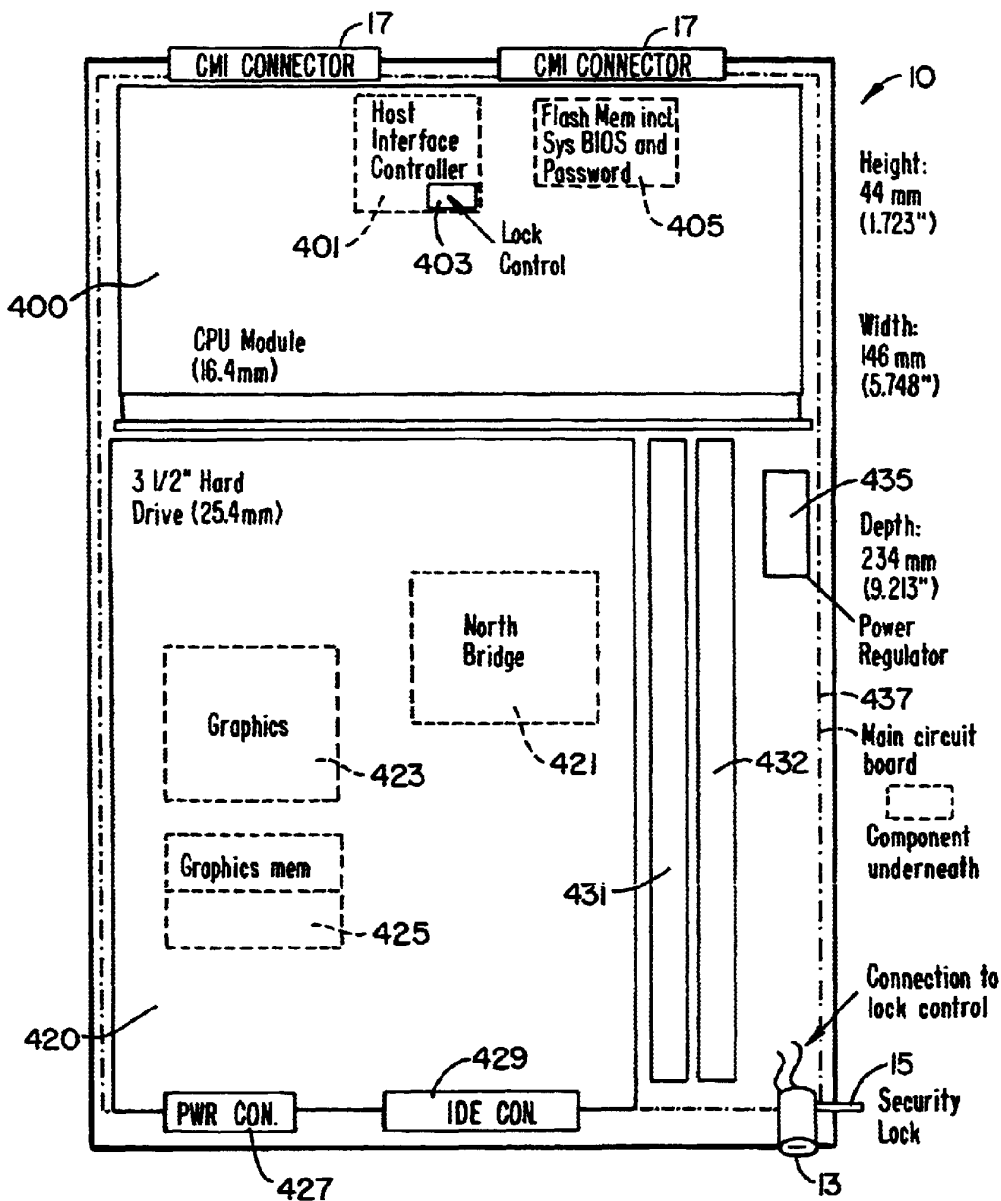
**FIG 2**

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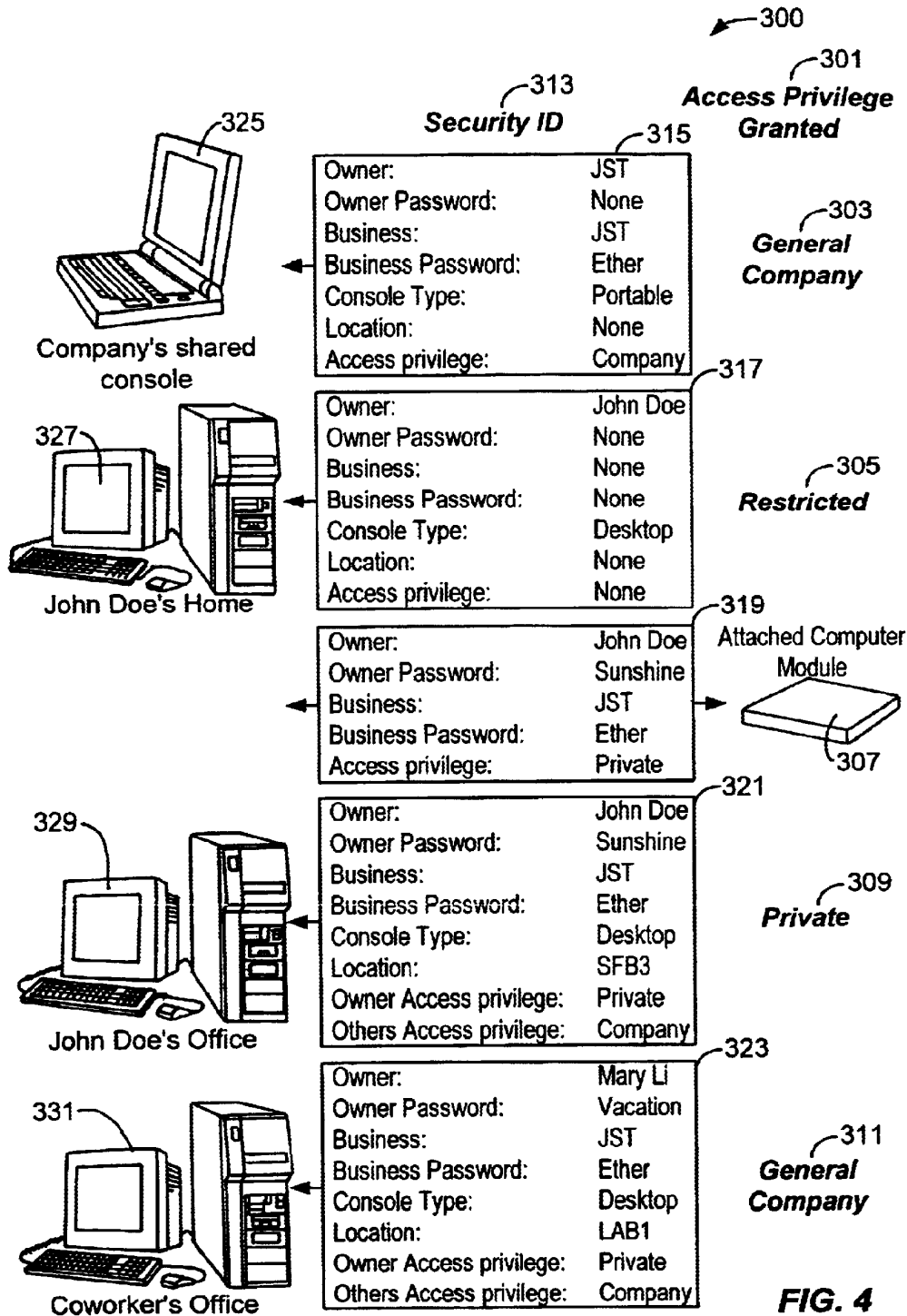


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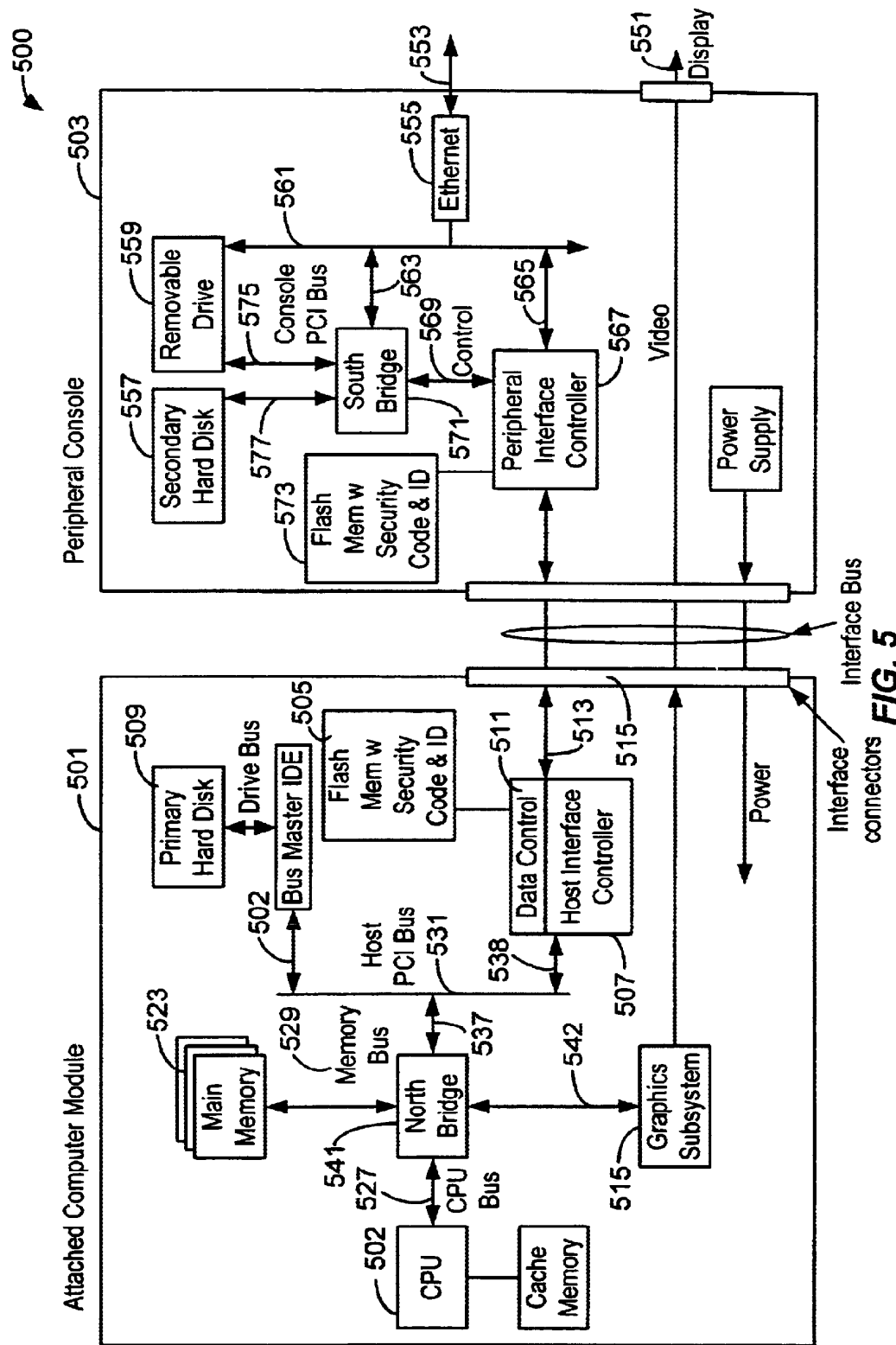


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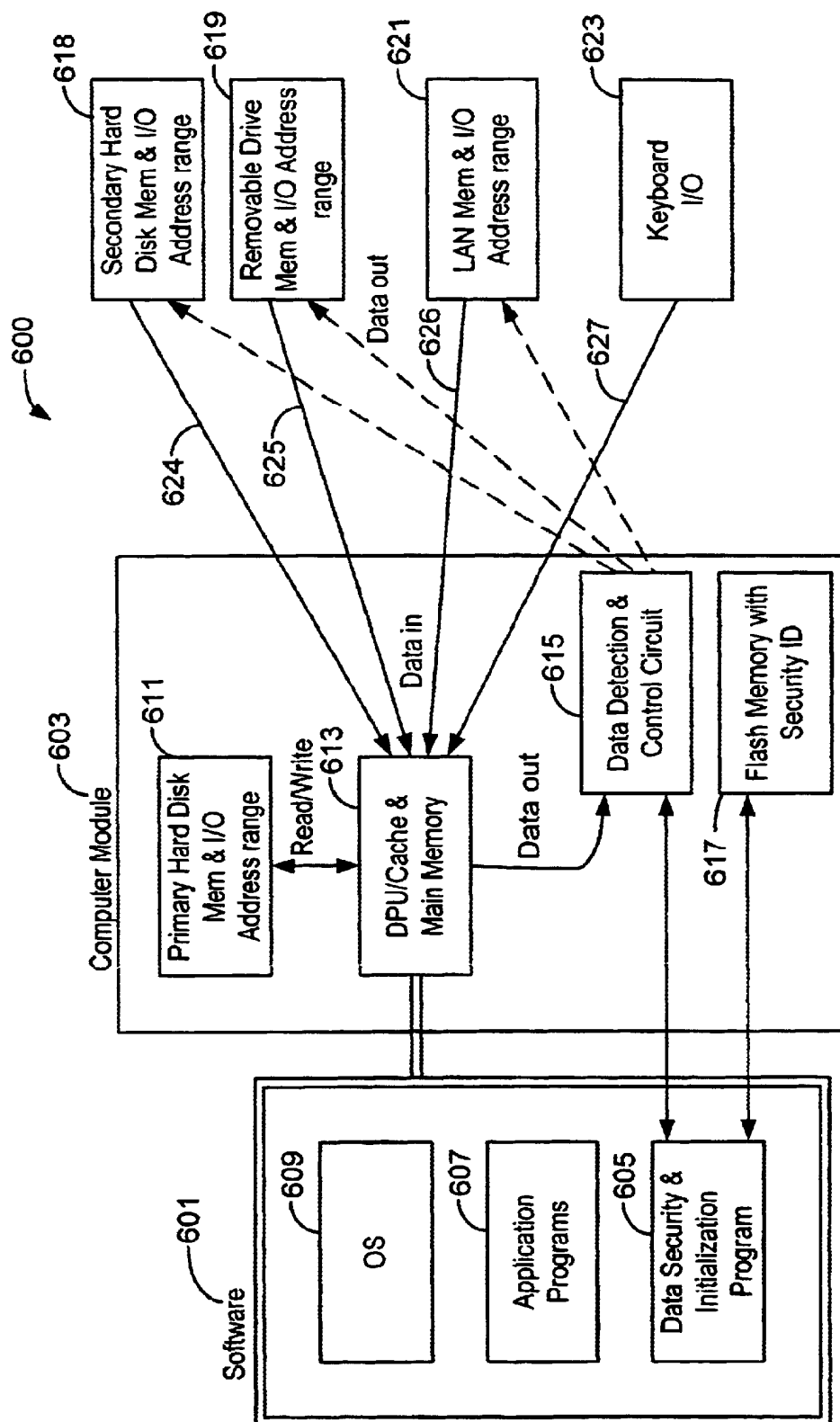


FIG. 6



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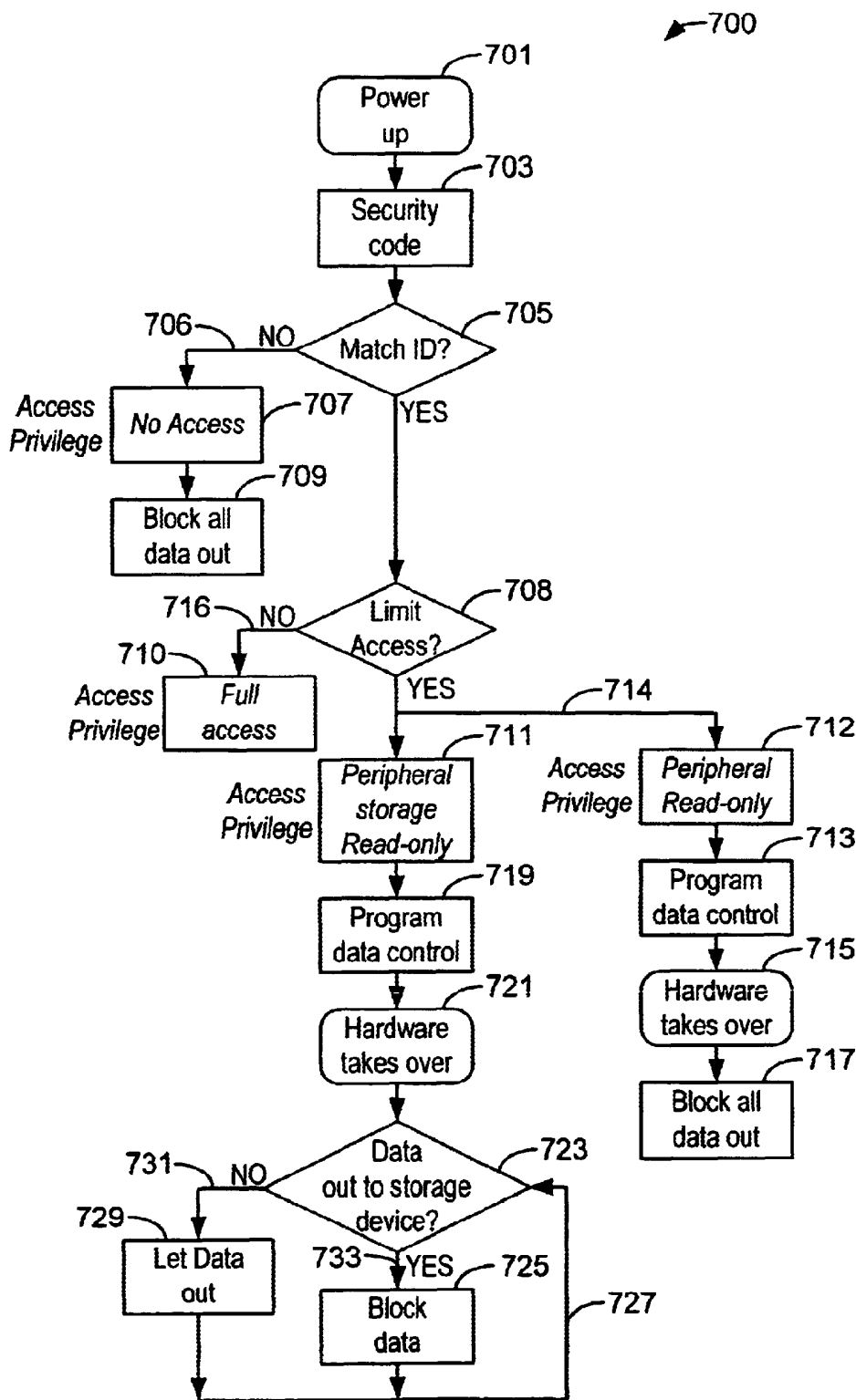


FIG. 7

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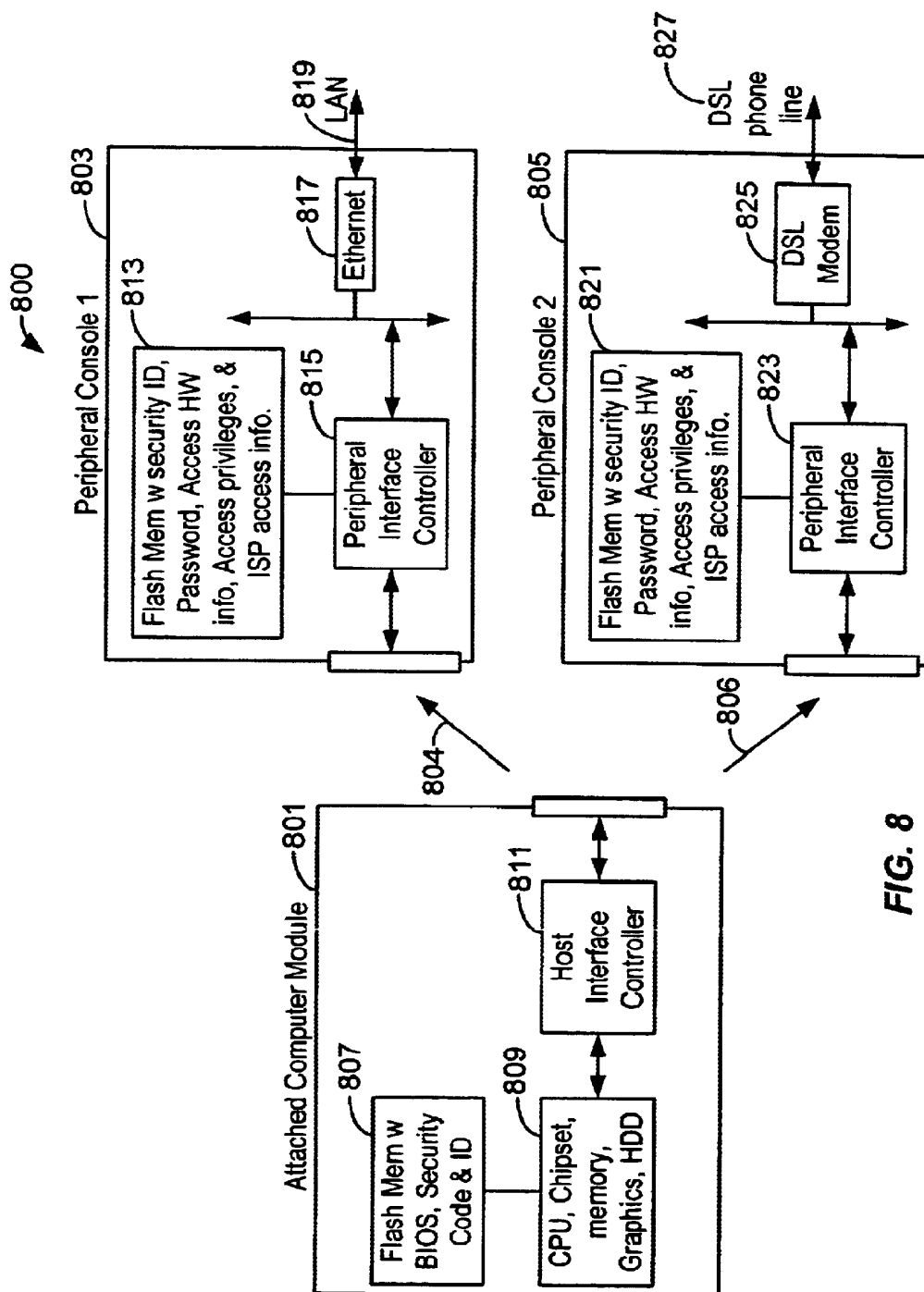


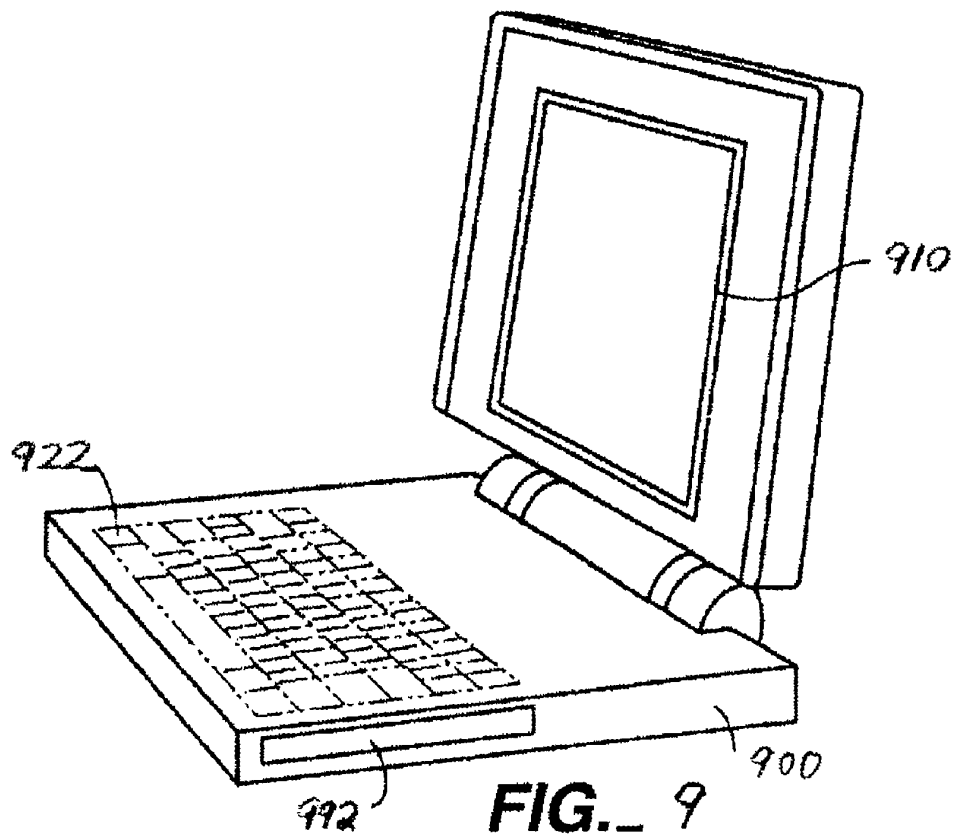
FIG. 8

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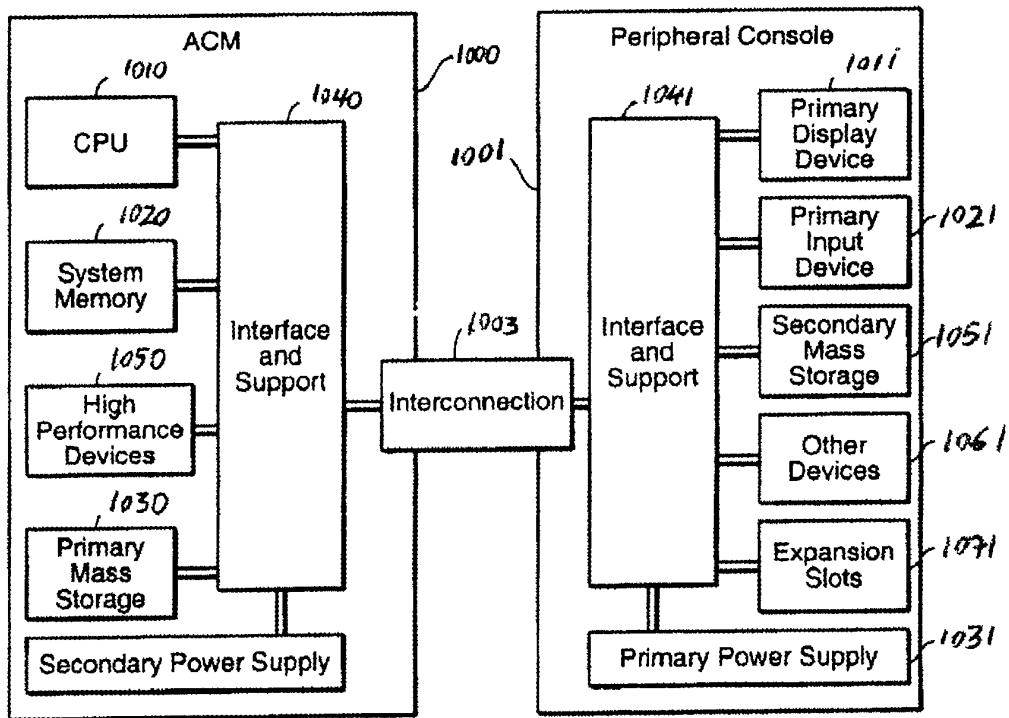


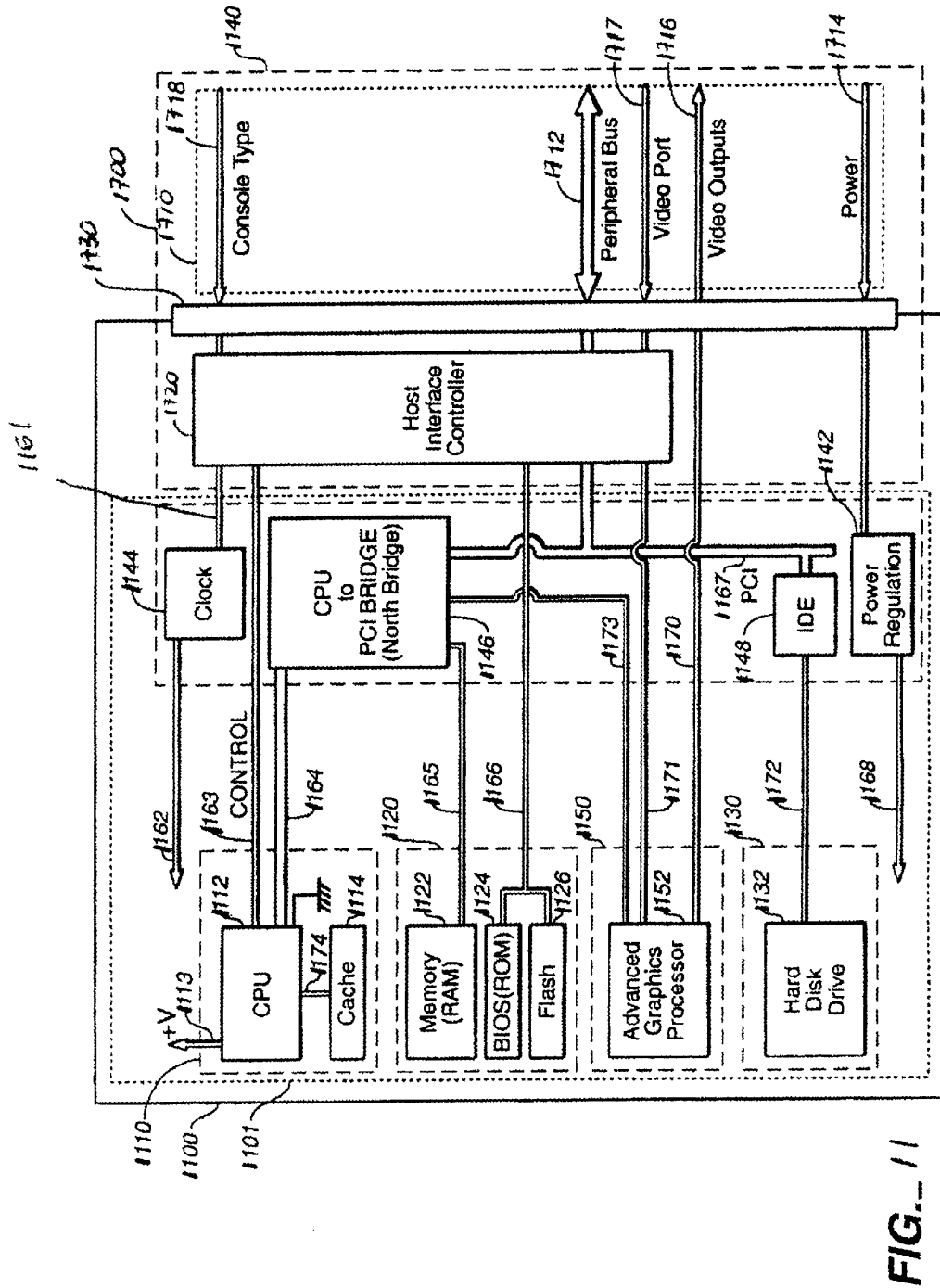
FIG. 10

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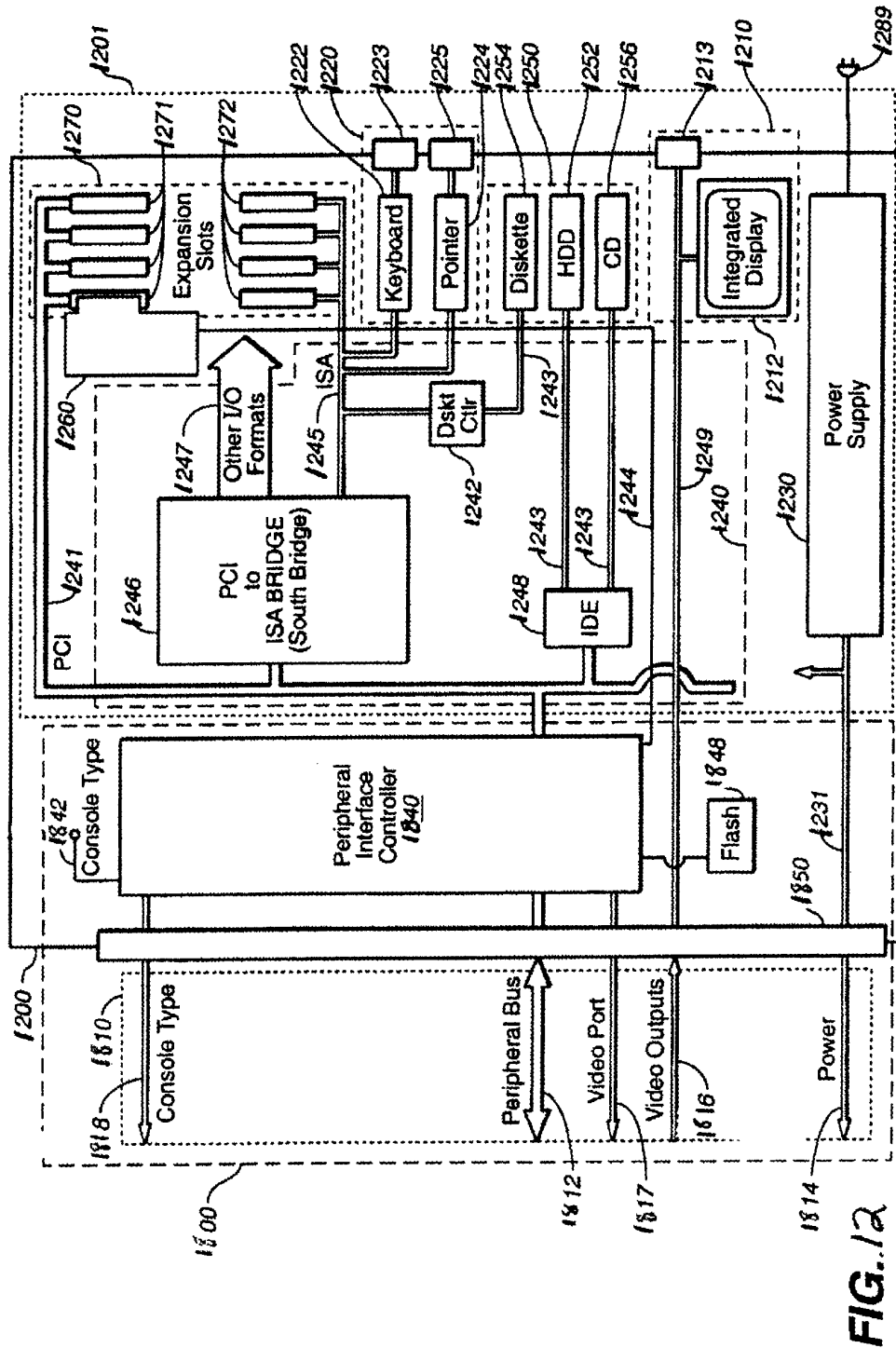


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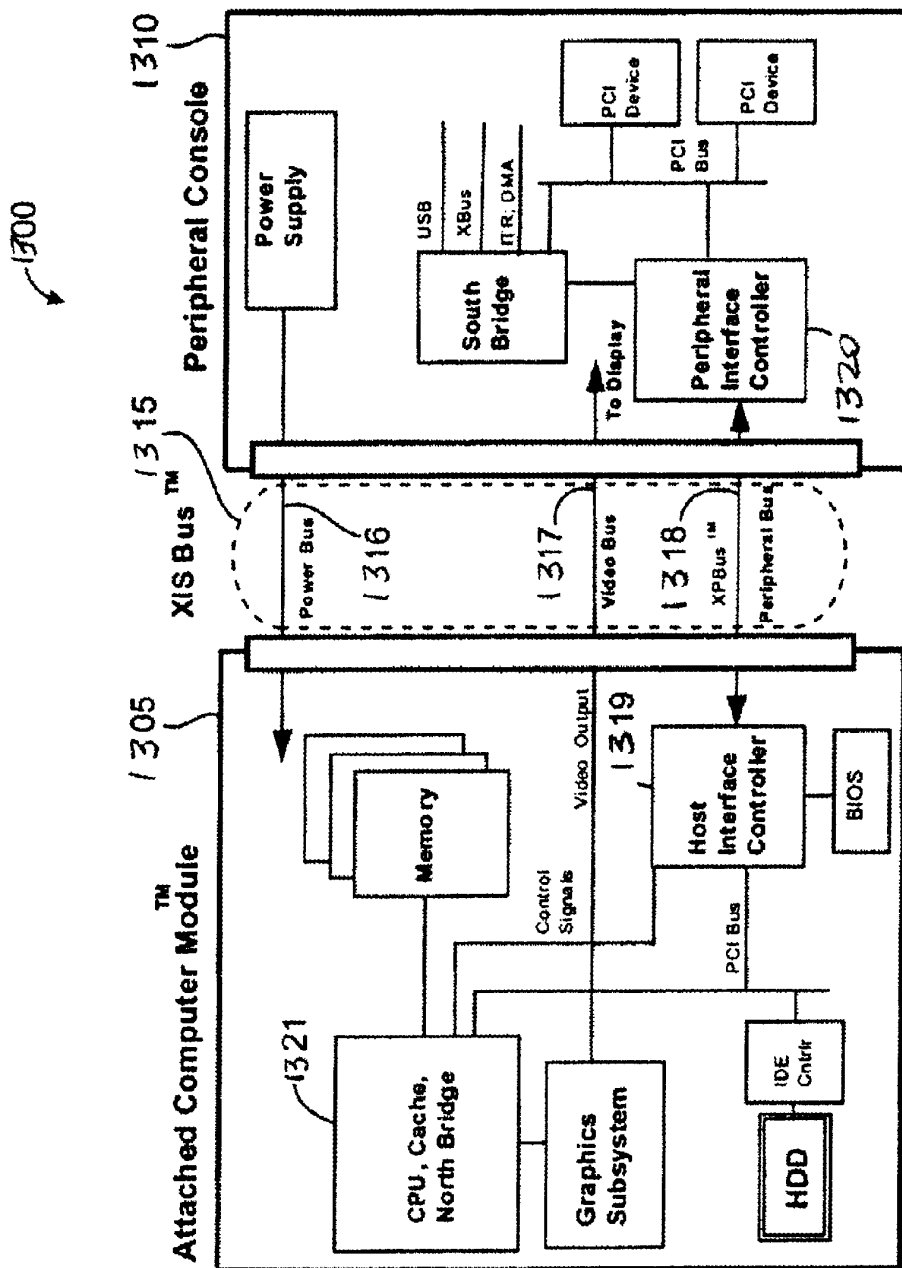


FIG. 13

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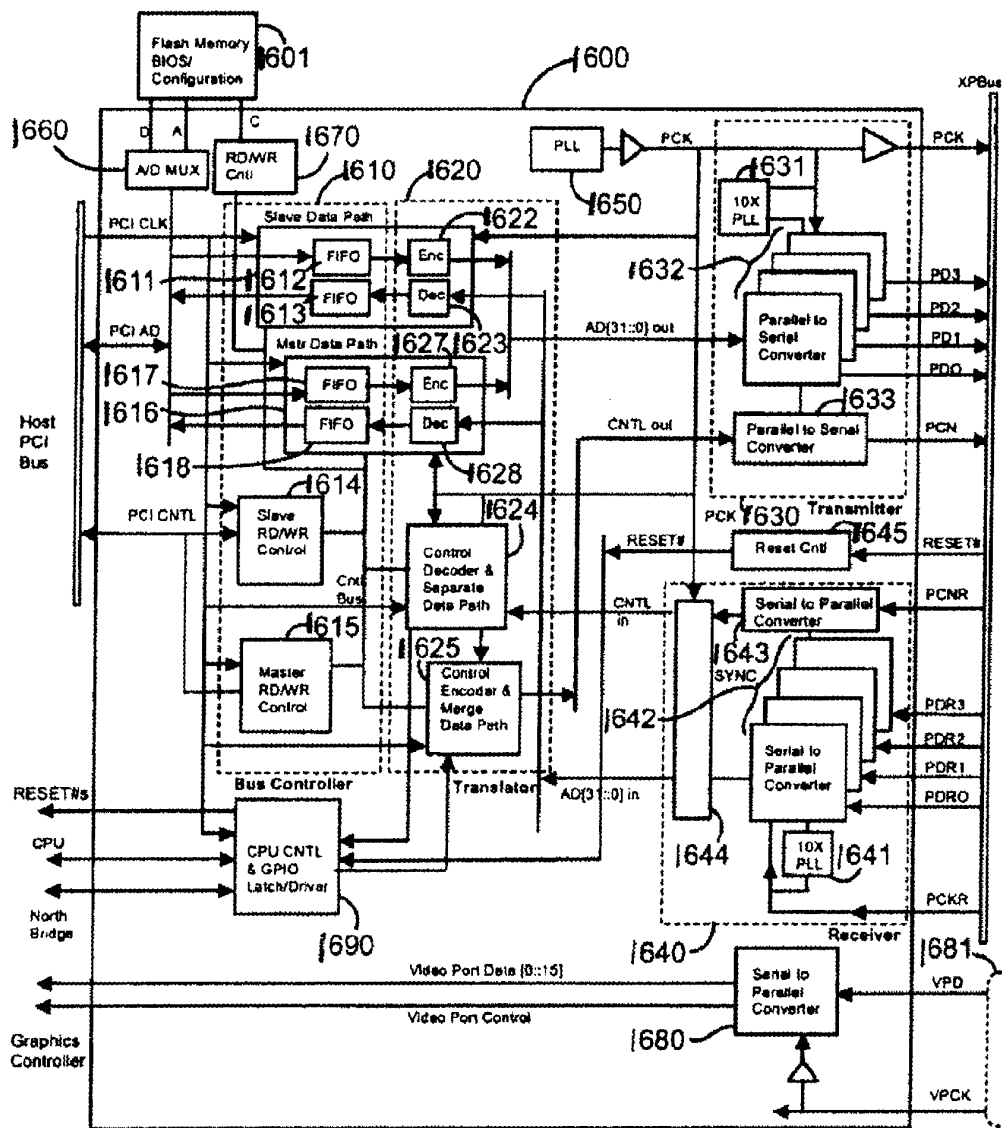


FIG. 14

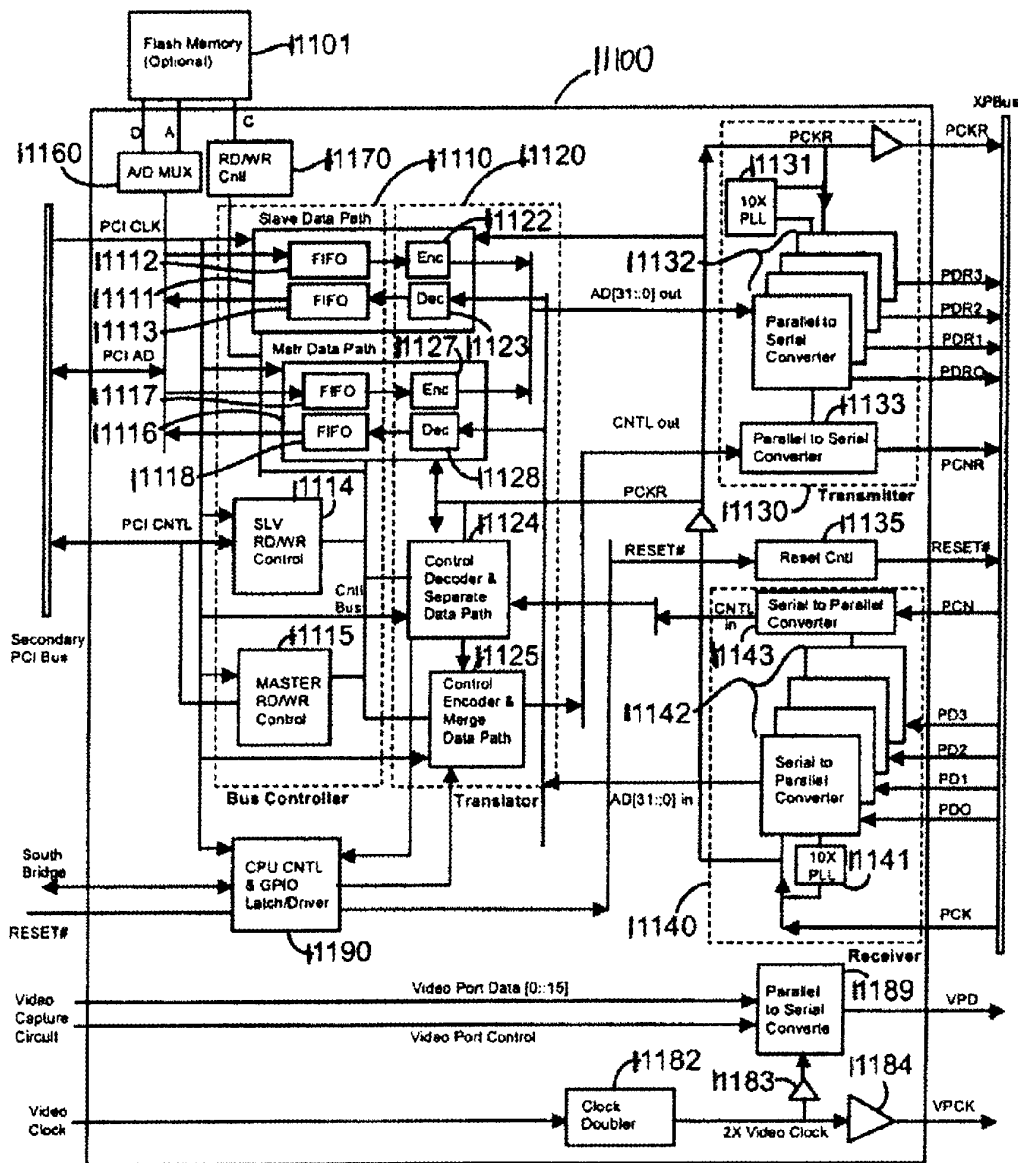


FIG. 15

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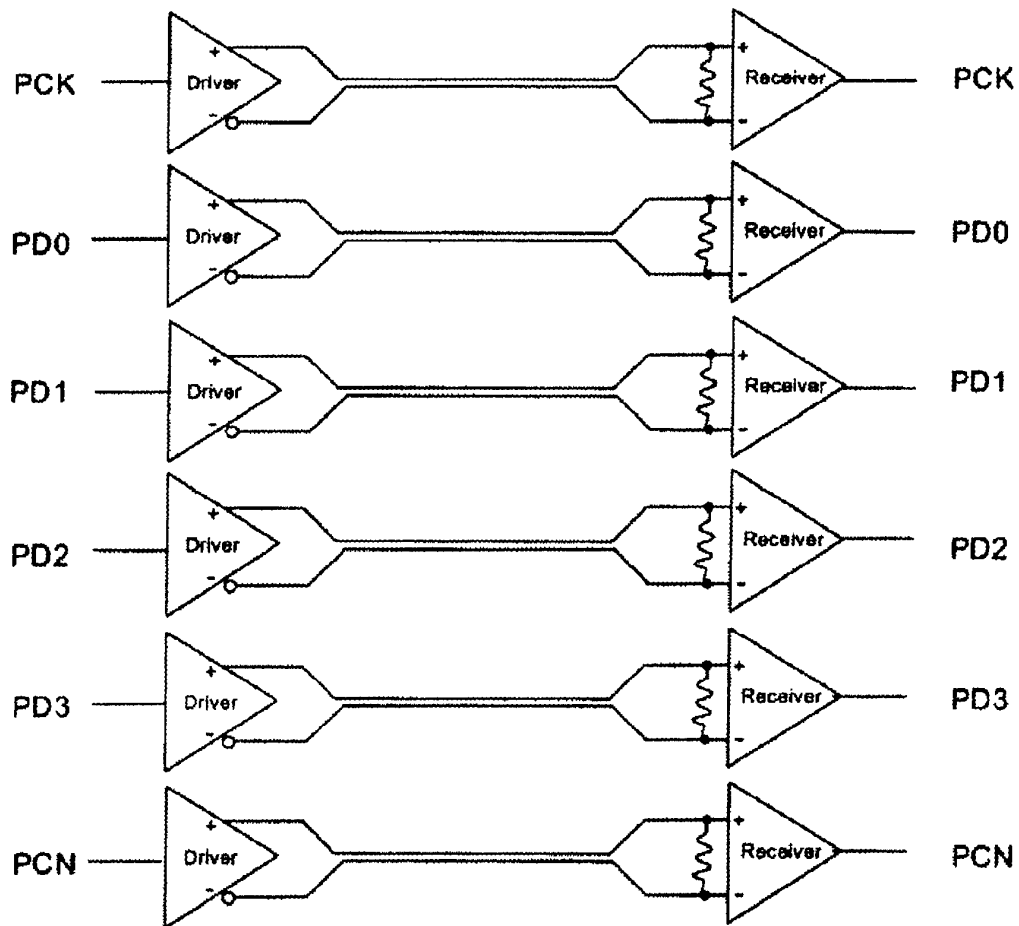


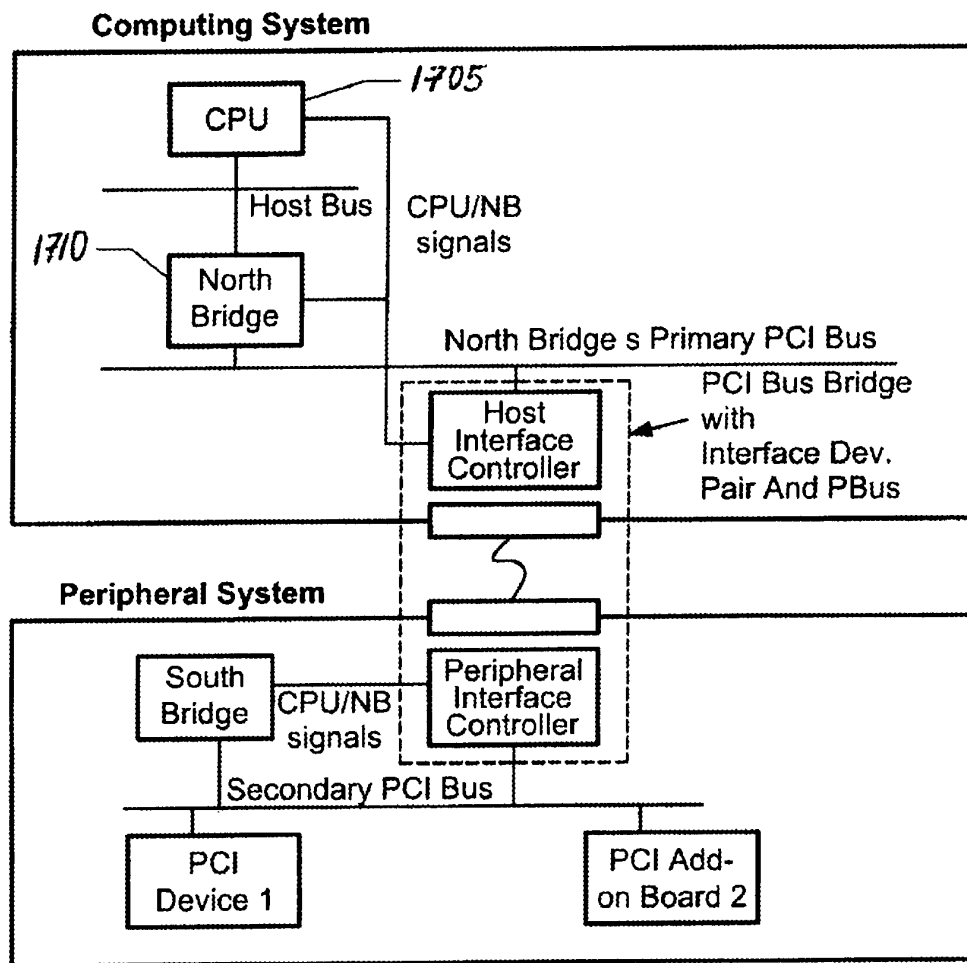
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**FIGURE 17**

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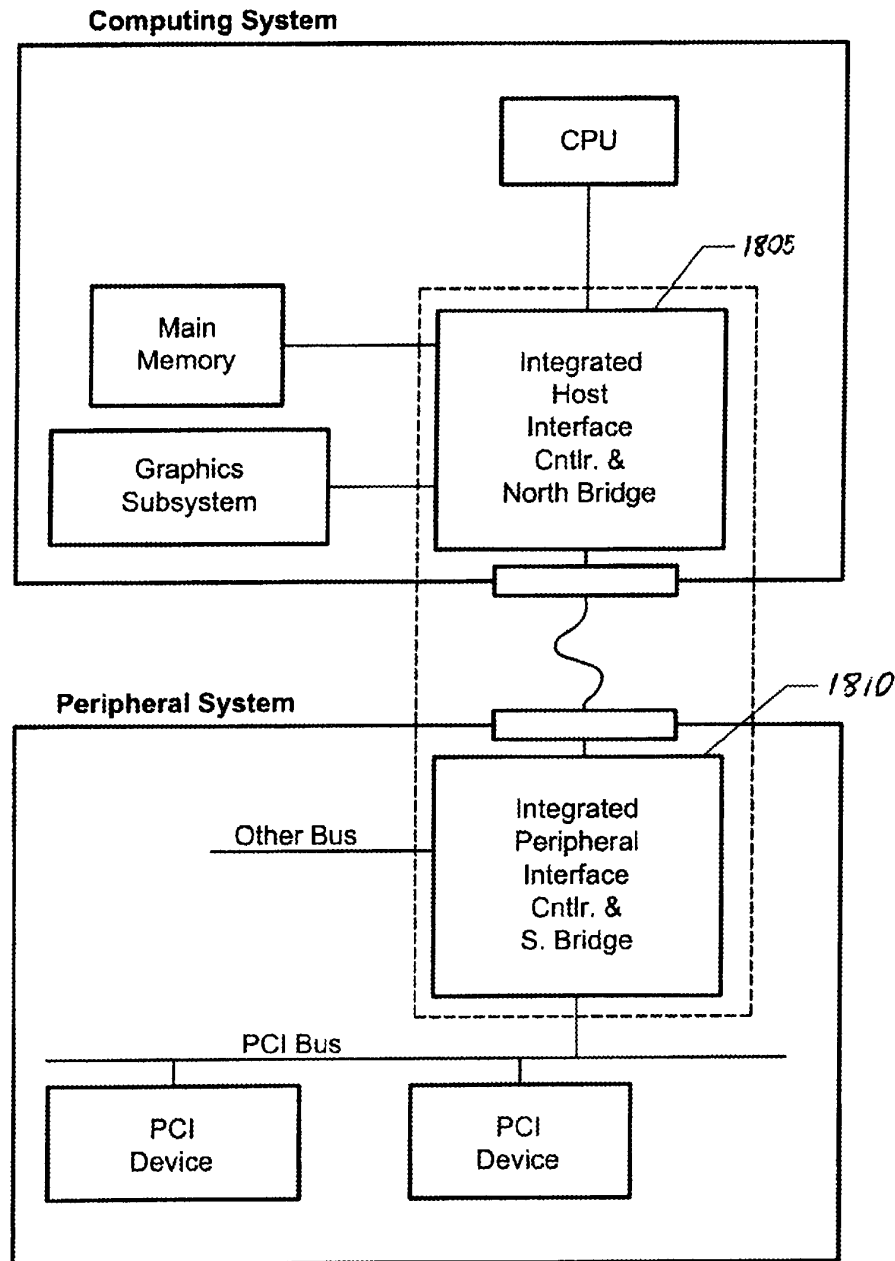


FIGURE 18



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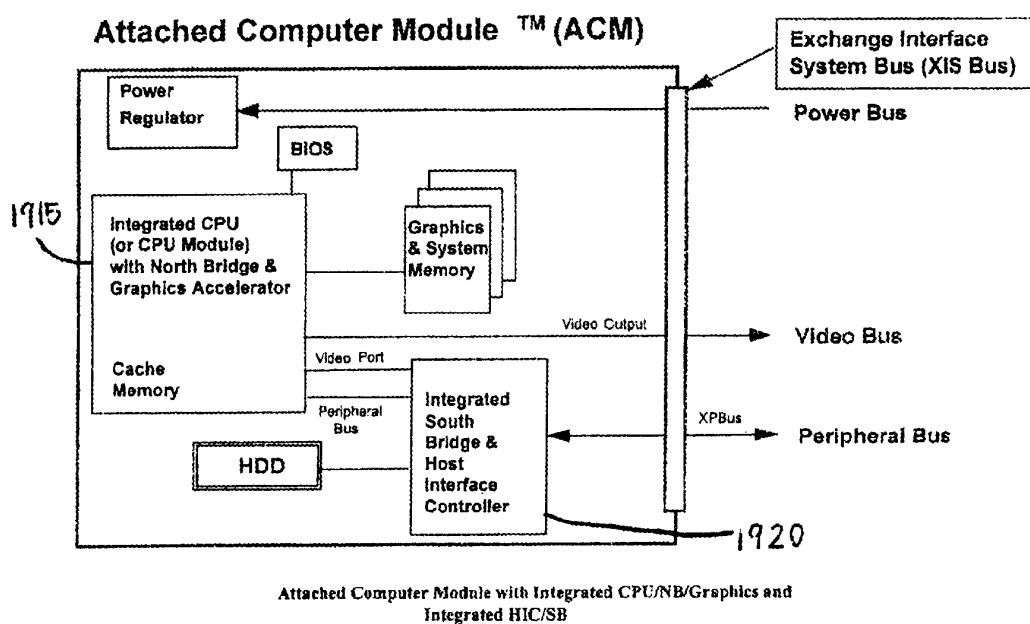


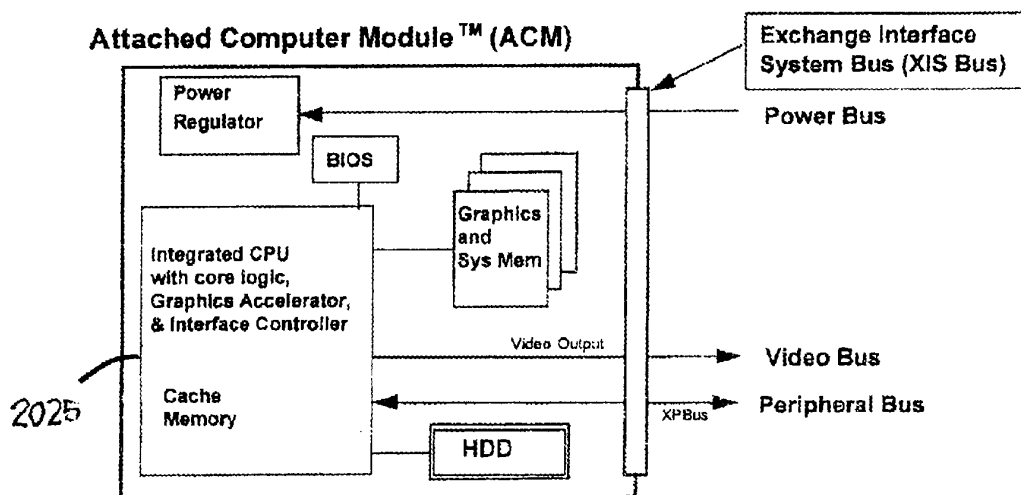
FIG. 19

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Attached Computer Module with Single Chip fully integrated: CPU, Cache, Core logic, Graphics controller and Interface controller

FIG. 20

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Pin No.	Symbol	Signal	Standard	Description
P2	PDR0 +	LVDS		Peripheral data reverse 0 +
P3	PDR0 -	LVDS		Peripheral data reverse 0 -
P5	PDR1 +	LVDS		Peripheral data reverse 1 +
P6	PDR1 -	LVDS		Peripheral data reverse 1 -
P8	PDR2 +	LVDS		Peripheral data reverse 2 +
P9	PDR2 -	LVDS		Peripheral data reverse 2 -
P11	PCKR +	LVDS		Peripheral clock reverse +
P12	PCKR -	LVDS		Peripheral clock reverse -
P15	PDR3 +	LVDS		Peripheral data reverse 3 +
P16	PDR3 -	LVDS		Peripheral data reverse 3 -
P18	PCNR +	LVDS		Peripheral control reverse +
P19	PCNR -	LVDS		Peripheral control reverse -
P24	PD0 +	LVDS		Peripheral data 0 +
P25	PD0 -	LVDS		Peripheral data 0 -
P27	PD1 +	LVDS		Peripheral data 1 +
P28	PD1 -	LVDS		Peripheral data 1 -
P30	PD2 +	LVDS		Peripheral data 2 +
P31	PD2 -	LVDS		Peripheral data 2 -
P33	PCK +	LVDS		Peripheral clock +
P34	PCK -	LVDS		Peripheral clock -
P37	PD3 +	LVDS		Peripheral data 3 +
P38	PD3 -	LVDS		Peripheral data 3 -
P40	PCN +	LVDS		Peripheral control +
P41	PCN -	LVDS		Peripheral control -
P13	Config 0	Static	3.3v or GND	Configuration bit 0
P35	Config 1	Static	3.3v or GND	Configuration bit 1
P14,P7,P10, P17,P23,P26, P32,P36,P39	GND		GND	Ground

FIG. 21

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Pin No.	Symbol	Signal	Standard	Description
V2	Red Video	Analog		Video
V4	Green Video	Analog		Video
V6	Blue Video	Analog		Video
V8	HSYNC			Horizontal Sync
V9	VSNC			Vertical Sync
V11	DDC2 SCL		VESA DDC std 2	DDC Clock
V12	DDC2 SDA		VESA DDC std 2	DDC Data
V14	TV-CV/CNTL 0			TV Composite Video
V15	SV Y/CNTL 1		Super Video	SV Luminance or Control 1
V16	SV C/CNTL 2		Super Video	SV Chrominance or Control 2
V24	D0 +	TMD5	VESA P & D	Data 0 +
V25	D0 -	TMD5	VESA P & D	Data 0 -
V27	CLK +	TMD5	VESA P & D	Clock +
V28	CLK -	TMD5	VESA P & D	Clock -
V30	D1 +	TMD5	VESA P & D	Data 1 +
V31	D1 -	TMD5	VESA P & D	Data 1 -
V33	D2 +	TMD5	VESA P & D	Data 2 +
V34	D2 -	TMD5	VESA P & D	Data 2 -
V37	VPCK +	LVDS		Video Port Pixel Clock +
V38	VPCK -	LVDS		Video Port Pixel Clock -
V40	VPD +	LVDS		Video Port Pixel Data +
V41	VPD -	LVDS		Video Port Pixel Data -
V13	Config 2		3.3v or GND	Configuration bit 2
V35	Config 3		3.3v or GND	Configuration bit 3
V1, V3, V5, V7, V10, V23, V26, V29, V32, V36, V39, V42, V43, V44	GND		GND	Ground

FIG. 22

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	Symbol	Signal	Data Rate	Description
1	PD0 RTN			GND
2	PD0 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 0 +
3	PD0 -			Computer to Peripheral LVDS Data 0 -
4	PD1 RTN			GND
5	PD1 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 1 +
6	PD1 -			Computer to Peripheral LVDS Data 1 -
7	PD2 RTN			GND
8	PD2 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 2 +
9	PD2 -			Computer to Peripheral LVDS Data 2 -
10	PD3 RTN			GND
11	PD3 +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Data 3 +
12	PD3 -			Computer to Peripheral LVDS Data 3 -
13	PCK RTN			GND
14	PCK +	Clock	Clock rate	Computer to Peripheral LVDS Clock +
15	PCK -			Computer to Peripheral LVDS Clock -
16	PCN RTN			GND
17	PCN +	Synch. To PCK	10 x clock rate	Computer to Peripheral LVDS Control +
18	PCN -			Computer to Peripheral LVDS Control -
19	PDR0 RTN			GND
20	PDR0 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 0 +
21	PDR0 -			Peripheral to Computer LVDS Data 0 -
22	PDR1 RTN			GND
23	PDR1 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 1 +
24	PDR1 -			Peripheral to Computer LVDS Data 1 -
25	PDR2 RTN			GND
26	PDR2 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 2 +
27	PDR2 -			Peripheral to Computer LVDS Data 2 -
28	PDR3 RTN			GND
29	PDR3 +	Synch. To PCKR	10 x clock rate	Peripheral to Computer LVDS Data 3 +
30	PDR3 -			Peripheral to Computer LVDS Data 3 -
31	PCKR RTN			GND
32	PCKR +	Reverse Dir. Clock	Clock rate	Peripheral to Computer LVDS Clock +
33	PCKR -			Peripheral to Computer LVDS Clock -
34	PCNR RTN			GND
35	PCNR +	Synch. To PCKR	10 x Clock rate	Peripheral to Computer LVDS Control +
36	PCNR -			Peripheral to Computer LVDS Control -
37	RESET#		Asynchronous	Reset

FIG. 23

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ID bits (P0 P1 P2 P3)	Data Packet Type
XX00	PCI 1st address/data segment
XX10	PCI 2nd address/data segment
0001	Control 1st segment with PCI response
1001	Control 1st segment without PCI response
0101	Control 2nd segment with PCI response
1101	Control 2nd segment without PCI response
0011	Reserved
1011	Reserved
0111	Initialization
1111	NOOP

FIG. 24



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DATA SECURITY METHOD AND DEVICE  
FOR COMPUTER MODULES

**Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.**

*Notice: More than one reissue application has been filed for the reissue of U.S. Pat. No. 6,643,777. The reissue applications are U.S. application Ser. No. 11/056,604 (a parent reissue application), Ser. No. 11/545,056 (which is a reissue continuation of the parent reissue application), Ser. No. 12/561,138 (which is a reissue continuation of the parent reissue application), Ser. No. 13/294,108 (which is a reissue continuation of U.S. application Ser. No. 12/561,138), and Ser. No. 13/562,210 (the present application, which is a reissue continuation of U.S. application Ser. No. 13/294,108).*

*This application is a reissue continuation of U.S. application Ser. No. 13/294,108, which is a reissue continuation of U.S. application Ser. No. 12/561,138, which is a reissue continuation of U.S. application Ser. No. 11/056,604, which is a reissue of U.S. Pat. No. 6,643,777, which are incorporated herein by reference.*

## BACKGROUND OF THE INVENTION

The present invention relates to computing devices. More particularly, the present invention provides a method and device for securing a personal computer or set-top box. Merely by way of example, the present invention is applied to a modular computing environment for desk top computers, but it will be recognized that the invention has a much wider range of applicability. It can be applied to other portable or modular computing applications.

Many desktop or personal computers, which are commonly termed PCs, have been around and used for over ten years. The PCs often come with state-of-art microprocessors such as the Intel Pentium™ microprocessor chips. They also include a hard or fixed disk drive including memory in the giga-byte range. Additionally, the PCs often include a random access memory integrated circuit device such as a dynamic random access memory device, which is commonly termed DRAM. The DRAM devices now provide up to millions of memory cells (i.e., mega-bit) on a single slice of silicon. PCs also include a high resolution display such as cathode ray tubes or CRTs. In most cases, the CRTs are at least 15 inches or 17 inches or 19 inches in diameter. High resolution flat panel displays are also used with PCs.

Many external or peripheral devices can be used with the PCs. Among others, these peripheral devices include mass storage devices such as a Zip™ Drive product sold by Iomega Corporation of Utah. Other storage devices include external hard drives, tape drives, and others. Additional devices include communication devices such as a modem, which can be used to link the PC to a wide area network of computers such as the Internet. Furthermore, the PC can include output devices such as a printer and other output means. Moreover, the PC can include special audio output devices such as speakers the like.

PCs also have easy to use keyboards, mouse input devices, and the like. The keyboard is generally configured similar to a typewriter format. The keyboard also has the length and width for easily inputting information by way of keys to the

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computer. The mouse also has a sufficient size and shape to easily move a cursor on the display from one location to another location.

Other types of computing devices include portable computing devices such as "laptop" computers and the like. Although somewhat successful, laptop computers have many limitations. These computing devices have expensive display technology. In fact, these devices often have a smaller flat panel display that has poor viewing characteristics. Additionally, these devices also have poor input devices such as smaller keyboards and the like. Furthermore, these devices have limited common platforms to transfer information to and from these devices and other devices such as PCs.

Up to now, there has been little common ground between these platforms including the PCs and laptops in terms of upgrading, ease-of-use, cost, performance, and the like. Many differences between these platforms, probably somewhat intentional, has benefited computer manufacturers at the cost of consumers. A drawback to having two separate computers is that the user must often purchase both the desktop and laptop to have "total" computing power, where the desktop serves as a "regular" computer and the laptop serves as a "portable" computer. Purchasing both computers is often costly and runs "thousands" of dollars. The user also wastes a significant amount of time transferring software and data between the two types of computers. For example, the user must often couple the portable computer to a local area network (i.e., LAN), to a serial port with a modem and then manually transfer over files and data between the desktop and the portable computer. Alternatively, the user often must use floppy disks to "zip" up files and programs that exceed the storage capacity of conventional floppy disks, and transfer the floppy disk data manually.

Another drawback with the current model of separate portable and desktop computer is that the user has to spend money to buy components and peripherals the are duplicated in at least one of these computers. For example, both the desktop and portable computers typically include hard disk drives, floppy drives, CD-ROMs, computer memory, host processors, graphics accelerators, and the like. Because program software and supporting programs generally must be installed upon both hard drives in order for the user to operate programs on the road and in the office, hard disk space is often wasted.

One approach to reduce some of these drawbacks has been the use of a docking station with a portable computer. Here, the user has the portable computer for "on the road" use and a docking station that houses the portable computer for office use. The docking station typically includes a separate monitor, keyboard, mouse, and the like and is generally incompatible with other desktop PCs. The docking station is also generally not compatible with portable computers of other vendors. Another drawback to this approach is that the portable computer typically has lower performance and functionality than a conventional desktop PC. For example, the processor of the portable is typically much slower than processors in dedicated desktop computers, because of power consumption and heat dissipation concerns. As an example, it is noted that at the time of drafting of the present application, some top-of-the-line desktops include 400 MHz processors, whereas top-of-the-line notebook computers include 266 MHz processors.

Another drawback to the docking station approach is that the typical cost of portable computers with docking stations can approach the cost of having a separate portable computer and a separate desktop computer. Further, as noted above, because different vendors of portable computers have propri-

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etary docking stations, computer users are held captive by their investments and must rely upon the particular computer vendor for future upgrades, support, and the like.

To date, most personal computers provide data file security through software only. A wide variety of removable storage media are available for a personal computer. These removable media do not provide any access security protection in hardware. Data encryption program often must be used for protection. Such program is cumbersome to handle for the user requiring extra cost and time. Data encryption is more commonly used for communication over an unprotected network or the Internet. Having a large number of frequently used files managed by encryption software is not practical. Without software security program, any file can be read and copied illegally from a hard disk drive on a PC or any removable media.

PC architecture generally allows freedom of data flow between memory and peripheral devices within the allowed memory and I/O address spaces. In conventional PC architecture, a peripheral bus, i.e. PCI bus, is used to control all data transactions among peripheral devices. PCI bus allows any device to be a bus master and perform data transaction with another device. Also when a software program is in control, it can move data between any two devices. There is no hardware or protocol security mechanism on a standard peripheral bus such as PCI Bus to detect or block data transactions. Operating system may have individual files read or write protected. These types of special security feature require significant additional user interaction to control. This is too cumbersome for a typical user to manage. There is no mechanism in current PCs to allow access to the primary hard disk drive and yet prevent copying of its content. The conventional PC is a single machine that does not have a mechanism to perform security ID matching in hardware.

Thus, what is needed are computer systems that provide improved security features to prevent illegal or unauthorized access to information.

## SUMMARY OF THE INVENTION

According to the present invention, a technique including a method and device for securing a computer module in a computer system is provided. In an exemplary embodiment, the present invention provides a security system for an attached computer module ("ACM"). In an embodiment, the ACM inserts into a computer module bay (CMB) within a peripheral console to form a functional computer. A security program reads an identification number in a security memory device to determine a security level of the ACM according to one embodiment.

In a specific embodiment, the present invention provides a system for secured information transactions. The system has a console (e.g., computer housing) comprising a peripheral controller housed in the console; and a security memory device (e.g., flash memory device) coupled to the peripheral controller. The system also has an attached computer module (i.e., a removable module with memory and microprocessor) coupled to the console. The attached computer module has a host interface controller housed within the attached computer module to interface to the security memory device through the peripheral controller.

In an alternative embodiment, the present invention provides a security protection method for a computer module. The method includes steps or acts of inserting the computer module into a console. Once the module has been inserted, the method initiates a security program in the module to read a security identification of the console and to read a security

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identification of the computer module. Based upon a relationship of the console identification and the computer module identification, a predetermined security status is determined from, for example, a look up table or the like. The method then selects the predetermined security status, which can be one of many. The method then operates the computer module based upon the security status.

In a further alternative embodiment, the present invention provides a method for identifying a user for a computer module. The method includes inserting a computer module into a console; and initiating a security program in memory of the computer module. The method prompts a plurality of input fields corresponding to respective input information on a user interface to be provided by a user of the computer module. Next, the method inputs the input information into the user interface of the computer module. The input information includes a user (e.g., owner) name, a user (e.g., owner) password, a business name, a business password, and a location.

Still further, the present invention provides a system for secured information transactions, e.g., data security, electronic commerce, private communications. The system includes a console comprising a peripheral controller housed in the console. A user identification input device (e.g., keyboard, retinal reader, finger print reader, voice recognition unit) is coupled to the peripheral controller. The user identification input device is provided for user identification data of the user. The system has an attached computer module coupled to the console. The attached computer module has a security memory device (e.g., flash memory device) stored with the user identification data.

Numerous benefits are achieved using the present invention over previously existing techniques. The present invention provides mechanical and electrical security systems to prevent theft or unauthorized use of the computer system in a specific embodiment. Additionally, the present invention substantially prevents accidental removal of the ACM from the console. In some embodiments, the present invention prevents illegal or unauthorized use during transit. The present invention is also implemented using conventional technologies that can be provided in the present computer system in an easy and efficient manner. Depending upon the embodiment, one or more of these benefits can be available. These and other advantages or benefits are described throughout the present specification and are described more particularly below.

These and other embodiments of the present invention, as well as its advantages and features, are described in more detail in conjunction with the text below and attached FIGS.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a simplified diagram of a computer system according to an embodiment of the present invention;

FIG. 2 is a simplified diagram of a computer module according to an embodiment of the present invention;

FIG. 3 is a simplified top-view diagram of a computer module according to an embodiment of the present invention;

FIG. 4 is a simplified illustration of security systems according to embodiments of the present invention;

FIG. 5 is a simplified diagram of a computer module in a console according to an embodiment of the present invention;

FIG. 6 is a simplified diagram of a security method for a module according to an embodiment of the present invention; and

FIG. 7 is a simplified diagram of a method according to an embodiment of the present invention.

FIG. 8 is a simplified diagram of a system 800 according to an alternative embodiment of the present application.

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FIG. 9 depicts a peripheral console configuration.

FIG. 10 is a block diagram of one embodiment of a computer system employing the present invention.

FIG. 11 is a block diagram of an attached computing module (ACM).

FIG. 12 is a block diagram of a peripheral console (PCON).

FIG. 13 is a block diagram of one embodiment of a computer system using the interface of the present invention.

FIG. 14 is a detailed block diagram of one embodiment of the host interface controller of the present invention.

FIG. 15 is a detailed block diagram of one embodiment of the PIC of the present invention.

FIG. 16 is a schematic diagram of the signal lines PCK, PD0 to PD3, and PCN.

FIG. 17 is a partial block diagram of a computer system using the interface of the present invention as a bridge between the north and south bridges of the computer system.

FIG. 18 is a partial block diagram of a computer system in which the north and south bridges are integrated with the host and peripheral interface controllers, respectively.

FIG. 19 shows an attached computer module with Integrated CPU/NB/Graphics and Integrated HIC/SB.

FIG. 20 shows an attached computer module with single chip fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

FIGS. 21 and 22 are tables including the pin number, symbol, signal, standard and description for the pins on the peripheral and video connectors, respectively.

FIG. 23 is a table showing the symbols, signals, data rate and description of signals in a first embodiment of the XPBus.

FIG. 24 is a table showing different types of first nibbles and their corresponding data packet types.

#### DESCRIPTION OF THE SPECIFIC EMBODIMENTS

FIG. 1 is a simplified diagram of a computer system 1 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The computer system 1 includes an attached computer module (i.e., ACM) 10, a desktop console 20, among other elements. The computer system is modular and has a variety of components that are removable. Some of these components (or modules) can be used in different computers, workstations, computerized television sets, and portable or laptop units.

In the present embodiment, ACM 10 includes computer components, as will be described below, including a central processing unit ("CPU"), IDE controller, hard disk drive, computer memory, and the like. The computer module bay (i.e., CMB) 40 is an opening or slot in the desktop console. The CMB houses the ACM and provides communication to and from the ACM. The CMB also provides mechanical protection and support to ACM 10. The CMB has a mechanical alignment mechanism for mating a portion of the ACM to the console. The CMB further has thermal heat dissipation sinks, electrical connection mechanisms, and the like. Some details of the ACM can be found in co-pending U.S. patent application Ser. Nos. 09/149,882 and 09/149,548 filed Sep. 8, 1998 commonly assigned, and hereby incorporated by reference for all purposes.

In a preferred embodiment, the present system has a security system, which includes a mechanical locking system, an electrical locking system, and others. The mechanical locking

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system includes at least a key 11. The key 11 mates with key hole 13 in a lock, which provides a mechanical latch 15 in a closed position. The mechanical latch, in the closed position, mates and interlocks the ACM to the computer module bay. The mechanical latch, which also has an open position, allows the ACM to be removed from the computer module bay. Further details of the mechanical locking system are shown in the FIG. below.

FIG. 2 is a simplified diagram of a computer module 10 according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. Some of the reference numerals are similar to the previous FIG. for easy reading. The computer module 10 includes key 11, which is insertable into keyhole 13 of the lock. The lock has at least two position, including a latched or closed position and an unlatched or open position. The latched position secures the ACM to the computer module bay. The unlatched or open position allows the ACM to be inserted into or removed from the computer bay module. As shown, the ACM also has a slot or opening 14, which allows the latch to move into and out of the ACM. The ACM also has openings 17 in the backside for an electrical and/or mechanical connection to the computer module bay, which is connected to the console.

FIG. 3 is a simplified top-view diagram 10 of a computer module for computer system according to an embodiment of the present invention. This diagram is merely an illustration and should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The layout diagram illustrates the top-view of the module 10, where the backside components (e.g., Host Interface Controller) are depicted in dashed lines. The layout diagram has a first portion, which includes a central processing unit ("CPU") module 400, and a second portion, which includes a hard drive module 420. A common printed circuit board 437 houses these modules and the like. Among other features, the ACM includes the central processing unit module 400 with a cache memory 405, which is coupled to a north bridge unit 421, and a host interface controller 401. The host interface controller includes a lock control 403. As shown, the CPU module is disposed on a first portion of the attached computer module, and couples to connectors 17. Here, the CPU module is spatially located near connector 17.

The CPU module can use a suitable microprocessing unit, microcontroller, digital signal processor, and the like. In a specific embodiment, the CPU module uses, for example, a 400 MHz Pentium II microprocessor module from Intel Corporation and like microprocessors from AMD Corporation, Cyrix Corporation (now National Semiconductor Corporation), and others. In other aspects, the microprocessor can be one such as the Compaq Computer Corporation Alpha Chip, Apple Computer Corporation PowerPC G3 processor, and the like. Further, higher speed processors are contemplated in other embodiments as technology increases in the future.

In the CPU module, host interface controller 401 is coupled to BIOS/flash memory 405. Additionally, the host interface controller is coupled to a clock control logic, a configuration signal, and a peripheral bus. The present invention has a host interface controller that has lock control 403 to provide security features to the present ACM. Furthermore, the present invention uses a flash memory that includes codes to provide password protection or other electronic security methods.

The second portion of the attached computer module has the hard drive module 420. Among other elements, the hard



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drive module includes north bridge **421**, graphics accelerator **423**, graphics memory **425**, a power controller **427**, an IDE controller **429**, and other components. Adjacent to and in parallel alignment with the hard drive module is a personal computer interface ("PCI") bus **431**, **432**. A power regulator **435** is disposed near the PCI bus.

In a specific embodiment, north bridge unit **421** often couples to a computer memory, to the graphics accelerator **423**, to the IDE controller, and to the host interface controller via the PCI bus. Graphics accelerator **423** typically couples to a graphics memory **423**, and other elements. IDE controller **429** generally supports and provides timing signals necessary for the IDE bus. In the present embodiment, the IDE controller is embodied as a 643U2 PCI-to IDE chip from CMD Technology, for example. Other types of buses than IDE are contemplated, for example EIDE, SCSI, USB, and the like in alternative embodiments of the present invention.

The hard drive module or mass storage unit **420** typically includes a computer operating system, application software program files, data files, and the like. In a specific embodiment, the computer operating system may be the Windows98 operating system from Microsoft Corporation of Redmond Washington. Other operating systems, such as WindowsNT, MacOS8, Unix, and the like are also contemplated in alternative embodiments of the present invention. Further, some typical application software programs can include Office98 by Microsoft Corporation, Corel Perfect Suite by Corel, and others. Hard disk module **420** includes a hard disk drive. The hard disk drive, however, can also be replaced by removable hard disk drives, read/write CD ROMs, flash memory, floppy disk drives, and the like. A small form factor, for example 2.5", is currently contemplated, however, other form factors, such as PC card, and the like are also contemplated. Mass storage unit **240** may also support other interfaces than IDE.

In a specific embodiment, the present invention provides a file and data protection security system and method for a removable computer module or ACM. ACM contains the primary hard disk drive (HDD) where the operating system, application programs, and data files reside. The security system is used to prevent illegal access and copying of any file residing on the HDD inside ACM. An ACM is a self-contained computing device that can be armed with security software and hardware to protect its owner's private files and data. ACM docks with a computer bay in a wide variety of peripheral consoles. The combined ACM and peripheral console function as a personal computer. A computer module interface bus connects ACM and peripheral device. In some embodiments, all ACM data passes through computer module interface (CMI) bus to reach any device in the peripheral console, i.e. floppy drive, removable media, secondary hard disk drive, modem, and others. CMI bus data transfer is controlled by a pair of interface controllers on either side of the bus. This partitioning of a personal computer offer a way of protecting against illegal access of data residing within ACM by guarding data transaction through the computer module interface bus.

In a specific embodiment, a secured ACM has an enclosure that includes the following components:

- 1) A CPU,
- 2) Main memory,
- 3) A primary Hard Disk Drive (HDD),
- 4) Operating System, application software, data files on primary HDD,
- 5) Interface circuitry and connectors to peripheral console,
- 6) Flash memory used for storing security code and ID,
- 7) Data detection and control circuitry to manage data flow to peripheral console,

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- 8) Circuit board connecting the above components, and others.

A peripheral console includes some of the following elements:

- 1) Input means, e.g. keyboard and mouse,
- 2) Display means, e.g. CRT monitor, or integrated LCD display,
- 3) Removable storage media subsystem, e.g. Floppy drive, CDROM drive,
- 4) Communication device, e.g. LAN or modem,
- 5) Computer Module Bay, interface device and connectors to ACM,
- 6) Flash memory with security ID,
- 7) Power supply or battery system, and other devices.

The Computer Module Bay (CMB) is an opening in a peripheral console that receives ACM. CMB provides mechanical protection and electrical connection to ACM. The Computer Module Interface bus is made up of 3 bus components: video bus, peripheral data bus, and power bus. Video Bus consists of video output of graphics devices, i.e. analog RGB and control signals for monitor, or digital video signals to drive flat panel displays. Power bus supplies the power for ACM. Peripheral data bus is a high speed, compressed, peripheral bridge bus managed by a Host Interface Controller in ACM and a peripheral Interface Controller in peripheral console. In some embodiments, all peripheral data transaction passes through the interface controllers.

The implementation of the secured ACM generally includes the following elements:

- 1) A programmable Flash memory controlled by the Peripheral Interface Controller containing the security ID for the peripheral console,
- 2) A programmable Flash memory controlled by the Host Interface Controller containing hardware specific security code and ID for the computer module,
- 3) A data detection and control circuitry within Host Interface Controller to detect and manage data going out of ACM, and
- 4) A low level hardware dependent security code to perform security ID matching, hardware programming to manage data flow,
- 5) A high-level security program to manage user interface, program security ID, program security level, and other functions.

The hardware and software implementation allow more flexibility in the level of security protection offered to an ACM owner. Some examples of security levels are:

- 1) No access—Security IDs do not match according to owner's requirement. The Host Interface Controller blocks all peripheral data traffic between ACM and peripheral console except for keyboard and mouse,
- 2) Peripheral Read-only—No files can be written to any peripheral devices. All peripheral devices in peripheral console are managed as Read-only devices. The primary hard disk drive in ACM can be accessed freely,
- 3) Limited access—Certain peripheral devices are allowed read/write access, i.e. modem, and other devices are Read-only, i.e. removable media devices,
- 4) Full access—No restriction, and others.

Upon power up, the low level security code is executed to compare security ID between the respective flash memory between ACM and peripheral console. Typical security ID can include:

- 1) User ID
- 2) User password
- 3) User Access privilege
- 4) Business ID

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- 5) Business password
- 6) Equipment ID
- 7) Equipment access privilege, and any other security IDs.

The user through the security program can activate different levels of password protection, which can be stored in a look up table. The company through the security program can control different levels of access privilege of a user, a business group, or equipment. The security code then program the security level allowed by the access privilege determined by the security ID matching result. For example, if an unidentified peripheral console is detected upon power up by the low level security code, e.g. a home unit, the access privilege can be set to Peripheral Read-only. With Read-only access privilege for all peripheral devices in peripheral console, the data detection and control circuitry is programmed to monitor all data traffic going to the peripheral console. Any memory block transfer to peripheral console will be detected and blocked. Under this mode, a user can use the computer with free access to the primary HDD in ACM. Any files can be read from other storage media in the peripheral console. But no files from the primary HDD can be copied to another media.

The data detection circuitry separately monitors peripheral bus operation type and memory address range being accessed. A specific address range for memory accesses and for I/O accesses can be programmed for the data detection circuitry to flag a match. A data blocking circuitry is triggered by the detection circuitry when a match occurs, and blank out the data that is being sent to the peripheral console. For the security system to be effective, a [temper] tamper resistant enclosure must be used to prevent removal of the hard disk drive and the flash memory inside ACM. Further details are shown throughout the present specification and more particularly below.

FIG. 4 is a simplified illustration of security systems 300 according to embodiments of the present invention. This illustration is merely an example, which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The systems show various examples of ways to implement the present invention. Here, a user relies upon certain consoles to access information. A company's shared portable console 325 can access general company information 303. Selected security identification information 315 is entered into the shared console to access the information via a network. The information generally includes owner, owner password, business, business password, console type, location, and access privilege information, which is displayed on a user display. The owner is generally the user name. Owner password is the user password. The business is the business unit name and business password is the business unit password. The console type can be portable for laptops, notebooks, and the like. Alternatively, the console type can be a desktop. The location generally specifies the desktop location or address for a networked system. Alternatively, the location can also be a home location. Access privilege can be categorized into many different levels. For example, the user can access general company information, but not information directed to other business units. The user can also be limited to access his/her private information, which is company related. Many other types of information can be restricted or accessed depending upon the embodiment.

Other types of access can be granted depending upon the consoles. For example, various consoles include, among others, a console at a user's home, e.g., "John Doe's," a console in the user's office 329, a console in a co-worker's office 331, which the user can access. The access from John Doe's home console uses security identification 317 and provides

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restricted access 305. The user's use of the module 307 can be from a variety of consoles and is accessed using security identification 319. Here, access privilege is private, which allows the user to access private personal information or private company information that the user has created. The user's access from his office relies upon security identification 321, which grants access to private information and general company information. The co-worker's console can also be used with security identification 323, which allows the user to access general company information but not private information of John Doe, for example. Depending upon the console used by the user, the security system can provide partial or full access to information on servers via network as well as an attached computer module. Information can also be limited to read only for certain information sources such as a server, a hard drive, a floppy drive, and others.

In a specific embodiment, the present invention also provides a security feature for the ACM 307. Here, the user of the ACM can be granted access to information in the ACM if the correct security identification information 319 is provided to the combination of ACM and console. Once the correct information is provided, the user can access the information on the hard drive of the ACM, which can be for private use. Other levels of access and security can also be provided depending upon the application.

FIG. 5 is a simplified diagram 500 of a computer module in a console according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The block diagram 500 includes an attached computer module 501 and a peripheral console 503, as well as other elements as desired. These elements have a variety of features such as those noted above, as well as others. In the present diagram, different reference numerals are used to show the operation of the present system.

The block diagram 500 illustrates attached computer module 501. The module 501 has a central processing unit 502, which communicates to a north bridge 541, by way of a CPU bus 527. The north bridge couples to main memory 523 via memory bus 529. The main memory can be any suitable high speed memory device or devices such as dynamic random access memory ("DRAM") integrated circuits and others. The DRAM includes at least 32 Meg. or 64 Meg. and greater of memory, but can also be less depending upon the application. Alternatively, the main memory can be coupled directly with the CPU in some embodiments. The north bridge also couples to a graphics subsystem 515 via bus 542. The graphics subsystem can include a graphics accelerator, graphics memory, and other devices. Graphics subsystem transmits a video signal to an interface connector, which couples to a display, for example.

The attached computer module also includes a primary hard disk drive 509 that serves as a main memory unit for programs and the like. The hard disk can be any suitable drive that has at least 2 GB and greater. As merely an example, the hard disk is a Marathon 2250 (2.25 GB, 2½ inch drive) product made by Seagate Corporation of Scotts Valley, but can be others. The hard disk communicates to the north bridge by way of a hard disk drive controller and bus lines 502 and 531. The hard disk drive controller couples to the north bridge by way of the host PCI bus 531, which connects bus 537 to the north bridge. The hard disk includes computer codes that implement a security program according to the present invention. Details of the security program are provided below.

The attached computer module also has a flash memory device 505 with a BIOS. The flash memory device 505 also has codes for a user password that can be stored in the device.

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The flash memory device generally permits the storage of such password without a substantial use of power, even when disconnected. As merely an example, the flash memory device has at least 512 kilobits or greater of memory, or 1 megabits or greater of memory. The flash memory device can store a security identification number or the like. The flash memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The flash memory generally has at least 128 kilobits storage cells or more. The flash memory can be any product such as a W29C020 product made by a company called Winbond of Taiwan, but can also be others. The flash memory cell and user identification will be more fully described below in reference to the FIGS. A host interface controller **507** communicates to the north bridge via bus **535** and host PCI bus. The host interface controller also has a data control **511**. Host interface controller **507** communicates to the console using bus **513**, which couples to connection **515**.

Peripheral console **503** includes a variety of elements to interface to the module **501**, display **551**, and network **553**. The console forms around south bridge **571**, which couples to bus **563**, which couples to bus **561**. Bus **561** is in communication with network card **555**, which is a local area network for Ethernet, for example. South bridge also couples through control **569** to peripheral interface controller **567**, which also communicates to bus **561**. Peripheral interface controller also couples to host interface controller through connection **515** and bus **513**. The peripheral console has a primary removable drive **559** connected to south bridge through bus **575**. South bridge also couples to secondary hard disk through bus **577**.

In a specific embodiment, the peripheral console also has a serial EEPROM memory device **575**, which is coupled to the peripheral interface controller. The memory device can store a security identification number or the like. The memory device is generally non-volatile and can preserve information even when the power is turned off, for example. The memory generally has at least 16 kilobits of storage cells or more. Preferably, the memory device is a 16 kilobit device or 64 megabit device or greater, depending upon the application. The memory can be any product such as a X24320 product made by a company called Xicor, but can also be others. The memory cell and user identification will be more fully described below in reference to the FIGS.

FIG. **6** is a simplified diagram of a security method **600** for a module according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method shows an example of how the present security method can be implemented. The present method uses a combination of software **601** and hardware **603**, which is in the computer module. A plurality of external devices can be accessed depending upon the embodiment. These external devices include a secondary hard drive **618**, a removable drive **619**, a network (e.g., LAN, modem) device **621**, and others. A keyboard **623** is also shown, which can act locally.

The software **601** includes an operating system **609**, application programs **607**, and a data security and initialization program **605**. Other programs can also exist. Additionally, some of these programs may not exist. Preferably, the data security and initialization program exists. This data security and initialization program is initiated once the attached computer module is inserted into the console. The program interface and oversees a variety of hardware features, which will

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be used to control access to the external devices, for example. Of course, the particular configuration of the software will depend upon the application.

Hardware features can be implemented using a primary hard disk **611** coupled to a CPU/cache combination, which includes a main memory. The main memory is often a volatile memory such as dynamic random access memory. Data from any one of the external devices can enter the CPU/cache combination. For example, the secondary hard disk memory and I/O address range data is transferred **624** to the CPU/cache combination. The removable drive memory and I/O address range data can also transfer **625** to the CPU/cache combination. The LAN memory and I/O address range data can also transfer **626** to the CPU/cache combination. Keyboard data can also transfer **627** to the CPU/cache combination. To write data from the module into any one of these external elements, the data security program interfaces with the data detection and control circuit to determine of such data should be transferred to any one of the external elements. As noted, the external elements include, among others, secondary hard disk, and removable drive. Here, the data security program checks the security identification number with other numbers to determine the security access level. There are many other ways that the present invention can be implemented. These methods are described more fully below.

FIG. **7** is a simplified diagram **700** of a method according to an embodiment of the present invention. This diagram is merely an illustration which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives. The present method begins at power up, which is step **701**. The present method reads a security code, which has been entered by a user, for example, in step **703**. The security code can be a string of characters, including numbers and letters. The security code is preferably a mixture of numbers and letters, which are at least about 6 characters in length, but is not limited.

The present method reads (step **703**) the security code, which has been entered. Next, the security code is compared with a stored code, which is in flash memory or the like (step **705**). If the compared code matches with the stored code, the method resumes to step **708**. Alternatively, the method goes to step **707** via branch **706** where no access is granted. When no access is granted, all data are blocked out from the user that attempts to log onto the system. Alternatively, the method determines if a certain level of access is granted, step **708**. Depending upon the embodiment, the present method can grant full access, step **710**, via branch **716**. The present method allows full access based upon information stored in the flash memory device. Alternatively, the method can allow the user to access a limited amount of information.

Here, the present method allows for at least one or more than two levels of access. In a specific embodiment, the present method allows for the user of the module to access peripheral storage (step **711**). The access privilege is read-only. The user can read information on the peripheral storage including hard disks and the like. Once the user accesses the storage, the method data control, step **719**, takes over, where the hardware prevents the user from accessing other information, step **721**. In a specific embodiment, the method can allow information to be removed from the peripheral storage. If the method allows for data to be removed, step **723**, the method goes through branch **731** to let data out, which can occur through the module. Alternatively, the method goes to block data (step **725**) via branch **733**. Depending upon the embodiment, the method returns to the decision block, step **723**. Alternatively, the method traverses branch **714** to a peripheral read-only process, step **712**. The read-only process



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programs data control, step 713. Next, the hardware takes over (step 715). The method blocks all data from being accessed by the user, step 717.

FIG. 8 is a simplified diagram of a system 800 according to an alternative embodiment of the present invention. This diagram is merely an example which should not limit the scope of the claims herein. One of ordinary skill in the art would recognize many other variations, modifications, and alternatives. The system 800 includes an attached computer module 801, which can be inserted into one of a plurality of console devices to create a “plug and play” operation. For example, the console device can be peripheral console 801 or peripheral console 805. Each peripheral console can have similar or different connection characteristics. Peripheral console 803 couples to a local area network using Ethernet 817. Peripheral console 805 couples to a DSL line 827 through a DSL modem 825. Other consoles can also be included to use other types of networks such as ADSL, Cable Modem, wireless, Token Ring, and the like.

As shown, the attached computer module has elements such as a memory region 807, which stores BIOS information, a security code, and a security identification number on a flash memory device or the like. The memory region couples to a central processing region 809, which can include CPU, chipset, cache memory, graphics, and a hard disk drive, as well as other features. The central processing region couples to a host interface controller, which interfaces the attached computer module to one of the peripheral consoles. Any of the above information can also be included in the attached computer module.

Each peripheral console also has a variety of elements. These elements include a region 813, 821, which has a flash memory device with a security identification number, a password, access information, access privileges, internet service provider access information, as well as other features, which were previously noted. The peripheral console also has an interface controller 815, 823, which couples region 813, 821, respectively to a networking device 817, 825. The networking device can be an Ethernet card 817, which allows communication to the local area network 819. Alternatively, the networking device can be a DSL modem 825, which allows communication to a DSL (or ADSL) phone line. Other types of networking device can also be used, depending upon the application.

Each console provides a selected connection based upon set of predefined factors. These factors include communication hardware information so that software in attached computer module can read and allow a connection to a network. Here, access information can be provided to the user. Information about connection information will also be included. This connection information includes telephone numbers, account numbers, passwords (local), or a company password. The console and module combination will take care of charges, etc. based upon time bases. Module will have credit card information, but will have security. In a specific embodiment, the module inserts into the console. The module then asks the console which hardware will be used. If the hardware is an Ethernet connect, the module configures connection information to access the Ethernet connection. Alternatively, if the hardware requires a DSL connection, the module configures connection information to access the DSL connection. Other configuration information such as company server information, password, can also be provided.

A personal computer system that comprises two physically separate units and the interconnection between them is disclosed. The first unit, an attached computing module (ACM), contains the core computing power and environment for a

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computer user. The second unit, a peripheral console (PCON), contains the power supply and primary input and output devices for the computer system. An ACM and a PCON are coupled with one another to form a fully functional personal computer system.

FIG. 9 depicts a notebook computer PCON configuration. The opening of the computer bay 992 is visible at the side of the PCON unit 900. The PCON 900 provides an integrated LCD display panel 910 as the user's primary display device. The PCON 900 provides an integrated keyboard 922 as the user's primary input device.

FIG. 10 is a block diagram of the components in one computer system. The computer system comprises an attached computer module (ACM) 1000, a peripheral console (PCON) 1001, and the interconnection apparatus 1003 between them. The ACM 1000 includes the central processing unit (CPU) 1010, system memory 1020, high performance devices 1050, primary mass storage 1030, and related interface and support circuitry 1040. The PCON 1001 includes primary display 1011, primary input 1021, secondary mass storage 1051, other devices 1061, expansion slots 1071, the primary power supply 1031, and related interface and support circuitry 1041. The interconnection apparatus 1003 includes circuitry to convey power and operational signals between the ACM 1000 and PCON 1001.

Within the ACM 1000, the CPU 1010 executes instructions and manipulates data stored in the system memory 1020. The CPU 1010 and system memory 1020 represent the user's core computing power. The core computing power may also include high performance devices 1050 such as advanced graphics processor chips that greatly increase overall system performance and which, because of their speed, need to be located close to the CPU 1010. The primary mass storage 1030 contains persistent copies of the operating system software, application software, configuration data, and user data. The software and data stored in the primary mass storage device 1030 represent the user's computing environment. Interface and support circuitry 1040 primarily includes interface chips and signal busses that interconnect the CPU 1010, system memory 1020, high performance devices 1050, and primary mass storage 1030. The interface and support circuitry 1040 also connects ACM-resident components with the ACM-to-PCON interconnection apparatus 1003 as needed.

Within the PCON 1001, the primary display component 1011 may include an integrated display device or connection circuitry for an external display device. This primary display device 1011 may be, for example, an LCD, plasma, or CRT display screen used to display text and graphics to the user for interaction with the operating system and application software. The primary display component 1011 is the primary output of the computer system, i.e., the paramount vehicle by which programs executing on the CPU 1010 can communicate toward the user.

The primary input component 1021 of the PCON 1001 may include an integrated input device or connection circuitry for attachment to an external input device. The primary input 1021 may be, for example, a keyboard, touch screen, keypad, mouse, trackball, digitizing pad, or some combination thereof to enable the user to interact with the operating system and application software. The primary input component 1021 is the paramount vehicle by which programs executing on the CPU 1010 receive signals from the user.

The PCON 1001 may contain secondary mass storage 1051 to provide additional high capacity storage for data and software. Secondary mass storage 1051 may have fixed or

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removable media and may include, for example, devices such as diskette drives, hard disks, CD-ROM drives, DVD drives, and tape drives.

The PCON 1001 may be enhanced with additional capability through the use of integrated "Other Devices" 1061 or add-on cards inserted into the PCON's expansion slots 1071. Examples of additional capability include sound generators, LAN connections, and modems. Interface and support circuitry 1041 primarily includes interface chips, driver chips, and signal busses that interconnect the other components within the PCON 1001. The interface and support circuitry 1041 also connects PCON-resident components with the ACM-to-PCON interconnection apparatus 1003 as needed.

Importantly, the PCON 1001 houses the primary power supply 1031. The primary power supply 1031 has sufficient capacity to power both the PCON 1001 and the ACM 1000 for normal operation. Note that the ACM 1000 may include a secondary "power supply" in the form, for example, of a small battery. Such a power supply would be included in the ACM 1000 to maintain, for example, a time-of-day clock, configuration settings when the ACM 1000 is not attached to a PCON, or machine state when moving an active ACM immediately from one PCON to another. The total energy stored in such a battery would, however, be insufficient to sustain operation of the CPU 1010 at its rated speed, along with the memory 1020 and primary mass storage 1030, for more than a fraction of an hour, if the battery were able to deliver the required level of electrical current at all.

FIG. 11 is a block diagram of an attached computing module (ACM) 1100. The physical ACM package 1100 contains the ACM functional components 1101 and the ACM side of the ACM-to-PCON Interconnection 1700. The ACM 1101 comprises a CPU component 1110, a system memory component 1120, a primary mass storage component 1130, a high performance devices components 1150, and an interface and support component 1140.

The ACM side of the ACM-to-PCON Interconnection 1700 comprises a Host Interface Controller (HIC) component 1720 and an ACM connector component 1730. The HIC 1720 and connector 1730 components couple the ACM functional components 1100 with the signals of an ACM-to-PCON interface bus 1710 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1710 comprises conveyance for electrical power 1714 and signals for a peripheral bus 1712, video 1716, video port 1717, and console type 1718. The preferred ACM-to-PCON Interconnection 1700 is described in detail in a companion U.S. patent application Ser. No. 09/149,882, entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," by the same inventor, filed on Sep. 8, 1998, and hereby incorporated by reference. The preferred ACM-to-PCON interconnection 1700 includes circuitry to transmit and receive parallel bus information from multiple signal paths as a serial bit stream on a single signal path. This reduces the number of physical signal paths required to traverse the interconnection 1700. Further, employing low-voltage differential signaling (LVDS) on the bit stream data paths provides very reliable, high-speed transmission across cables. This represents a further advantage of the present invention.

Clocking circuitry 1144 generates clock signals for distribution to other components within the ACM 1100 that require a timing and synchronization clock source. The CPU 1110 is one such component. Often, the total power dissipated by a CPU is directly proportional to the frequency of its main clock signal. The presently described embodiment of the ACM 1100 includes circuitry that can vary the frequency of the main

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CPU clock signal conveyed to the CPU 1110 via signal path 1162, in response to a signal received from the host interface controller (HIC) 1720 via signal path 1161. The generation and variable frequency control of clocking signals is well understood in the art. By varying the frequency, the power consumption of the CPU 1110 (and thus the entire ACM 1100) can be varied.

The variable clock rate generation may be exploited to match the CPU power consumption to the available electrical power. Circuitry in the host interface controller (HIC) 1720 of the presently described embodiment adjusts the frequency control signal sent via signal path 1161 to the clocking circuitry 1144, based on the "console type" information signal 1718 conveyed from the peripheral console (PCON) by the CPU-to-PCON interconnection 1700.

FIG. 12 is a block diagram of a peripheral console (PCON). A peripheral console couples with an ACM to form an operating personal computer system. The peripheral console (PCON) supplies an ACM with primary input, display, and power supply; the ACM supplies the core computing power and environment of the user. In the presently described embodiment the physical PCON package 1200 contains the PCON functional components 1201 and the PCON side of the ACM-to-PCON Interconnection 1800. The PCON functional components 1201 comprise primary display 1210, a primary input 1220, a primary power supply 1230, interface and support 1240, secondary mass storage 1250, other devices 1260, and expansion slots 1270.

The PCON side of the ACM-to-PCON Interconnection 1800 comprises a Peripheral Interface Controller (PIC) component 1840, a PCON connector component 1850, console-type component 1842, and flash memory device 1848. The PIC 1840 and connector 1850 components couple the PCON functional components 1201 with the signals of an ACM-to-PCON interface bus 1810 used to operatively connect an ACM with a PCON. The ACM-to-PCON interface bus 1810 comprises conveyance for electrical power 1814 and signals for a peripheral bus 1812, video 1816, video port 1817, and console-type 1818. The preferred ACM-to-PCON Interconnection 1800 is described in detail in the U.S. patent application entitled "A Communication Channel and Interface Devices for Bridging Computer Interface Buses," already incorporated herein by reference.

Connector component 1850 may be selected to mate directly with the connector component 1730 of an ACM (shown in FIG. 11). Alternatively, connector component 1850 may be selected to mate with, for example, the connector on one end of a cable intervening between the PCON and an ACM in a particular embodiment. The ACM-to-PCON interconnection described in the aforementioned companion patent application has the advantage of providing reliable signal conveyance across low cost cables.

Flash memory device 1848 provides non-volatile storage. This storage may be accessible to devices in both the ACM and the PCON, including the host interface controller and the peripheral interface controller 1840 to which it is connected. As such, flash memory 1848 may be used to store configuration and security data to facilitate an intelligent mating between an ACM and a PCON that needs no participation of the CPU.

The secondary mass storage component 1250 of the PCON functional circuitry 1201 of the presently described embodiment comprises diskette drive 1254, hard disk drive 1252, and CD-ROM drive 1256. Secondary mass storage 1250 generally provides low-cost, non-volatile storage for data files which may include software program files. Data files stored on secondary mass storage 1250 are not part of a computer

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user's core computing power and environment. Secondary mass storage 1250 may be used to store, for example, seldom used software programs, software programs that are used only with companion hardware devices installed in the same peripheral console 1200, or archival copies of data files that are maintained in primary mass storage 1130 of an ACM (shown in FIG. 11). Storage capacities for secondary mass storage 1250 devices may vary from the 1.44 megabytes of the 3.5-inch high density diskette drive 1254, to more than 10 gigabytes for a large format (5-inch) hard disk drive 1252. Hard disk drive 1252 employs fixed recording media, while diskette drive 1254 and CD-ROM drive 1256 employ removable media. Diskette drive 1254 and hard disk drive 1252 support both read and write operations (i.e., data stored on their recording media may be both recalled and modified) while CD-ROM drive 1256 supports only read operations.

Two PCI or PCI-like buses are interfaced using a non-PCI or non-PCI-like channel. PCI control signals are encoded into control bits, and the control bits, rather than the control signals that they represent, and are transmitted on the interface channel. At the receiving end, the control bits representing control signals are decoded back into PCI control signals prior to being transmitted to the intended PCI bus.

The fact that control bits rather than control signals are transmitted on the interface channel allows using a smaller number of signal channels and a correspondingly small number of conductive lines in the interface channel than would otherwise be possible. This is because the control bits can be more easily multiplexed at one end of the interface channel and recovered at the other end than control signals. This relatively small number of signal channels used in the interface channel allows using LVDS channels for the interface. As mentioned above, an LVDS channel is more cable friendly, faster, consumes less power, and generates less noise than a PCI bus channel. Therefore, an LVDS channel is advantageously used for the hereto unused purpose of interfacing PCI or PCI-like buses. The relatively smaller number of signal channels in the interface also allows using connectors having smaller pins counts. As mentioned above an interface having a smaller number of signal channels and, therefore, a smaller number of conductive lines is less bulky and less expensive than one having a larger number of signal channels. Similarly, connectors having a smaller number of pins are also less expensive and less bulky than connectors having a larger number of pins.

In one embodiment, the present invention encompasses an apparatus for bridging a first computer interface bus and a second computer interface bus, in a microprocessor based computer system where each of the first and second computer interface buses have a number of parallel multiplexed address/data bus lines and operate at a clock speed in a predetermined clock speed range having a minimum clock speed and a maximum clock speed. The apparatus comprises an interface channel having a clock channel and a plurality of bit channels for transmitting bits; a first interface controller coupled to the first computer interface bus and to the interface channel to encode first control signals from the first computer interface bus into first control bits to be transmitted on the interface channel and to decode second control bits received from the interface channel into second control signals to be transmitted to the first computer interface bus; and a second interface controller coupled to the interface channel and the second computer interface bus to decode the first control bits from the interface channel into third control signals to be transmitted on the second computer interface bus and to

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encode fourth control signals from the second computer interface bus into the second control bits to be transmitted on the interface channel.

In one embodiment, the first and second interface controllers comprise a host interface controller (HIC) and a peripheral interface controller (PIC), respectively, the first and second computer interface buses comprise a primary PCI and a secondary PCI bus, respectively, and the interface channel comprises an LVDS channel.

In a preferred embodiment, the interface channel has a plurality of serial bit channels numbering fewer than the number of parallel bus lines in each of the PCI buses and operates at a clock speed higher than the clock speed at which any of the bus lines operates. More specifically, the interface channel includes two sets of unidirectional serial bit channels which transmit data in opposite directions such that one set of bit channels transmits serial bits from the HIC to the PIC while the other set transmits serial bits from the PIC to the HIC. For each cycle of the PCI clock, each bit channel of the interface channel transmits a packet of serial bits.

The HIC and PIC each include a bus controller to interface with the first and second computer interface buses, respectively, and to manage transactions that occur therewith. The HIC and PIC also include a translator coupled to the bus controller to encode control signals from the first and second computer interface buses, respectively, into control bits and to decode control bits from the interface channel into control signals. Additionally, the HIC and PIC each include a transmitter and a receiver coupled to the translator. The transmitter converts parallel bits into serial bits and transmits the serial bits to the interface channel. The receiver receives serial bits from the interface channel and converts them into parallel bits.

FIG. 13 is a block diagram of one embodiment of a computer system 1300 using the interface of the present invention. Computer system 1300 includes an attached computer module (ACM) 1305 and a peripheral console 1310, which are described in greater detail in the application of William W. Y. Chu, Ser. No. 09/149,548, for "Personal Computer Peripheral Console With Attached Computer Module" filed on Sep. 8, 1998 and incorporated herein by reference. The ACM 1305 and the peripheral console 1310 are interfaced through an exchange interface system (XIS) bus 1315. The XIS bus 1315 includes power bus 1316, video bus 1317 and peripheral bus (XPBus) 1318, which is also herein referred to as an interface channel. The power bus 1316 transmits power between ACM 1305 and peripheral console 1310. In a preferred embodiment power bus 1316 transmits power at voltage levels of 3.3 volts, 5 volts and 12 volts. Video bus 1317 transmits video signals between the ACM 1305 and the peripheral console 1310. In a preferred embodiment, the video bus 1317 transmits analog Red Green Blue (RGB) video signals for color monitors, digital video signals (such as Video Electronics Standards Association (VESA) Plug and Display's Transition Minimized Differential Signaling (TMDS) signals for flat panel displays), and television (TV) and/or super video (S-video) signals. The XPBus 1318 is coupled to host interface controller (HIC) 1319 and to peripheral interface controller (PIC) 1320, which is also sometimes referred to as a bay interface controller.

In the embodiment shown in FIG. 13, HIC 1319 is coupled to an integrated unit 1321 that includes a CPU, a cache and a north bridge. In another embodiment, such as that shown in FIG. 17, the CPU 1705 and north bridge 1710 are separate rather than integrated units. In yet another embodiment, such as that shown in FIG. 18, the HIC and PIC are integrated with the north and south bridges, respectively, such that integrated



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HIC and north bridge unit 1805 includes an HIC and a north bridge, while integrated PIC and south bridge unit 1810 includes a PIC and a south bridge. FIG. 19 shows an attached computer module with integrated CPU/NB/Graphics 1915 and Integrated HIC/SB 1920. FIG. 20 shows an attached computer module with single chip 2025 fully integrated: CPU, Cache, Core Logic, Graphics controller and Interface controller.

FIG. 14 is a detailed block diagram of one embodiment of the HIC of the present invention. As shown in FIG. 14, HIC 1600 comprises bus controller 1610, translator 1620, transmitter 1630, receiver 1640, a PLL 1650, an address/data multiplexer (A/D MUX) 1660, a read/write controller (RD/WR Cntl) 1670, a video serial to parallel converter 1680 and a CPU control & general purpose input/output latch/driver (CPU CNTL & GPIO latch/driver) 1690.

HIC 1600 is coupled to an optional flash memory BIOS configuration unit 1601. Flash memory unit 1601 stores basic input output system (BIOS) and PCI configuration information and supplies the BIOS and PCI configuration information to A/D MUX 1660 and RD/WR Control 1670, which control the programming, read, and write of flash memory unit 1601.

Bus controller 1610 is coupled to the host PCI bus, which is also referred to herein as the primary PCI bus, and manages PCI bus transactions on the host PCI bus. Bus controller 1610 includes a slave (target) unit 1611 and a master unit 1616. Both slave unit 1611 and master unit 1616 each include two first in first out (FIFO) buffers, which are preferably asynchronous with respect to each other since the input and output of the two FIFOs in the master unit 1616 as well as the two FIFOs in the slave unit 1611 are clocked by different clocks, namely the PCI clock and the PCK. Additionally, slave unit 1611 includes encoder 1622 and decoder 1623, while master unit 1616 includes encoder 1627 and decoder 1628. The FIFOs 1612, 1613, 1617 and 1618 manage data transfers between the host PCI bus and the XPBus, which in the embodiment shown in FIG. 14 operate at 33 MHz and 66 MHz, respectively. PCI address/data (AD) from the host PCI bus is entered into FIFOs 1612 and 1617 before they are encoded by encoders 1622 and 1627. Encoders 1622 and 1627 format the PCI address/data bits to a form more suitable for parallel to serial conversion prior to transmittal on the XPBus. Similarly, address and data information from the receivers is decoded by decoders 1623 and 1628 to a form more suitable for transmission on the host PCI bus.

The multiplexed parallel A/D bits and some control bits input to transmitter 1630 are serialized by parallel to serial converters 1632 of transmitter 1630 into 10 bit packets. These bit packets are then output on data lines PD0 to PD3 of the XPBus. Other control bits are serialized by parallel to serial converter 1633 into 10 bit packets and sent out on control line PCN of the XPBus.

FIG. 15 is a detailed block diagram of one embodiment of the PIC of the present invention. PIC 11100 is nearly identical to HIC 1600 in its function, except that HIC 1600 interfaces the host PCI bus to the XPBus while PIC 11100 interfaces the secondary PCI bus to the XPBus. Similarly, the components in PIC 11100 serve the same function as their corresponding components in HIC 1600. Reference numbers for components in PIC 11100 have been selected such that a component in PIC 11100 and its corresponding component in HIC 1600 have reference numbers having the same two least significant digits. Thus for example, the bus controller in PIC 11100 is referenced as bus controller 11110 while the bus controller in HIC 1600 is referenced as bus controller 1610. As many of the elements in PIC 11100 serve the same functions as those

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served by their corresponding elements in HIC 1600 and as the functions of the corresponding elements in HIC 1600 have been described in detail above, the function of elements of PIC 11100 having corresponding elements in HIC 1600 will not be further described herein. Reference may be made to the above description of FIG. 14 for an understanding of the functions of the elements of PIC 11100 having corresponding elements in HIC 1600.

FIG. 16 is a schematic diagram of lines PCK, PD0 to PD3, and PCN. These lines are unidirectional LVDS lines for transmitting clock signals and bits from the HIC to the PIC. The bits on the PD0 to PD3 and the PCN lines are sent synchronously within every clock cycle of the PCK. Another set of lines, namely PCKR, PDR0 to PDR3, and PCNR, are used to transmit clock signals and bits from the PIC to HIC. The lines used for transmitting information from the PIC to the HIC have the same structure as those shown in FIG. 16, except that they transmit data in a direction opposite to that in which the lines shown in FIG. 16 transmit data. In other words they transmit information from the PIC to the HIC. The bits on the PDR0 to PDR3 and the PCNR lines are sent synchronously within every clock cycle of the PCKR. Some of the examples of control information that may be sent in the reverse direction, i.e., on PCNR line, include a request to switch data bus direction because of a pending operation (such as read data available), a control signal change in the target requiring communication in the reverse direction, target busy, and transmission error detected.

The XPBus which includes lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, and PCNR, has two sets of unidirectional lines transmitting clock signals and bits in opposite directions. The first set of unidirectional lines includes PCK, PD0 to PD3, and PCN. The second set of unidirectional lines includes PCKR, PDR0 to PDR3, and PCNR. Each of these unidirectional set of lines is a point-to-point bus with a fixed transmitter and receiver, or in other words a fixed master and slave bus. For the first set of unidirectional lines, the HIC is a fixed transmitter/master whereas the PIC is a fixed receiver/slave. For the second set of unidirectional lines, the PIC is a fixed transmitter/master whereas the HIC is a fixed receiver/slave. The LVDS lines of XPBus, a cable friendly and remote system I/O bus, transmit fixed length data packets within a clock cycle.

The XPBus lines, PD0 to PD3, PCN, PDR0 to PDR3 and PCNR, and the video data and clock lines, VPD and VPCK, are not limited to being LVDS lines, as they may be other forms of bit based lines. For example, in another embodiment, the XPBus lines may be IEEE 1394 lines.

It is to be noted that although each of the lines PCK, PD0 to PD3, PCN, PCKR, PDR0 to PDR3, PCNR, VPCK, and VPD is referred to as a line, in the singular rather than plural, each such line may contain more than one physical line. For example, in the embodiment shown in FIG. 16, each of lines PCK, PD0 to PD3 and PCN includes two physical lines between each driver and its corresponding receiver. The term line, when not directly preceded by the terms physical or conductive, is herein used interchangeably with a signal or bit channel of one or more physical lines for transmitting a signal. In the case of non-differential signal lines, generally only one physical line is used to transmit one signal. However, in the case of differential signal lines, a pair of physical lines is used to transmit one signal. For example, a pair of physical lines together transmit a signal in a bit line or bit channel in an LVDS or IEEE 1394 interface.

A bit based line (i.e., a bit line) is a line for transmitting serial bits. Bit based lines typically transmit bit packets and

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use a serial data packet protocol. Examples of bit lines include an LVDS line, an IEEE 1394 line, and a Universal Serial Bus (USB) line.

FIGS. 21 and 22 are tables including the pin number, symbol, signal, standard and description for the pins on the peripheral and video connectors, respectively. FIG. 23 is a table showing the symbols, signals, data rate and description of signals on the XPBus, where RTN indicates a ground (GND) reference. In the above tables, P&D stands for plug and display and is a trademark of the Video Electronics Standards Association (VESA) for the Plug and Display standard, DDC2:SCL and DDC2:SDA stand for the VESA display data channel (DDC) standard 2 clock and data signals, respectively, SV stands for super video, V33 is 3.3 volts, and V5 is 5.0 volts. TMDS stands for Transition Minimized Differential Signaling and is a trademark of Silicon Images and refers to their Panel Link technology, which is in turn a trademark for their LVDS technology. TMDS is used herein to refer to the Panel Link technology or technologies compatible therewith.

The reserved data packet types can be used to support non-PCI bus transactions, e.g., USB transactions. The bits sent in the first nibble of each data packet indicate the type of the data packet. FIG. 24 is a table showing different types of first nibbles and their corresponding data packet types.

Although the functionality above has been generally described in terms of a specific sequence of steps, other steps can also be used. Here, the steps can be implemented in a combination of hardware, firmware, and software. Either of these can be further combined or even separated. Depending upon the embodiment, the functionality can be implemented in a number of different ways without departing from the spirit and scope of the claims herein. One of ordinary skill in the art would recognize other variations, modifications, and alternatives.

While the above is a full description of the specific embodiments, various modifications, alternative constructions and equivalents may be used. Therefore, the above description and illustrations should not be taken as limiting the scope of the present invention which is defined by the appended claims.

What is claimed is:

[1. A security protection method for a computer module, said method comprising:

inserting the computer module into a console;

initiating a security program in said module to read a security identification of said console and to read a security identification of said computer module;

determining of a predetermined security status based upon a relationship of said console identification and said computer module identification;

selecting said predetermined security status; and  
operating said computer module based upon said security status.]

[2. The method of claim 1 wherein said predetermined security status disables a network access to the computer module.]

[3. The method of claim 1 wherein said predetermined security status disables a secondary storage of information from said computer module to substantially prevent information to be transferred from a memory of the computer module to said secondary storage.]

[4. The method of claim 1 wherein said security program is provided in a system BIOS.]

[5. The method of claim 1 wherein said step of initiating reads said security identification of said computer module from a flash memory device.]

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[6. The method of claim 1 wherein said step of initiating reads said security identification of said console from a flash memory device.]

[7. The method of claim 1 wherein said console is selected from a desktop home computing device, an office desktop computing device, a mobile computing device, a television set-top computing device, and a co-worker's computing device.]

[8. A system for secured information transactions, the system comprising:

a console comprising a peripheral controller housed in the console;

a user identification input device coupled to the peripheral controller, the user identification input device being provided for user identification data; and

an attached computer module coupled to the console, the attached computer module comprising a security memory device stored with the user identification data.]

[9. The system of claim 8 wherein the user identification input device is a finger print reader.]

[10. The system of claim 8 wherein the user identification input device is a voice processing device.]

[11. A method for operating a module computer into one of a plurality of network systems, the method comprising:

providing a computer module, the module comprising a connection program;

inserting the computer module into a computer console, the computer console having access to a network;

receiving connection information from the computer console;

configuring the connection program to adapt to the connection information; and

establish a connection between the computer module and a server coupled to the network.]

[12. The method of claim 11 wherein the connection information comprises a connection protocol for providing the connection.]

[13. The method of claim 12 wherein the connection protocol is selected from TCP/IP, or mobile IP.]

[14. A computer for information transactions, comprising: a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly connected to the central processing unit; and

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect ("PCI") bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a PCI bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

[15. The computer of claim 14, further comprising a connector coupled to a console, wherein the second LVDS channel communicates the encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

[16. The computer of claim 15 further comprising a graphics controller that conveys digital video display information from the connector to the console.

[17. The computer of claim 15 wherein the console comprises a mass storage device that couples to the second LVDS channel.

[18. A computer system, comprising:

a console comprising a Liquid Crystal Display (LCD) display and a first Low Voltage Differential Signal (LVDS)

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channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and  
a computer coupled to the console through a connector, the computer comprising

an integrated central processing unit and graphics controller in a single chip directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a mass storage unit coupled to the central processing unit and graphics controller in a single chip;

wherein the graphics controller conveys digital video display information to the LCD display through the connector upon coupling to the console.

19. The computer system of claim 18 wherein the computer further comprises a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect ("PCI") bus, the peripheral bridge directly conveying an encoded serial bit stream of address and data bits of a PCI bus transaction.

20. The computer system of claim 19 wherein the peripheral bridge conveys the encoded serial bit stream of address and data bits of the PCI bus transaction to the first LVDS channel upon coupling of the computer to the console.

21. A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit Universal Serial Bus (USB) Protocol data in opposite directions;

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a connector coupled to the first LVDS channel; and

a main memory directly coupled to the central processing unit.

22. The computer of claim 21 wherein the second LVDS channel communicates an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

23. The computer of claim 21 wherein the first LVDS channel conveys Universal Serial Bus (USB) Protocol data to a console through the connector.

24. A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller;

a differential signal channel directly extending from the integrated central processing unit and graphics controller to convey digital video display information;

a connector for coupling to a console; and

a second differential signal channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second differential signal channel conveys Universal Serial Bus (USB) protocol data through the connector to the console.

25. The computer of claim 24 wherein the LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

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26. A modular computer system, comprising:

a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a mass storage unit coupled to the central processing unit,

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction over the second LVDS channel; and

wherein the second LVDS channel communicates to the first LVDS channel in the console upon the computer coupling to the console.

27. The modular computer system of claim 26 wherein the second LVDS channel conveys the encoded serial bit stream of the PCI bus transaction to the first LVDS channel upon coupling of the computer module to the console.

28. The modular computer system of claim 27 wherein the console further comprises a mass storage device that couples to the first and second LVDS channels.

29. A modular computer system, comprising:

a console comprising a power supply; and

a computer coupled to the console through a connector, the computer comprising

a central processing unit,

a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions,

a peripheral bridge directly coupled to the first LVDS channel to communicate an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction, the peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, and

wherein the power supply supplies power to the computer upon coupling to the console.

30. The computer system of claim 29 further comprising a second LVDS channel that conveys the encoded serial bit stream of address and data bits of the PCI bus transaction, wherein the second LVDS channel directly extends from the central processing unit.

31. A modular computer system, comprising:

a console comprising a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a computer that couples to the console, the computer comprising

an integrated central processing unit and graphics controller in a single chip, directly connected to a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, and

a connector that couples to the first LVDS channel in the console.



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32. The modular computer system of claim 31 wherein the second LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

33. The modular computer system of claim 31 wherein the first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction.

34. The modular computer system of claim 31 wherein the computer conveys Universal Serial Bus (USB) protocol data to the console upon the computer coupling to the console.

35. A computer, comprising:

a central processing unit;

a main memory directly connected to the central processing unit;

a peripheral bridge directly coupled to the central processing unit without any intervening Peripheral Component Interconnect (PCI) bus, wherein the peripheral bridge directly conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction over a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions; and

a mass storage device directly coupled the peripheral bridge.

36. The computer of claim 35 further comprising a graphics controller coupled to the peripheral bridge.

37. A computer, comprising:

a central processing unit directly connected to a first Low Voltage Differential Signal (LVDS) channel to convey a first encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction;

a main memory directly connected to the central processing unit; and

a peripheral bridge directly coupled to the central processing unit without any intervening PCI bus, wherein the peripheral bridge directly conveys a second encoded serial bit stream of address and data bits of a (PCI) bus transaction over a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions.

38. The computer of claim 37 further comprising a connector coupled to a console, wherein the second LVDS channel communicates the second encoded serial bit stream of address and data bits of the PCI bus transaction to the console.

39. The computer of claim 38 further comprising a graphics controller to convey digital video display information from the connector to the console.

40. The computer of claim 38 wherein the console comprises a peripheral device that couples to the second LVDS channel.

41. A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the integrated cen-

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tral processing unit and graphics controller conveys digital video display signals through a second differential signal channel;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

a mass storage device comprising flash memory.

42. The computer of claim 41 wherein the second differential signal channel conveys Transition Minimized Differential Signaling (TDMS) information.

43. The computer of claim 41 wherein the first LVDS channel conveys an encoded serial bit stream of address and data bits of a Peripheral Component Interconnect (PCI) bus transaction.

44. A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller;

a mass storage device comprising flash memory;

a connector that conveys Universal Serial Bus (USB) protocol information to a console; and

a second LVDS channel comprising two sets of unidirectional, serial bit channels to transmit data in opposite directions, wherein the second LVDS channel conveys said USB protocol information to the console through the connector.

45. A computer, comprising:

a Central Processing Unit (CPU) directly connected to a Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect ("PCI") bus transaction in opposite directions;

a main memory directly connected to the CPU; and

a mass storage device coupled to the CPU.

46. The computer of claim 45 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

47. The computer of claim 45 wherein the mass storage device comprises flash memory.

48. A computer, comprising:

an integrated central processing unit and graphics controller in a single chip directly connected to a first Low Voltage Differential Signal (LVDS) channel comprising two sets of multiple, unidirectional, serial bit channels to convey an encoded serial bit stream of encoded address and data bits of a Peripheral Component Interconnect (PCI) bus transaction in opposite directions;

a main memory directly coupled to the integrated central processing unit and graphics controller; and

an Ethernet communication device coupled to the first LVDS channel.

49. The computer of claim 48 further comprising a connector, wherein the connector connects to a console comprising a power supply, and the power supply supplies power to the computer upon coupling to the console.

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